ICETEEE-2020

International Conference on Emerging Technology in Electrical and Electronics Engineering

Jaipur, India

06th - 07th February, 2020

Organized by:

Institute For Engineering Research and Publication (IFERP)

Editorial:

We cordially invite you to attend the ***International Conference on Emerging Technology in Electrical and Electronics Engineering (ICETEEE-2020)*** organized by Institute For Engineering Research and Publication (IFERP) which will be held at ***Souvenir Premier Hotel, Jaipur, India*** on ***February 06th-07th, 2020***. The main objective of ***ICETEEE*** is to provide a platform for researchers, students, academicians as well as industrial professionals from all over the world to present their research results and development activities in relevant fields of Recent Advancements in Engineering and Technology. This conference will provide opportunities for the delegates to exchange new ideas and experience face to face, to establish business or research relationship and to find global partners for future collaboration.

These proceedings collect the up-to-date, comprehensive and worldwide state-of-art knowledge on cutting edge development of academia as well as industries. All accepted papers were subjected to strict peer-reviewing by a panel of expert referees. The papers have been selected for these proceedings because of their quality and the relevance to the conference. We hope these proceedings will not only provide the readers a broad overview of the latest research results but also will provide the readers a valuable summary and reference in these fields.

The conference is supported by many universities, research institutes and colleges. Many professors played an important role in the successful holding of the conference, so we would like to take this opportunity to express our sincere gratitude and highest respects to them. They have worked very hard in reviewing papers and making valuable suggestions for the authors to improve their work. We also would like to express our gratitude to the external reviewers, for providing extra help in the review process, and to the authors for contributing their research result to the conference.

Since December 2019, the Organizing Committees have received more than 50 manuscript papers, and the papers cover all the aspects in Electrical and Electronics Engineering. Finally, after review, about 21 papers were included to the proceedings of ***ICETEEE-2020***.

We would like to extend our appreciation to all participants in the conference for their great contribution to the success of ***ICETEEE-2020*** We would like to thank the keynote and individual speakers and all participating authors for their hard work and time. We also sincerely appreciate the work by the technical program committee and all reviewers, whose contributions made this conference possible. We would like to extend our thanks to all the referees for their constructive comments on all papers; especially, we would like to thank to organizing committee for their hard work.

Mr. Ankit Rath
Chief Scientific Officer (CSO)
Institute for Engineering Research and Publication (IFERP)

Message

IFERP is hosting the **International Conference on Emerging Technology in Electrical and Electronics Engineering** this year in month of February. The main objective of **ICETEEE** is to grant the amazing opportunity to learn about groundbreaking developments in modern industry, talk through difficult workplace scenarios with peers who experience the same pain points, and experience enormous growth and development as a professional. There will be no shortage of continuous networking opportunities and informational sessions. The sessions serve as an excellent opportunity to soak up information from widely respected experts. Connecting with fellow professionals and sharing the success stories of your firm is an excellent way to build relations and become known as a thought leader.

I express my hearty gratitude to all my Colleagues, Staffs, Professors, Reviewers and Members of organizing committee for their hearty and dedicated support to make this conference successful. I am also thankful to all our delegates for their pain staking effort to travel such a long distance to attain this conference.

Sincerely,

Ankit Rath

ICETEEE-2020

International Conference on Emerging Technology in Electrical and Electronics Engineering

Keynote Speaker

R.M. Mehra

Professor Emeritus

Sharda University

Greater Noida, India

Message

It is a matter of great pleasure that the Institute For Engineering Research and Publication (IFERP), one of the world's largest non-profitable professional associations operating under Technoarete Research and Development Association (TRADA), is organizing an International Conference on Emerging Technology in Electrical and Electronics Engineering (ICETEEE-20) from 06th to 07th February, 2020 at Jaipur, India.

The theme of this conference revolves around the current scenario in fields of engineering, technology, and management research areas synchronically on an indivisible platform. This ICETEEE will be an arena for Academicians, Doctorates, Scientists, Researchers, Students and Business Delegates to attend and showcase their recent research in front of huge gathering of people from all around the Globe. I am sure that this conference will provide a platform for exchange of ideas and thoughts among the eminent scientist, scholars and delegates from all over the world to enrich the knowledge in the field and ensuring collaborations within and outside India. Participants will also be able to build new networks to meet different personalities and learn about the latest tools available.

I wish a grand success of the conference.

R.M. Mehra

R.M. Mehra

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PAPERS

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Fabrication and Characterizations of ionic polymers blend membrane (IPC) using graphene oxide base for the actuation application

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Abstract:

PVDF/PSSA/PVP blend membrane in the blend ratio of 60/15/25 and 40/30/30 were prepared by solution cast technique. The actuating performance of PVSD/PSSA/PVP (40/30/30) and water uptake (WUP) of blend membrane was found to be higher than blend ratio of 60/15/25. PVDF/PSSA/PVP (40/30/30) characterized by different techniques such as XRD, SEM, FTIR and electrical conductivity was determined at different frequency. Ionic –polymer composite (IPC) actuator that display continuously large actuation displacement without back relaxation and with large blocking force at direct current (DC) voltage (1-30V). In this membrane PSSA is the polyelectrolyte, PVP is the hydrophilic basic polymer and PVDF is the hydrophobic polymer

1. INTRODUCTION

In the last few decades there has been high much attention in actuators system that changes or converts electrochemical energy into mechanical energy for different application such as sensors, transducers, actuators and different biomedical devices. Different types of polymer actuators based on ion-exchange membranes exhibit large bending displacement (1-10mm) under low applied voltage (1-5V) and have different properties such as flexibility lightweight and biocompatibility [1-5]. Now carbonaceous nanomaterials such as graphene oxide (GO), reduced graphene oxide (rGO), fullerene, carbon nanotube (CNT) etc. have attention researches due to their notable mechanical strength, flexibility, large surface area, light weight, excellent chemical stability and high carrier mobility. Many researcher efforts have been made to the powerfully add in CNT, GO and nanoscale materials into the polymer matrix and also used as electrode in the actuators [6-8].

Polymer matrixes are a novel class of all-organic electro active polymers that can operate both as electromechanical actuators and as sensors. The aim of this research article to develop and characterize polymer blend membrane for the actuation purpose which actuate in air at low voltage (DC). IPC actuators have different types of advantages over the traditional EAP or IPMC actuators like good input response, light weight, small structure high efficiency of power transition etc. [8-10].

Underwater micro-robots have a huge demand because of their easy maneuverability and efficiency. Underwater micro-robot including swimming micro-robots and walking micro-robots has found applications in industrial, medical and military purposes [8-14].

Further these IPC actuators because of their light weight, flexible nature and low initial applied voltage for movement, can be used as wireless switches in detonators for explosives.

The polymer blend membranes prepared by PVDF/PSSA/PVP with the blend ration 60/15/25 and 40/30/30 with the graphene oxide and polyaniline electrode coating. The polymer blend membrane composites with different compositions will be characterized for their electrical, physical and chemical properties.

2. MATERIALS AND METHODS

2.1 Materials

PVDF, Polyvinylidene fluoride, Poly (sodium 4-styrenesulfonate) (PSSA), Polyvinylpyrrolidone (PVP), Aniline, Toluene, Copper Sulphate, Graphite Flake, Sodium nitrate (Na_2No_3), Sulfuric acid (H_2So_4) and Dimethylformamide (DMF) used as a solvent.

2.1.1 Preparation of Graphene oxide (GO)

Graphical representation of synthesis of graphene oxide using modified Hummers method is given in Fig.1

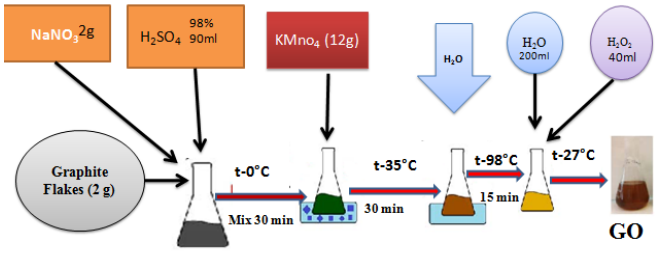

Fig.1. Synthesis of graphene oxide (GO) using modified hummers method

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2.1.2 Preparation of polyaniline

Toluene and Aniline taken in 1:4 weight ratios and 0.1M solution of copper sulphate was used for polymerization. This mixture was kept for 6–8 h and the precipitate obtained this precipitate washed and heated at 100 °C for 10 h to form PANI.

2.1.3 Fabrication of PVDF/PSSA/PVP (40/30/30) blend membrane

Polyvinylidene fluoride (PVDF), Polyvinylpyrrolidone (PVP), and Poly(4-styrenesulfonic acid) (PSSA) were taken in the ratio (60:15:25) Both PVDF & PVP were stirred with *N*,*N*-Dimethylformamide (DMF) in separate sample bottles for ~48h; then both the solutions are mixed and stirred for ~12 hrs. PSSA was added into the blend of PVDF+PVP and further stirred for 48 hrs in order to have a uniform solution. The viscous solution was casted in polypropylene petridish, and left in lab conditions for solvent evaporation, after that the film was formed.

2.1.4 Electrode fabrication on the polymer membrane PVDF/PVP/PSSA (40:30:30)

Firstly 0.1g polyaniline (PANI) dissolve in 10ml DMF with continuous stirring for 24h, and after that the graphene oxide (GO) mixed (90wt% of polyamine, 0.09g) with Polyaniline solution with continuous string for 48 h, to form a viscous solution of GO/PANI and after that the polymer blend membrane is dipped in a viscous solution of GO/PANI for 8 hours. The polymer blend membrane film was taken out, washed with distilled water and dipped again for 8 hours, this process repeated thrice so as to form a smooth and proper coating (Fig.2)

Once the coating is finished, the membrane is dipped in 1.5N LiCl solution for cation exchange process. The film is dipped in 1.5N LiCl solution for cation exchange process for 24h then film was taken out for actuation process.

Fig.2. (a is the Viscous solution of GO/PANI, b is s the coated film, and c is the film dipped in 1.5N lithium chloride solution for cat ion exchange process).

3. RESULT AND DISCUSSION

3.1 Water uptake potential

Water uptake potential of PVDF/PSSA/PVP blend membrane with different composition are given in Table 1 and Table 2

Table 1 Water uptake potential data

System	WUP	Dry Film (Weight, g)	Wet Film (Weight, g))	WUP
PVDF+PVP +PSS (40:30:30)	$\frac{W_w - W_D}{W_D}$	1.019	2.241	1.3

Water Uptake Potential (WUP)
Dry Film weight: 1.009g
Film dipped in water for 24h
Film weight after dipping: 2.241g
Water Uptake Potential: 1.1

Table 2 Water uptake potential data

System	WUP	Dry Film (Weight, g)	Wet Film (Weight, g))	WUP
PVDF+PVP +PSS (60:15:25)	$\frac{W_w - W_D}{W_D}$	0.07	0.08	0.11

The WUP of this system was excellent (WUP should be nearly equal to or greater than 1), and also the conductivity was good compare then other above systems. Therefore the system PVDF/PSSA/PVP (40:30:30) has been carried forward for actuation purpose.

3.2 Impedance Analysis

The conductivity study of the polymer electrolyte film was carried out with CHI 604D electrochemical workstation. A small part of the film was fixed between two SS electrodes and frequency range was 1 MHz to 1 Hz. The conductivity calculated by the given Eq.1. The obtained conductivity value was 6.6×10^{-5}S/cm.(Fig.3).

$$\sigma = \frac{1}{R_b} \times \frac{l}{A} \qquad \textbf{Eq. (1)}$$

Where,
R_b = bulk resistance
L = thickness of thin film.
A = area of the thin film.

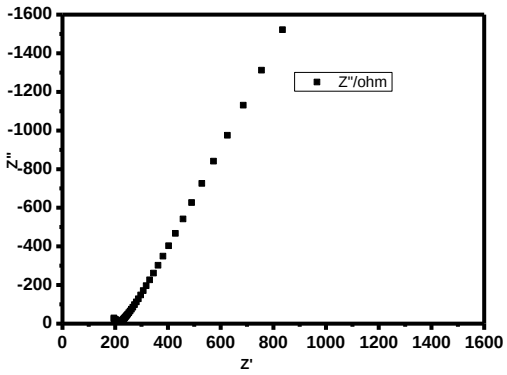

Fig. 3. Impedance graph of PVDF+ PVP +PSSA (40:30:30)

3.3 Optical Microscopy image

The optical image of polymer blend membrane given in Fig. the dark region causes amorphous nature of polymer blend membrane Therefore, the conductivity increased of polymer blend membrane. (Fig.4.)

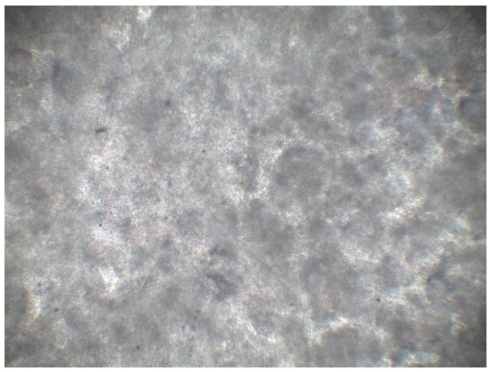

Fig.4. Optical microscopy image of PVDF+ PVP +PSSA (40:30:30)

3.4 X-ray Diffraction studies

XRD pattern PVDF/PSSA/PVP (40:30:30) is given in Fig (5). The peaks corresponding to twice he diffraction angle and d value in brackets 18.3 (110), 26.4 (020) and 41.7 (021). The graph has more crystalline and have higher intensity.

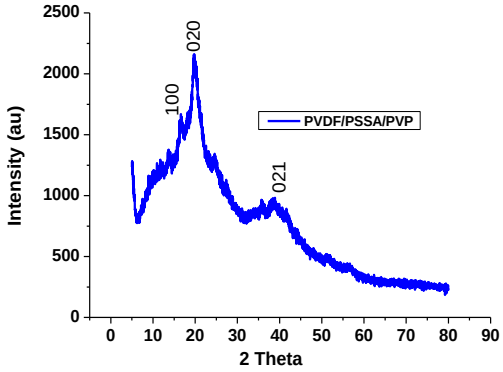

Fig.5 XRD Pattern of PVDF/PSSA/PVP

3.5 Displacement graph of actuator

The actuation performance and graph of PVDF/PSSA/PVP (40:30:30) blend membrane is given in Fig. 6. The actuation performance was taken with DC voltage (1-30V). It was found that the highest actuation at 29 V up to 0.65mm.

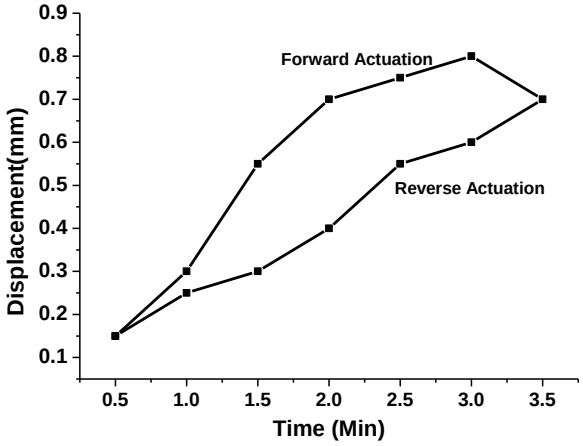

Fig.6 Actuation graph of PVDF/PSSA/PVP (40:30:30)

4. CONCLUSION

The polymer blend membrane PVDF/PSSA/PVP with different composition prepared by simple solution cast technique and blend membrane were characterized by different techniques such as XRD and optical microscope, Electrical measurement was also measured. It was found that the PVDF/PSSA/PVP with blend ratio (40:30:30) has higher actuation at 29V (DC). Therefore, the PVDF/PSSA/PVP based IPC actuator with these characteristics can be utilized as biomimetic sensors, actuators, transducers, artificial muscles, and biomedical devices.

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Fault Tolerant Speed Control of Five Phase Induction Motor with fuzzy logic controller for Electric Vehicle

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Abstract:

The multiphase induction motor is a highly preferable choice for the electric vehicle application where the reliability and safety of passengers are one of the major concerns. This paper presents a fuzzy logic based novel speed controller, which deals with fault tolerant operation of five phase induction motor (FPIM). The rotor oriented field control (RFOC) scheme is employed for controlling the FPIM. Under the fault condition the controller reconfiguration is minimized by modelling the open circuit fault using method of back EMF calculation in faulty phase. The inner current control is achieved using hysteresis controllers due to their simplicity and ease of implementation. The outer speed controller action is designed through a robust fuzzy logic controller with fine tuned membership function to generate optimal torque reference. The complete RFOC scheme for faulted FPIM is built in MATLAB/Simulink incorporating fuzzy logic controller. The comparative analysis between fuzzy logic speed controller (FLSC) and the conventional proportional-integral (PI) controller is presented for its dynamic response, robustness and parameter sensitivity under healthy and faulty condition of FPIM. Different speed tracking performances under healthy, faulty and fault tolerant mode of operation are enhanced using proposed FLSC as compared to PI controller.

Keywords:

Fault Tolerance, Five Phase Induction Motor (FPIM), Fuzzy Logic Controller, Electric Vehicle

1. INTRODUCTION

Rapid diminution of fossil fuel and need of green environment has attracted the world automobile technology to focus on Electrical propulsion system. The latest challenge in design of electric propulsion system for electric vehicle is to develop a cost-effective, safety critical, robust and reliable drive. Extensive research has been conducted to select appropriate motor for electric vehicle. Considering merits and demerits of the existing motor technologies stated in [1] multiphase induction motors are highly preferable choice as a propulsion drive of electric vehicle. In addition to that the three phase drives need redundant equipments and over dimensioned designs with increased cost and space requirements for the fault tolerant control of drive [2]. Multiphase drives can manage faulty operation without the need of extra equipment, depending on the specific electrical machine configuration [3]. In the electric vehicle drive system the major fault prone locations are the inverter, condition monitoring circuits and the electric motor are as shown in fig. 1. The effect of winding faults as well as sensor fault is same in case of three phase or five phase drive system. In the electric drive system the power converter faults are more prominent and can affect the entire system behavior. As shown in fig. 1, they can be again classified as gate failure, single switch short circuit (SSC) fault or open circuit (SOC) fault, phase leg open (PLO) or short circuit (PLS) fault, or line open fault. These kinds of faults can occur due to the burning out of the power electronic switches or driver failure.

In the literature, various control techniques like FOC (field oriented control) [4-6], MPC (model predictive control) [7], proportional resonant controller (PR) [8,9], direct torque control [10] and others are addressed for fault tolerant control of multiphase induction motor. Few researchers have focused on non linear control techniques and intelligent controllers for fault tolerant mode of operations like fuzzy logic control, Sliding Mode Control (SMC) [11] and others. Similar approach of non linear controller has been reported for other motors like BLDC in [12]. However the FLC based speed controllers has not been examined under open circuit fault condition of FPIM drive.

Also, same has not provided any information regarding potency of FLC under parameters uncertainty under the fault condition. Hence, development and real-time implementation of the FLC-based PFIM is important for appropriate solution of electric vehicle under healthy and open circuit fault condition. The most authoritative contribution of this paper by equate with other works is to enquire the dynamic performance of FPIM drive using the FLSC under healthy and faulty condition.

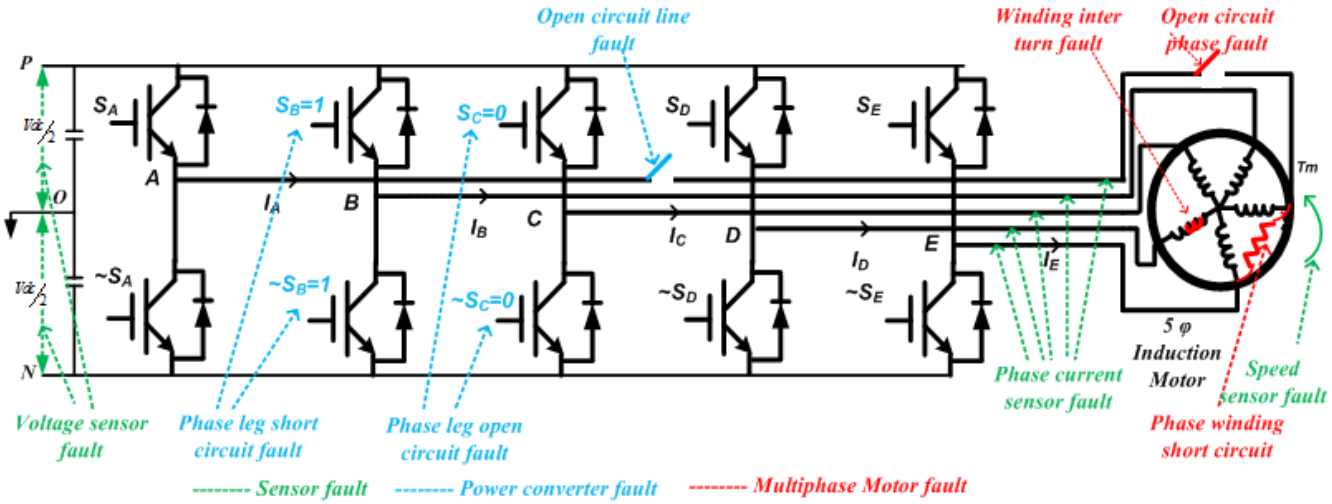

Fig. 1. Different types of fault in five phase drive

Also, same has not provided any information regarding potency of FLC under parameters uncertainty under the fault condition. Hence, development and real-time implementation of the FLC-based PFIM is important for appropriate solution of electric vehicle under healthy and open circuit fault condition. The most authoritative contribution of this paper by equate with other works is to enquire the dynamic performance of FPIM drive using the FLSC under healthy and faulty condition.

The above attempt is achieved all through the following points.

1) To facilitate that a prototype 2 HP five phase induction motor model is formed in d-q frame under faulty phase condition. The fault is modelled by considering the back EMF calculation in faulty phase under one phase open circuit condition;
2) The post fault currents are obtained by considering the circular trajectory of stator d-q flux to remain unchanged. In order to get the modified current reference under fault condition the non-energy current components are utilized as weighted energy current components;
3) The minimum torque ripples criterion is selected to decide the corresponding weight factor for the new reference currents generation;
4) Based on the preceding model fuzzy logic speed controller in indirect vector controlled five phase induction motor for healthy and faulty condition is proposed and membership functions are tuned for the robust performance;
5) Verify and compares the robustness of the proposed controller with PI controller under different healthy, faulty and fault tolerant conditions;
6) Examine the THD (Total Harmonic Distortion) of stator current under application of both the controllers.

In summary the main accusative of this work is to design a fuzzy based robust speed controller which works equally well with healthy and open circuit fault condition of the FPIM drive for electric vehicle. Robustness of the proposed controller in healthy and faulty condition at various operating points is verified through simulation results. The paper has been conferred in following pattern. In section II five phase induction motor modelling under healthy condition is presented in brief and under open circuit fault is formulated. Section III discusses fault tolerant indirect rotor field oriented control during fault condition. Section IV presents fuzzy speed controller design. Section V shows various MATLAB/Simulink results for different operating condition followed by concluding remarks in section V.

2. FIVE PHASE INDUCTION MOTOR (FPIM) MODELING IN HEALTHY AND FAULTY CONDITION

2.1 Five phase machine modelling in healthy condition

The multiphase winding can be reduced to a set of two phase winding by using the transformation matrix, which in turn eliminates the time varying inductances from the voltage, current and flux equations.

$$\left[f_{\alpha\beta xy0} \right] = K_s \left[f_{abcde} \right] \tag{1}$$

$$K_s = \sqrt{\frac{2}{5}} \begin{bmatrix} 1 & \cos(\varphi) & \cos(2\varphi) & \cos(2\varphi) & \cos(\varphi) \\ 0 & -\sin(\varphi) & -\sin(2\varphi) & \sin(2\varphi) & \sin(\varphi) \\ 1 & \cos(2\varphi) & \cos(\varphi) & \cos(\varphi) & \cos(2\varphi) \\ 0 & -\sin(2\varphi) & \sin(\varphi) & -\sin(\varphi) & \sin(2\varphi) \\ \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} \end{bmatrix} \tag{2}$$

The transformation matrix K_s [13] is used to convert voltages, currents and fluxes into stationary $[\alpha \ \beta \ x \ y \ 0]$ reference frame which is also known as decoupling matrix. The α-β plane is connected with energy conversion

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variables and responsible for fundamental torque development. The x - y plane is associated with loss producing components, hence for the torque production, the x-*y* components do not contribute for undistorted sinusoidal distribution of flux in the airgap. The last row is associated with the zero sequence components, which may be ignored for an isolated neutral point [14]. For the short circuited squirrel cage rotor x-y components are absent. The angle in transformation matrix $\theta = (2\pi/5)$. The *α-β* equations are further rotated to synchronous reference frame and the model equations are shown below. The *x-y* components do not link with rotor and contribute to torque, so they are not rotated.

$$\left.\begin{aligned} V_{ds} &= R_s I_{ds} + \frac{d}{dt}\psi_{ds} - \omega_e \psi_{qs},\ V_{xs} = R_s I_{xs} + \frac{d}{dt}\psi_{xs}, \\ V_{qs} &= R_s I_{qs} + \frac{d}{dt}\psi_{qs} + \omega_e \psi_{ds}, V_{ys} = R_s I_{ys} + \frac{d}{dt}\psi_{ys}, \\ V_{0s} &= R_s I_{0s} + \frac{d}{dt}\psi_{0s} \end{aligned}\right\} (3)$$

$$\left.\begin{aligned} V_{dr} &= R_r I_{dr} + \frac{d}{dt}\psi_{dr} - (\omega_e - P\omega_r)\psi_{qs} = 0 \\ V_{qr} &= R_r I_{qr} + \frac{d}{dt}\psi_{qr} - (\omega_e - P\omega_r)\psi_{ds} = 0 \end{aligned}\right\} \quad (4)$$

The flux linkage expressions with iron losses neglected are ,

$$\left.\begin{aligned} \psi_{ds} &= L_s I_{ds} + L_m I_{dr} \\ \psi_{qs} &= L_s I_{qs} + L_m I_{qr} \end{aligned}\right\} \quad (5)\ , \quad \left.\begin{aligned} \psi_{xs} &= L_{ls} I_{xs} \\ \psi_{xs} &= L_{ls} I_{xs} \end{aligned}\right\} \quad (6)$$

$$\left.\begin{aligned} \psi_{dr} &= L_m I_{ds} + L_r I_{dr} \\ \psi_{qr} &= L_m I_{qs} + L_r I_{qr} \end{aligned}\right\} \quad (7),\ \left.\begin{aligned} \psi_{xr} &= L_{lr} I_{xr} \\ \psi_{yr} &= L_{lr} I_{yr} \end{aligned}\right\} \quad (8)$$

The above terms are rearranged to obtain the state space model of motor as shown in (11) is further used for rotor field oriented vector control.

The electromagnetic torque in power invariant form is expressed as

$$T_e = P\frac{L_m}{L_r}(\Psi_{dr}\, i_{qs} - \Psi_{qr}\, i_{ds}) \quad (9)$$

Torque balancing equation is

$$J\frac{d\omega_r}{dt} + B\omega_r = T_e - T_L \quad (10)$$

Where, *Lm*, *Ls* and *Lr* are representation of magnetizing, *stator* and *rotor* inductances respectively.

The subscripts ds, qs, dr and qr represents d and q-axis stator and rotor quantities respectively. ω_e is reference frame angle speed and ω_r is the rotor angle speed of the rotor in rad/sec. ψ denotes flux linkage. R_r and R_s are the rotor and stator resistances per phase. *P* is representation of pole pairs number. J is representation of moment of inertia and *B* is representation of coefficient of viscous friction. T_L and *Te* are the load and developed torque respectively.

2.2 Five Phase induction motor modeling under Open circuit fault

A Five phase induction motor with symmetrical and distributed winding is considered for the analysis under open circuit. It is assumed here that the machine windings are healthy and the fault is due to failure of power converter switches. In the literature different approaches are used to model faulty multiphase machine. One approach is to use the traditional Clarke transformation matrix (*Ks*) in healthy state, and under faulty phase reduce order transformation is used [8]. However the controller reconfiguration is must because of machine equations obtained from the reduced order transformation have different machine parameters. Here the method based on back EMF calculation [12] is used for modeling the open phase condition so that the minimum change in the control strategy is required.

By using the transformation matrix *Ks*, $[f_{\alpha\beta xy0}]$ can be rewritten as follows:

$$\frac{d}{dt}\begin{bmatrix} I_{ds} \\ I_{qs} \\ \psi_{dr} \\ \psi_{qr} \end{bmatrix} = \begin{bmatrix} -a_1 & \omega_e & a_2 & Pa_3\omega_r \\ -\omega_e & -a_1 & Pa_3\omega_r & a_2 \\ a_5 & 0 & -a_4 & \omega_{sl} \\ 0 & a_5 & -\omega_{sl} & -a_4 \end{bmatrix} + \begin{bmatrix} I_{ds} \\ I_{qs} \\ \psi_{dr} \\ \psi_{qr} \end{bmatrix} + \begin{bmatrix} c & 0 \\ 0 & c \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{ds} \\ V_{qs} \end{bmatrix} \quad (11)$$

$$\sigma = 1 - \frac{L_m^{\,2}}{L_r L_s},\ a_1 = \frac{1}{\sigma L_S}\left(R_S + R_r\frac{L_m^{\,2}}{L_r^{\,2}}\right),\ a_2 = \frac{1}{\sigma L_S} R_r \frac{L_m^{\,2}}{L_r^{\,2}},\ a_3 = \frac{1}{\sigma L_S}\frac{L_m}{L_r},\ a_5 = \frac{R_r L_m}{L_r},\ a_4 = \frac{R_r}{L_r},\ \omega_e - P\omega = \omega_{sl},\ c = \frac{1}{\sigma L_S}$$

$$f_{\alpha s} = \sqrt{\frac{2}{5}}\left(\begin{aligned} &f_{as} + f_{bs}\cos(\gamma) + \\ &f_{cs}\cos(2\gamma) + f_{ds}\cos(2\gamma) + f_{es}\cos(\gamma) \end{aligned}\right) \quad (12)$$

$$f_{\beta s} = \sqrt{\frac{2}{5}}\left(\begin{aligned} &-f_{bs}\sin(\gamma) - \\ &f_{cs}\sin(2\gamma) + f_{ds}\sin(2\gamma) + f_{es}\sin(\gamma) \end{aligned}\right) \quad (13)$$

$$f_{xs} = \sqrt{\frac{2}{5}}\left(\begin{aligned} &f_{as} + f_{bs}\cos(2\gamma) + \\ &f_{cs}\cos(\gamma) + f_{ds}\cos(\gamma) + f_{es}\cos(2\gamma) \end{aligned}\right) \quad (14)$$

$$f_{ys} = \sqrt{\frac{2}{5}}\left(\begin{aligned} &-f_{bs}\sin(2\gamma) + \\ &f_{cs}\sin(\gamma) - f_{ds}\sin(\gamma) + f_{es}\cos(\gamma) \end{aligned}\right) \quad (15)$$

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$$f_{0s} = \sqrt{\frac{1}{5}}\left(f_{as} + f_{bs} + f_{cs} + f_{ds} + f_{es} \right) \quad (16)$$

The variable ***f*** describes current and voltage in the above equations. Considering phase 'a' is open, machine voltages become unbalanced. Phase 'a' voltage becomes unknown, due to which, $V_{\alpha s}$, V_{xs} and V_{0s} becomes unknown in eq. (12), (14), and (16). The following dependencies can be derived:

$$f_{\alpha s} - f_{xs} = \sqrt{\frac{2}{5}}\left(f_{bs} - f_{cs} - f_{ds} + f_{es} \right) * \left(\cos(\gamma) + \cos(2\gamma)\right) = \mathrm{E} \quad (17)$$

$$f_{\alpha s} + f_{xs} = 2\sqrt{\frac{2}{5}}(f_{as}) + \sqrt{\frac{2}{5}}\left(f_{bs} + f_{cs} + f_{ds} + f_{es} \right) \quad (18)$$

Equation (17) is used to eliminate unknown voltage of phase 'a' and equation (18) is used to get current relationship. Now, as faulted phase current i_{as}=0 and Kirchoff's current law applied to applied to star connected five phase induction motor results into eq. (19):

$$i_{\alpha s} + i_{xs} = 2\sqrt{\frac{2}{5}}(0) + \sqrt{\frac{2}{5}}(0) = 0 \Rightarrow i_{\alpha s} = -i_{xs} \quad (19)$$

Equation (19) can be substituted in (6) to get V_{xs},

$$V_{xs} = -R_s i_{\alpha s} - \frac{d}{dt} L_{ls} i_{\alpha s} \quad (20)$$

The Eq. (20) is substituted into equation Eq. (17)

$$V_{\alpha s} = \sqrt{\frac{2}{5}}\left(V_{bs} - V_{cs} - V_{ds} + V_{es} \right) * \left(\left(\cos(\gamma) + \cos(2\gamma)\right) \right) - \left(R_s i_{\alpha s} + \frac{d}{dt} L_{ls} i_{\alpha s} \right) \quad (21)$$

3. FIVE PHASE INDUCTION MOTOR CONTROL SCHEME

The five phase induction motor control is under healthy and faulty condition is obtained using rotor oriented field oriented control (RFOC) scheme.

3.1 Prefault operation under healthy condition

Under healthy condition, the *α–β* current components are only responsible for torque production. The *x–y* components do not contribute to the energy conversion process. Therefore only the *α–β* currents are used for reference current generation while the *x–y* current components are regulated to zero. For the five phase induction motor, the RFOC is obtained as follows.

The rotor flux orientation angle is calculated in (22). The slip angular speed is obtained as in (23). The reference currents are generated as in (24).

$$\theta_{\psi_r} = \int \omega_s dt = \int \left(\omega_{sl} + \omega_r \right) dt \quad (22)$$

$$\omega_{sl} = \left(\frac{1 + P\tau_r}{\tau_r} \right) \left(\frac{i_{qs}^*}{i_{ds}^*} \right) \quad (23)$$

$$i_{ds}^* = \frac{\psi_{dr}^*}{L_m}, i_{qs}^* = \frac{T_e^*}{k_t i_{ds}}, \text{ where } k_t = \frac{5PL_m^2}{4L_r} \quad (24)$$

The detailed scheme of control system is shown in Fig.2a. Under healthy condition i_x^* and i_y* are regulated to zero value. The scheme presented here uses the hysteresis current controllers as they are the simplest solution for the fault tolerant algorithms of multiphase induction motor.

3.2 Modified RFOC under open circuit fault condition

The model of the faulted five phase motor is obtained by calculating the back EMF in the faulted phase of the machine as explained in previous section.

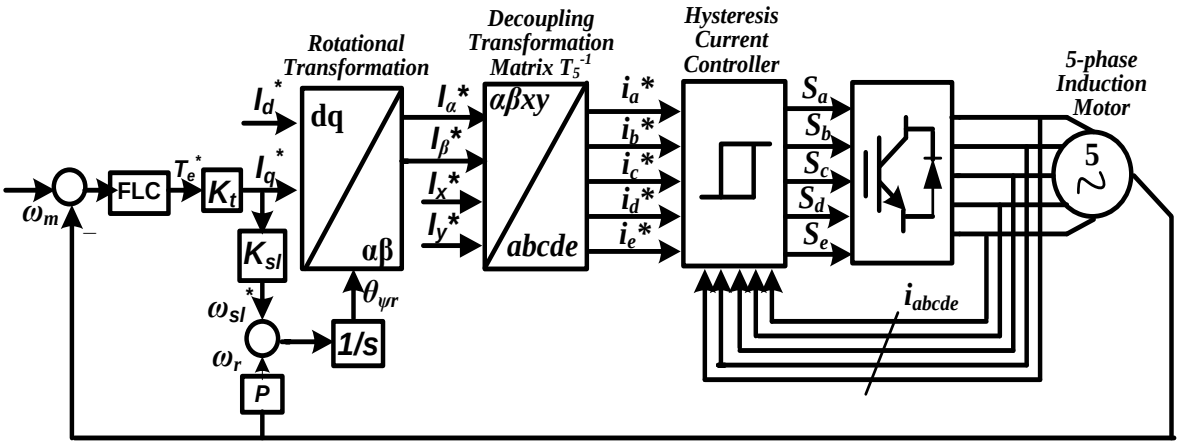

Fig.2a. The complete RFOC scheme for FPIM

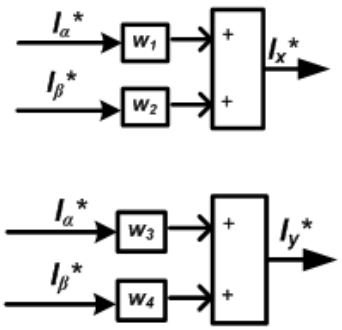

Fig.2b. Reference current generation under fault tolerant mode of operation

The calculated back EMF in faulty phase is applied as an input to realize the fault condition. Under the open circuit fault condition the voltages and so the currents become unbalanced. The magnitude of rest of the phase currents increases to larger than their rated one. This is reflected as additional ripples in the electromagnetic torque generated. The increased torque ripples are not tolerated for the disturbance free running operation of the vehicle. To maintain a smooth post fault operation with no additional torque ripples in the drive, redefinition of reference current is needed, which can maintain a smooth rotating magnetic flux trajectory on α –β plane.

For the star connected FPIM with isolated neutral point zero sequence components remain zero. The non energy i_x and i_y current components can be used to generate proper set of stator phase currents which will compensate for the distortion. This can be achieved by making them dependent on $i_{\alpha s}$ and $i_{\beta s}$ as written in (25):

$$\left.\begin{aligned} i_x &= K_1 i_{\alpha s} + K_2 i_{\beta s} \\ i_y &= K_3 i_{\alpha s} + K_4 i_{\beta s} \end{aligned}\right\} \quad (25)$$

Depending upon the values of weight factors $w_1 - w_4$, different modes of drive operation as minimum torque ripple or maximum efficiency is possible. Therefore the main aim here is to find the values of weight factors. As the number of equations is more than the unknown to be found, the solution of (26) is not unique and therefore there are different $w_1 - w_4$, coefficients are possible that can form circularly rotational magnetic flux trajectory. For the requirement $w_1 - w_4$ are found by considering the minimum torque ripple in the system. The current in faulty phase is zero, which is used to establish a relation between *Iα* and *Ix*. That gives the value of w_1 = -1. For making the analysis easy w_2 =0 is considered. The values of w_3 and w_4 are calculated as -0.2631 and 0 respectively. The corresponding reference current generation is shown in fig.2b.

4. SPEED CONTROLLER DESIGN

4.1 Conventional PI controller for FPIM

The conventional PI controllers are widely used in the industrial application as their parameters are directly associated with the system response specifications. Selection of appropriate parameters influences the speed response, overshoot, settling time and load rejection behavior of the drive. In this paper Ziegler Nichols tuning method is used to obtain the optimized value of proportional and integral gain parameters. However all the required performance characteristics cannot be achieved at the same time using the same parameters [15].

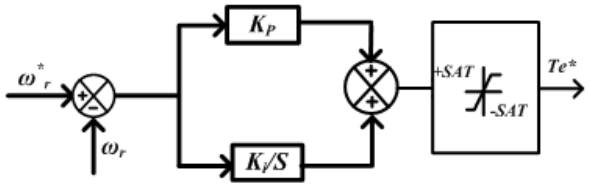

Fig.3. Schematic of PI speed controller

Fig. 3 shows schematic model of the PI speed controller. The controller functioning is explained in (27). The speed error is generated from difference of reference and actual speed command.

$$\left.\begin{aligned} \Delta\omega_r(t) &= \omega_r^*(t) - \omega_r(t) \\ T_e^* &= K_p \Delta\omega_r(t) + K_i \int \Delta\omega_r(t)dt \end{aligned}\right\} \quad (27)$$

The speed error is processed through PI speed controller. The output of PI controller is interpreted reference torque command, which is further applied to limiter as in (28) for final torque command generation. The limiter ensures the output torque and so the current of the inverter remains within the safe range.

$$\begin{bmatrix} i_a^{ref} \\ i_b^{ref} \\ i_c^{ref} \\ i_d^{ref} \\ i_e^{ref} \end{bmatrix} = \begin{bmatrix} 1+w_1 & w_2 \\ 0.3096-0.8080w_1+0.5888w_3 & 0.9509-0.8083w_2+0.5888w_4 \\ -0.8083+0.3066w_1-0.9518w_3 & 0.5888+0.3066w_2-0.9518w_4 \\ -0.8101+0.3127w_1+0.9499w_3 & -0.5862+0.3127w_2+0.9499w_4 \\ 0.3066-0.8120w_1-0.5837w_3 & -0.9518-0.8120w_2-0.5837w_4 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (26)$$

$$T_e^* = \begin{cases} T_{e\max}^* & for T_e^* \geq T_{e\max}^* \\ -T_{e\min}^* & for T_e^* \leq T_{e\min}^* \end{cases} \quad (28)$$

Where, $\Delta\omega_r(t)$ is the error speed, K_p is proportional and K_i is the integral gain constants. T_e^* is the reference torque component, $\omega_r^*(t)$ and $\omega_r(t)$ are the reference speed and actual speed, respectively.

4.2 Fuzzy Logic based controller (FLC) for FPIM

The fuzzy logic based controller is employed to overcome the problem of nonlinearities in the motor model as well as the parameter uncertainties due to exceptional conditions like faults. The inputs to the FLC block comprise of error between the reference speed and actual motor speed (speed error) and change in the speed error. The torque reference current is produced as an output of FLC. The schematic of FLC is shown in Fig.4.

Rewriting the torque balance equation of the motor

$$T_e = J\frac{d\omega_r}{dt} + T_L + B\omega_r \quad (29)$$

By considering the small changes in the electromagnetic toque in the machine, (29) can be rewritten as,

$$\Delta T_e = J\frac{d\Delta\omega_r}{dt} + \Delta T_L + B\Delta\omega_r \quad (30)$$

The above small signal model can be written in the discrete form as shown in (31). Model of small signal in discrete time for the simplified FPIM model with applying constant load expressed as

$$\Delta T_e(n) = J\Delta e(n) + B\Delta\omega_r(n) + \Delta T_L \quad (31)$$

$$T_e(n) = \sum_{n=1}^{N}\Delta T_e(n) = f\left(\Delta\omega_r(n), \Delta e(n)\right) \quad (32)$$

Where, N is the representation of total number of rules in FLC. $\Delta\omega_r(n) = \omega_r^*(n) - \omega_r(n)$ is the speed error. $\Delta e(n) = \Delta\omega_r(n) - \Delta\omega_r(n-1)$ is the change in speed error. $\Delta\omega_r(n)$ and $\Delta\omega_r(n-1)$ are the current and previous samples of speed respectively.

In the fuzzy controller design the derivative block is replaced by the time delay block, so that the calculation burden can be reduced. Also it protects the controller from the uncertainties like spikes in the output. The entire fuzzy logic controller is divided in mainly three different subsystems as fuzzification, fuzzy rule based decision making and defuzzificaiton as shown in fig. 4. The details are explained as under.

Fuzzification Process: A linguistic variables based FLC requires the conversion of its numerical inputs (word,crips set) to its variable form (linguistics) by Fuzzifier. The inputs of FLC speed error $\Delta\omega_r$ and error gradient Δe are normalized by factors named as $K\omega$, Ke so they are in an acceptable range of -1 to 1. The gain factor Kq for the output signal is determined in such a way that the output of the FLC can generate required reference torque component at various operating points. The optimum performance of FLC is based on proper selection of normalization factors. In this paper, these parameters are assumed constants. They are selected by trial and error method. The optimal drive simulations performance is determined by adopting the normalization factors $K\omega$ = 0.0063, Ke=0.064 and gain factor is Kq = 150.

Membership Function (Mf): The MFs of $\Delta\omega_r$, Δe, and Te are selected based on scaling parameters. The MFs should cover the universe of discourse overlapping with each other. The overlapping avoids discontinuity during the minor changes of inputs. A finer control is achieved with a narrow band of MFs near the zero regions. The wider band of MFs away from the zero region results in faster system response.

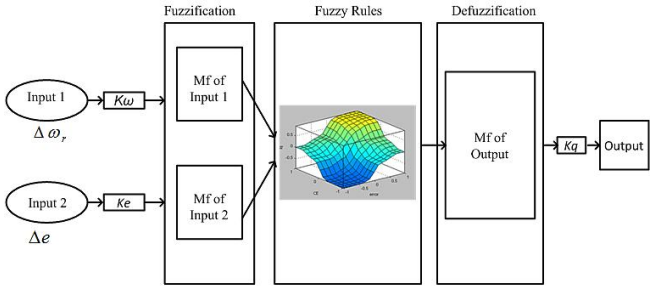

Fig. 4. Schematic of the Fuzzy logic controller

Fig. 5 shows the Degree of membership functions (DOM) used for the input and output fuzzy inputs. This paper adopts triangular and trapezoidal MFs for the fuzzy inputs and output due to their ease of mathematical implementation. In this paper seven MFs are considered for both the inputs and eleven MF for output so that the finer response under all operating conditions is possible. The Mfs are symmetrically distributed along the horizontal axis. They are tuned for the different operating conditions of system.

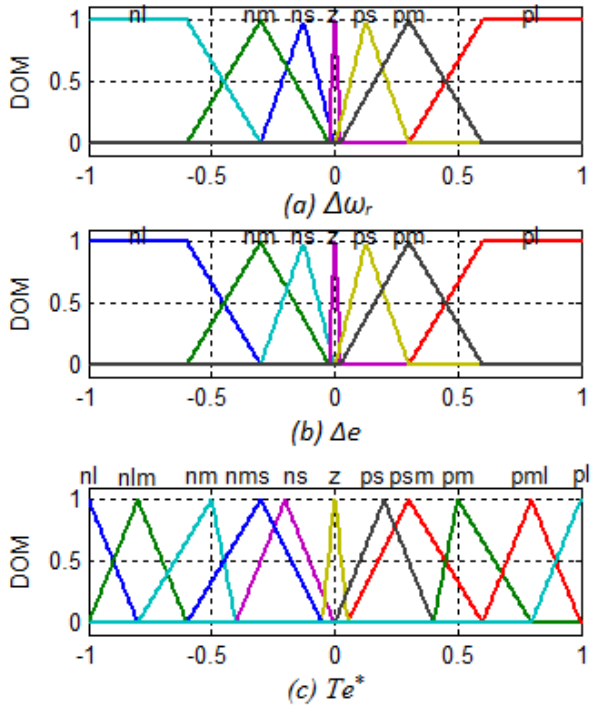

Fig.5. Degree of Membership Functions for (a) speed error '$\Delta\omega r$', (b) change in error Δe, (c) reference output 'Te^*'

They are nl (negative large-1), nlm (negative large medium-2), nm (negative medium-3), nms (negative medium small-4), ns (negative small-5), Z (Zero-6), ps (positive small-7), psm (positive small medium-8), pm (positive medium-9), pml (positive medium large-10), pl(positive large-11). The triangular membership functions are employed so that the burden of real time implementation can be reduced.

Knowledge Rule Based Process: The proposed fuzzy base rule table for five phase IM is shown in Table 1. The rules chosen are based on the IF AND- THEN logic. As indicated before the fuzzy set matrix is written for the variables '$\Delta\omega_r$' and 'Δe' respectively, and the Mfs of the output variable 'Te*' are shown in the body of the matrix. Total 49 rules are written. The corresponding surface view is shown in fig. 6.

Inference and Defuzzification: Fuzzy inference utilizes FL operators to map the function between input and output. The two basic methods of fuzzy inference are Mamdani and Sugeno. This work is based on Mamdani min-max method of fuzzification and method of centroid is chosen for defuzzifiation.

Table 1. Fuzzy rule table for speed controller output

Output (Te^*)		Speed Error ($\Delta\omega_r$)						
		1	**3**	**5**	**6**	**7**	**9**	**11**
Error gradient (Δe)	**1**	1	1	2	3	4	5	6
	3	1	2	3	4	5	6	7
	5	2	3	4	5	6	7	8
	6	3	6	5	6	7	8	9
	7	4	5	6	7	8	9	10
	9	5	6	7	8	9	10	11
	11	6	7	8	9	10	11	11

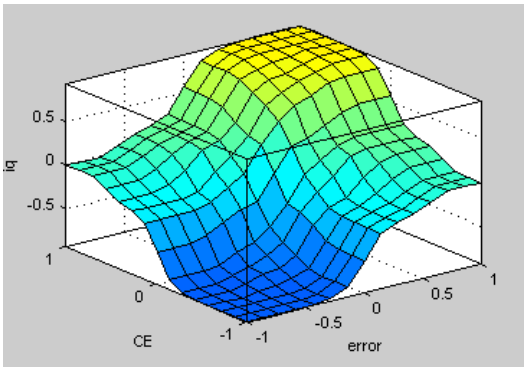

Fig.6. Surface view of FLC rules

5. RESULTS AND DISCUSSION

The model of 2 HP star connected five phase induction motor having rated torque of 8.33 Nm following parameters shown in table 2 is developed in MATLAB/Simulink for testing purpose.

Table 2. Motor Parameters

S=2 HP	*Vph= 220V*	*Iph=2.1 A*	*f*=50Hz
R_s=10Ω	R_r=6.3Ω	L_s=0.46H	L_r=0.46H
L_m=0.42H	*B*=0.008	*J*=0.03	*P=2*

Initially the FPIM drive performance is tested for both the controllers under healthy condition.

4.1 Controller performance under Prefault healthy mode of operation

The motor performance is observed for three different test groups: First is an acceleration performance or free characteristics. Next performance is tested under step speed response. The third test conditions are trapezoidal speed with step change in load torque.

1) Motor starting performance at 140 rad/s under noload torque condition

Initially the performance of the five phase induction motor is observed under no load torque condition. The FPIM is applied reference speed of 140rad/s. At starting, due to the motor develops the accelerating torque of 20 Nm with high amplitude to stator current (±5A) to attain the set speed of 140 rad/s. From the fig.(7) (i), it is understood that with PI speed controller the motor speed tracks the reference speed in 0.32 sec, but in the case of fuzzy FLC it takes 0.28 sec. The steady state error in FLC is neglected, whereas in case of PI it is observed to be 0.72%. Corresponding electromagnetic torque generated using both the controller and the phase 'a' current is shown in fig. 7 (ii) and (iii) respectively.

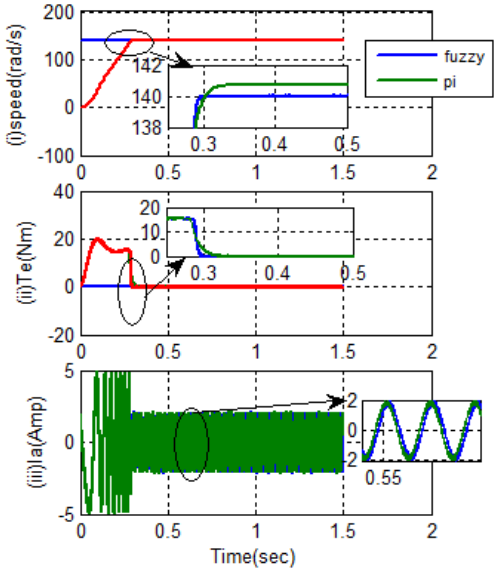

Fig.7. Motor starting performance at no load torque applied with FLC and PIC (i) speed, (ii) Torque, (iii) Phase 'a' current(blue-fuzzy, Green-PI)

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2) Motor performance at step change in speed at noload torque

Motor speed is changed from 140 rad/s to 30 rad/s at 1.5 sec and response is observed under no load torque applied. From It can be observed from fig.8(a) that the FLC settles to the reference speed after 0.05 sec from the application of sudden speed change with 0% overshoot, where as PI controller takes 0.5 sec to settle to the new speed reference with 33% undershoot(red corresponds to FLC and Green corresponds to PI). From the Fig. 8 (b) shows the results corresponding to speed change from 140rad/s to 157 rad/s. In speed response FLC settles after 0.02 sec with no overshoot, whereas PI controller takes 0.2 sec to settle with 10% overshoot.

3) Motor performance under trapezoidal speed command with application of step load torque

The motor is applied the trapezoidal speed command to realize the electric vehicle performance. Where initially vehicle is accelerated to rated speed, then the vehicle running with constant speed and last part is the deceleration of the vehicle. To realize this, the motor is applied accelerated reference speed from 0rad/s to 157 rad/s in 1.5 sec. then motor run with constant speed upto 3 sec and then motor decelerates to stand still speed in 1.5 sec. the step load torque of 8 Nm is applied at 1.5 sec and removed at 2.5 sec. Corresponding results are plotted in fig. 9.

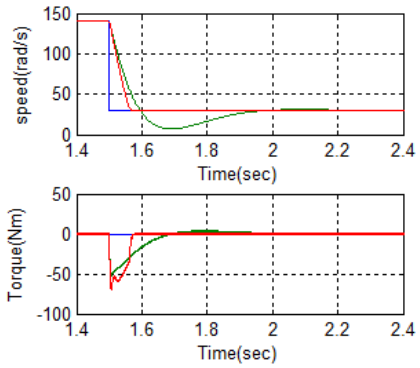

Fig.8. (a) Speed change from 140rad/s to 30 rad/s

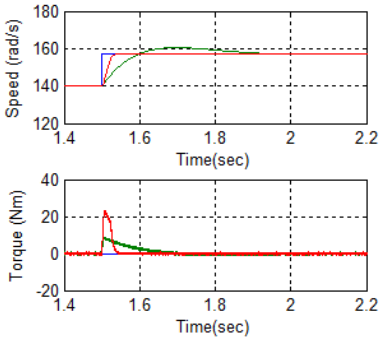

Fig.8. (b) Speed change from 140 rad/s to 157 rad/s

Fig. 8. Motor performance at step change in speed at noload torque

Figure 9(a) and (b) shows the motor speed and torque response with PI controller respectively. It can be observed that the controller follows the reference speed. At the application of load undershoot of 4% is observed and 3.18 % of overshoot is observed at time of removal of load. The settling time is Figure 9(c) and (d) shows the speed and torque response for FLC controller. There is no overshoot or under shoot is found under application or removal of load torque. Steady state error is found zero in case of both the controllers.

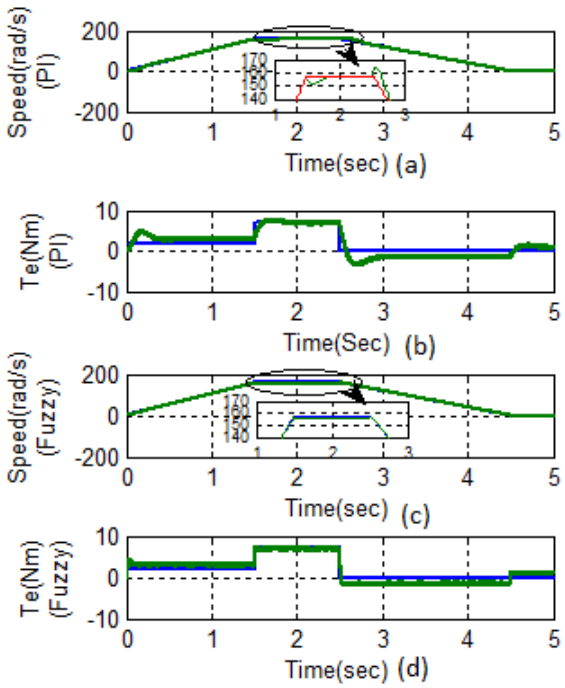

Fig.9. Speed and torque curves for trapezoidal speed reference and square load torque T_L=8 Nm (Blue-fuzzy, Green-PI)

4.2 Controller performance under Post fault mode of operation

The controller performance is now tested under the open circuit fault condition. The fault is created at a time of 4 sec with no load torque applied to the motor. The method of back emf in the fault phase is employed to model the fault as discussed in section II. The corresponding results are plotted in Fig. 10. As expected, after the occurrence of fault at 4 secs, the current in faulty phase 'a' is zero (blue line in fig. 10(iii) and (iv)). The system behaviour is tested under open circuit fault with 6 Nm of load applied on the motor. The reference speed is set to 157 r/s. The corresponding results are plotted in fig. 10.

Fig.10 (i) shows the speed response after the occurrence of fault at 4 sec. In speed response with PI controller the undershoot of 7.6% is observed at the fault application. It takes 1.2 sec for speed to get stabilize, where as there is no overshoot for the speed response with FLC. Fig.10 (ii) shows the corresponding torque variation in the motor. The

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torque ripple increases with both the controller but the in case of the FLC controller uniform rise of torque oscillation is observed as compared to that with PI controller. Fig. 10(iii) and (iv) show the corresponding five phase motor currents under fault condition. It is seen that the distortion in remaining four currents in case of FLC is less as compared to PI controller.

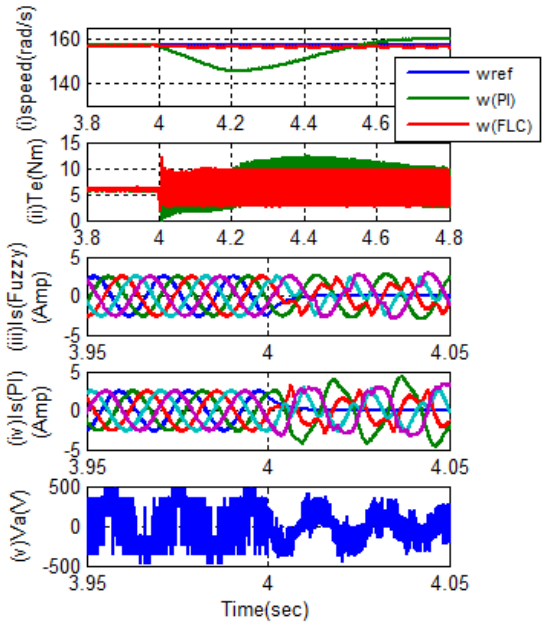

Fig. 10. Motor dynamics under post fault mode of operation (i)Speed (ii) Torque (iii)Five phase stator current with Fuzzy controller (iv)Five phase stator current with PI controller (v)Motor phase 'a' voltage

4.3 Controller performance under fault tolerant mode of operation

Now the fault tolerant strategy is applied at 2 sec after the occurrence of fault it means that at 6 sec. the motor behaviour is tested under 6 Nm of load torque. The d axis and q axis current are manipulated to get the circular trajectory. For the requirement $w_1 - w_4$ are found by considering the min torque ripple in the system as discussed in section III. Corresponding results are shown in fig.11.

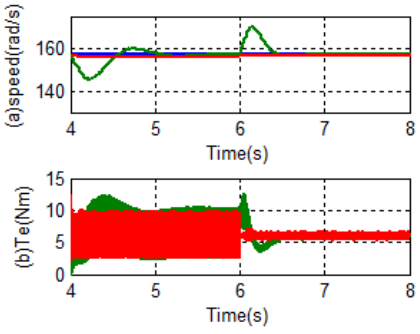

Fig. 11. Controller response under fault tolerant operation (a) speed response, (b) torque response

Fig. 11 (a) and (b) show speed and torque response after fault tolerant strategy respectively for PI and FLC (Red – Fuzzy, Green - PI). Fig. 11 (a) illustrates the speed behaviour of motor under PI and FLC. With the application of PI controller overshoot of 8.3% is observed in the speed response where as with fuzzy logic controller no overshoot is observed. The torque ripples reduces to significant level by applying the fault tolerant strategy with both the controllers. Before stabilizing to a lower ripple torque an overshoot of 16 % and under shoot of 10% is observed from the fig.11 (b).

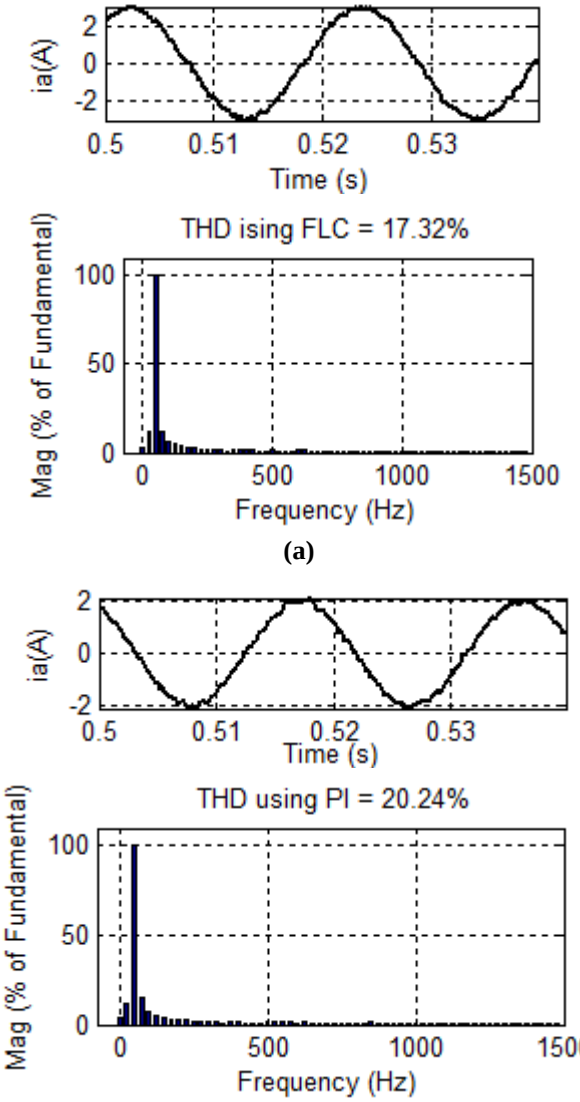

Fig. 12. FFT analysis of phase 'a' current under steady state (a) with PI controller, (b) with FLC

Fig. 12 (a) shows the simulation study of phase-*a* current in steady state and its THD at speed of 140 rad/s under rated load conditions using a PI controller with an five phase Hysteresis current controlled (FPHCC) inverter-

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fed FPIM drive. The Fig. 12 (b) shows the simulation study of steady-state phase-*a* current and its THD using an FLC at the same test conditions. It is observed that the motor phase-*a* current in steady state and its THD of the proposed FLC with the (FPHCC) inverter-fed FPIM drive has less THD compared with the traditional PI controller.

CONCLUSION

In this paper, a robust fuzzy logic based speed controller for five phase induction motor is proposed which works equally well under healthy and faulty condition. The effectiveness of controller is validated through different time response comparison under healthy and open circuit fault operation of the five phase induction motor. From the results obtained it is clear that the PI controller provides satisfactory performance under steady state condition but its response is poor under dynamic condition as well as fault condition. The nonlinear fuzzy logic based controller tracks the reference well and improved performance is obtained than the conventional PI controller under healthy and faulty condition. The application of proposed controller is highly suitable for high performance and reliable electric vehicle drive.

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A Walkthrough of Digital Forensics and its Tools

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Abstract:

The accelerated pace in technological advances and pervasive usage of digital assets has manifested the value of Digital Forensics. The operations of global phenomena are confronting a risk of exposure and threats from cyber penetrators as they are posing challenges towards everyone through anti-forensic techniques. This requires effective process and specialized digital forensics tools to acquire digital evidences to serve as an aid to justice. This paper provides a brief on digital forensics process, its evaluation metrics, and proposes a taxonomy of digital forensics tools which provides a detailed overview and comparison among different forensics tools based on different features in their categories. Furthermore, we identified several indispensable challenges in this fascinated area.

Keywords:

Digital Evidence, Digital Forensics, Digital Forensics Tools, Information Security

1. INTRODUCTION

The technical advances in digital technology has brought advantages to the mankind as the evolution has greatly contributed in providing smooth conduct of business, comfortable life and streamlined processes which has automated thanks to such advances. Consequently, the technical development comes at the cost of breach in security of information stored or exchanged digitally. The dramatic rise in digital technology gives rise to new avenues for digital penetrators to devise new and sophisticated attack methods in order to bypass security defense, trap the victim and breach the security setups. Across the globe, digital attacks performed by these determined cyber penetrators have impacted huge masses and nagged billions of dollars [1]. Almost every corporate and organization is spending huge amount in safeguarding their digital assets and to avoid being victim of the attacks. The emergence of digital crimes and dependence on technology has lead to the development of Digital Forensics which acts as an armor in this battlefield. The intervention of Digital Forensics is paramount as the forensic process and multitude of tools provided a streamlined manner to extract evidence and provides a way to combat and protect from numerous cyber crimes [2]. The more agile and automated forensic process gives us the tools we require to investigate the extracted evidence to make it admissible to the court. The data storage platforms varies from computers, IoT, database, email, network, mobile, memory and cloud and for the better extraction and investigation of these storage platforms different tools are needed. To serve this purpose we proposed a taxonomy of digital forensics and further extending this we described in detail each category in the taxonomy [54-58].

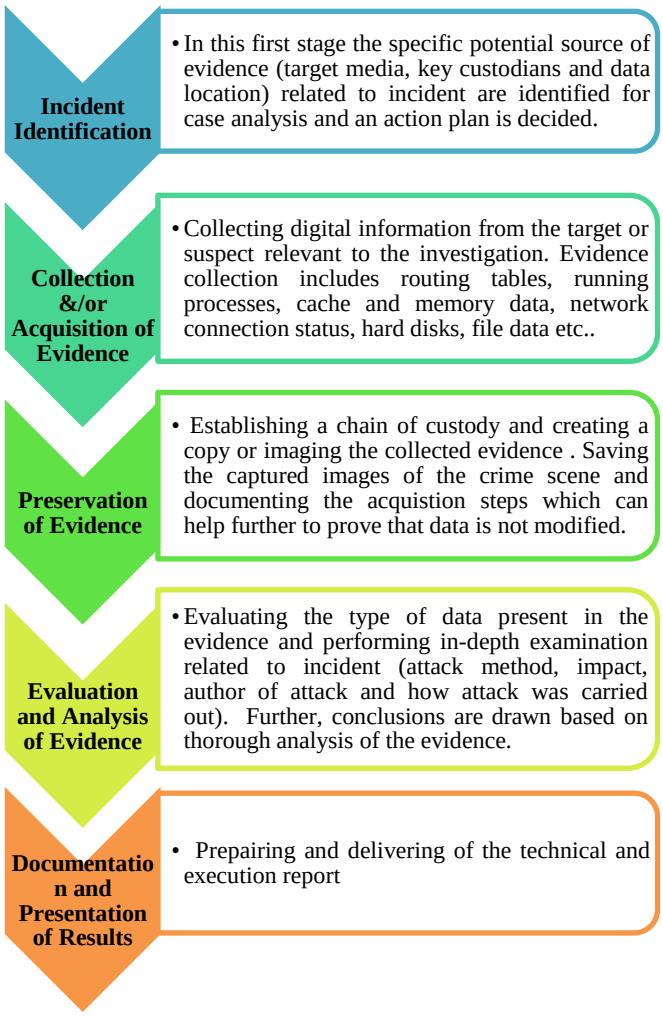

Fig. 1. Digital Forensic Process

2. EVALUATION METRICS FOR DIGITAL FORENSICS TOOLS

For validation of forensics tools it is important to assess them based on the evaluation metrics which can help community to select the tool with no bias and can help the vendors knowing the scope of improvement. These evaluation metrics cover all properties that can help in judging the capacity of the tool [3].

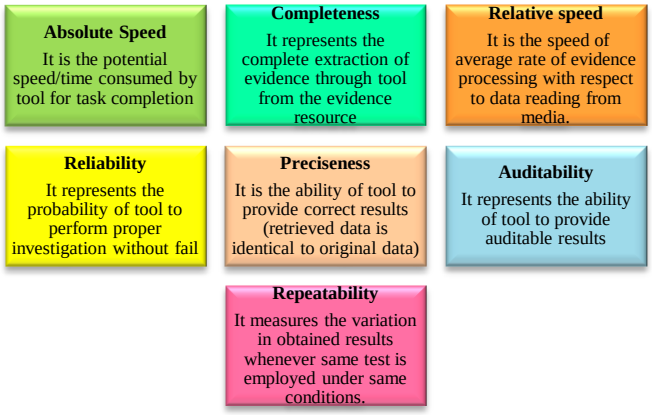

Fig. 2. Seven Evaluation Metrics for Digital Forensics Tools

3. DIGITAL FORENSICS TOOLS CHALLENGES

- Encryption
- Volume of Investigation data
- Evidence Size and its volatility
- Remarkable growth and sophistication in digital crimes
- Legal Issues (Jurisdiction, Privacy, Legal Process, Acceptability of forensics tools and mechanisms)
- Proliferation in digital media types and their life span
- Anti Digital Forensics
- Scarcity of Resources
- Emerging technologies, applications and devices
- Shortage of trained and certified personnel
- Incompatibility or automation absence among varied forensics tools
- Ethical Issues
- Trust in the Audit Process
- Manual Interventions
- Lack of Standardization
- Testing and Validation
- Malicious Programs

4. TAXONOMY OF DIGITAL FORENSICS

A Taxonomy of Digital Forensics is highlighted through Figure 3 and detailed explanation of different types of Digital forensics is provided in following sub-sections where ✓ means supported feature, × means non-supported, W stands for Windows, M stands for MAC OS, L stands for Linux, A stands for Android, I stands for iOS, BB stands for BlackBerry and U stands for Unix.

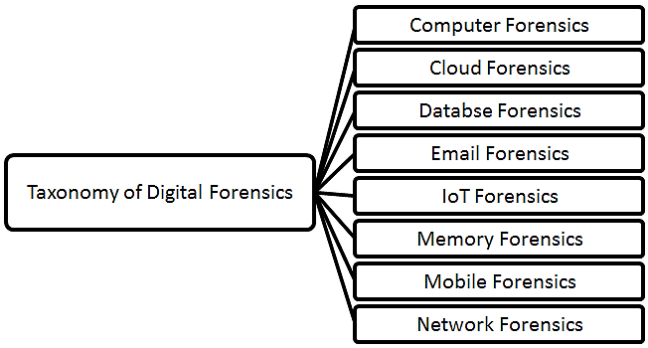

Fig. 3. Taxonomy of Digital Forensics

4.1 Computer Forensics and its Tools

Computer forensics is a vital form of digital forensics which investigates the evidential information extracted from computing devices, networks, storage elements and wireless communication and later analyzes it and preserves it for making it admissible in the court. The investigation is aimed towards collection of latent data. The tools are used to extract deleted data, password cracking, keyword searches, evaluation of windows registry and physical file data construction. The tools used for performing Computer Forensics with their features are highlighted in Table 1.

Table 1. Computer Forensics Tools

Features/Tool	Internet Evidence Finder [4]	X-Way Forensics [5]	FTK Imager [6]	EnCase [7]	The Sleuth Kit [8]	Helix [9]	Live View [10]
Identifying threats	✓	✓	✓	✓	✓	✓	×
User-friendly GUI	✓	✓	✓	✓	✓	×	✓
Protocols support like HTTP/POP	×	×	×	✓	✓	✓	×
Decryption for password recovery	✓	✓	✓	✓	✓	✓	✓
Data visualization	✓	✓	✓	✓	✓	✓	✓
Hash databases	✓	✓	✓	✓	✓	×	×
Supported Platforms	W/M	W	W	L	W /L	W /L	W /L

4.2 Cloud Forensics Tools

Cloud Forensics Tools perform investigation on Cloud i.e. forensic acquisition of cloud. The tools perform data acquisition only on the area where some false action has been performed (to collect evidence against attacker) as data on cloud is stored in logical pools which spans multiple servers containing vast and humongous amount of data. The tools can extract data from API logs, virtual disks, guest firewall logs, private social media accounts, mails, user location, etc. The tools used for performing Cloud Forensics with their features are highlighted in Table 2.

Table 2. Cloud Forensics Tools

Features/Tools	FROST [11]	UFED Cloud Analyzer[12]
Extraction of data from OpenStack cloud	✓	×
Compatibility with forensic formats	✓	✓
Infrastructure-as-a-Service (IaaS)	✓	×
Data sharing	✓	✓
Supported Platform	W	W

4.3 Database Forensics Tools

Database Forensics tools involve extraction and investigation of databases and their related metadata, where the tools after a critical failure/attack inspect changes in hard disk, perform kernel recovery (lost tables, stored procedures, quick scan, tracing of files, views and keys). The tools can recover deleted, damaged and hidden data. In addition to this, file comparing, disk cloning, file encryption and checksum creation are some of the features provided by these tools. The tools used for performing Database Forensics with their features are highlighted in Table 3.

Table 3. Database Forensics Tools

Features/Tools	IDEA[13]	ACL Audit exchange [14]	Arbutus[15]	SQL CMD [16]	Windows Forensic Toolchest [17]	Systools SQL Log Analyzer [18]
Data analysis	✓	✓	✓	✓	✓	✓
Visualization of data	✓	✓	✓	×	✓	×
Read only access	✓	✓	✓	✓	✓	✓
Audits	✓	✓	✓	×	✓	✓
SQL support	✓	✓	✓	✓	✓	✓
Supported platforms	W	W	W	W	W	W

4.4 Email Forensics Tools

Email forensics tools offer diverse and detailed information related to source and content of Email. To investigate the attacker's intent behind the attack, these tools helps in tracing the path followed by the email, its source and destination, sent and receipt date and time, transaction details, and are able to locate the phishing and spam networks. To extract the aforesaid information there is a need to perform header analysis, bait tactics, keyword searching, port scanning, sender mailer fingerprint identification etc. The tools used for performing Email Forensics with their features are highlighted in Table 4.

Table 4. Email Forensics Tools

Features/Tools	MailXaminer [19]	eMailTracker Pro [20]	Email Tracer [21]	Adcomplain [22]	Add4Mail Forensic [23]	Abuse Pipe [24]	FinaleMail [25]	Paraben (Network) E-mail Examiner[26]	Forensics Investigation Toolkit (FIT) [27]
Analysis and investigation of e-mails	✓	✓	✓	✓	✓	✓	✓	✓	✓
Abuse Reporting	×	✓	×	✓	✓	✓	×	✓	×
Spam filter	✓	✓	×	✓	✓	✓	×	✓	×
Recovery of lost e-mails and databases	✓	×	✓	×	✓	×	✓	✓	✓
Boolean searching	✓	×	✓	×	✓	×	×	✓	✓
Export format	✓	✓	✓	✓	✓	✓	×	✓	✓

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support									
Visualisation support	✓	✓	×	×	×	✓	✓	×	✓
Platforms supported	W/M	W	Content analysis	U/W	L/W/M	W/M/U	W/L	W	W

4.5 IoT Forensics Tools

The IoT forensics tools involves investigation of vast real time data collected from crime scene which involves variety of smart and communication capable IoT devices such as home appliances, embedded systems, mobile devices, sensors, etc. The area of region covered by these devices in the crime scene could be LAN, MAN, WAN or PAN. These tools after context establishment perform data, file and images extraction which is further followed by its investigation, analysis and reporting. The tools used for performing IoT Forensics with their features are highlighted in Table 5.

Table 5. IoT Forensics Tools

Features/Tools	Bulk Extractor [28]	CAINE [29]	NUIX [30]	RegRipper [31]	Pajek64 [32]
Scanning and extraction of information	✓	✓	✓	✓	×
Analysis of forensic images, data and files	✓	✓	✓	✓	✓
GUI Support	✓	×	✓	×	✓
Windows registry files	×	×	✓	✓	×
Supported Platforms	W/L/M	L/W/ U	W/ M/ L	W/ L	W/ M

4.6 Memory Forensics Tools

Memory Forensics Tools involves investigation of current status of system's memory/memory dump. The memory dump is captured (volatile information) to form a real time image of the system which is later analyzed for investigation. This file contains information about running processes, running exe files, file related information, logged in users, network related information, user activity, timestamp comparison and decoded applications in memory. For live acquisition Process Hacker, Helix ISO etc. tools can be used. The tools used for performing Memory Forensics with their features are highlighted in Table 6.

Table 6. Memory Forensics Tools

Features/Tools	Memoryze [33]	Belkasoft RAM Capturer [34]	Volatility Suite [35]	Windows SCOPE [36]	Rekall [37]
Live Acquisition	✓	✓	✓	✓	✓
Memory Image acquisition	✓	×	✓	✓	✓
Find Physical Address	×	×	✓	✓	×
Find Virtual Address	✓	×	✓	✓	×
Running Processes	✓	×	✓	✓	×
Malware detection	×	✓	✓	×	×
GUI Support	×	×	×	✓	✓
Command Line Support	✓	✓	✓	×	×
Paging file Inclusion	✓	×	×	×	×
Reporting device and driver layering	✓	×	×	×	×
Verify digital signature	✓	×	×	×	×
Images full system memory	✓	×	✓	✓	✓
Enumerating Running Processes	✓	×	✓	✓	×
Listing Network Sockets	✓	×	✓	✓	×
Bypass Active Anti-Debugging and Anti-Dumping Protection	×	✓	×	×	×
Analyze rootkits	✓	×	✓	×	×
Supported Platform	W	W	W/ L/ M/A	W	W

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4.7 Mobile Forensics Tools

Mobile Forensics deals with the potential recovery of digital evidence from different sources of mobile device (mobile phones, PDAs, GPS devices, Tablets) such as SIM card, SD card and Handset memory. The forensic process of a mobile device involves following stages: seizure, identification, acquisition, examination and reporting. The evidences such as contact list, messages (SMS and MMS), photos, videos, emails, notes, location information, social networking sites related and web browsing information are acquired using any of the data acquisition technique such as physical, manual, brute force and logical. The tools used for performing Memory Forensics with their features are highlighted in Table 7.

Table 7. Memory Forensics Tools

Features/Tools	MOBILed It Forensic Express [38]	Cellebrite UFED Ultimate [39]	Paraben E3:DS Mobile Forensic [40]	Secure View APEX [41]	Micro Systemation XRY/XACT [42]	Oxygen Forensic Suite [43]
Screen Lock Disabler	✓	✓	✓	✓	✓	✓
Password and PIN breaker	✓	✓	✓	×	✓	✓
Data Reports	✓	✓	✓	✓	✓	✓
Call Logs	✓	✓	✓	✓	✓	✓
Messages	✓	✓	✓	✓	✓	✓
User Data	✓	✓	✓	✓	✓	✓
Application Data	✓	✓	✓	✓	✓	✓
Internet Data	✓	✓	×	×	✓	×
Social Networking Data	✓	✓	`×	×	✓	✓
GPS data	✓	✓	✓	×	✓	✓
Drone Data	×	✓	✓	×	✓	✓
Cloud Data	✓	✓	✓	×	✓	✓
Keyword Search	✓	✓	✓	✓	✓	✓
IoT device support	×	×	✓	✓	×	✓
Organizer	✓	×	×	×	×	✓
Deleted data Recovery	✓	✓	×	✓	✓	✓
Logical Acquisition	✓	✓	✓	×	✓	✓
Physical Acquisition	✓	✓	✓	✓	✓	×
Hex Viewer	×	✓	✓	×	✓	✓
SQLite Databases	✓	✓	✓	✓	×	✓
GUI Support	✓	✓	✓	✓	✓	✓
Command Line support	×	×	×	×	×	×
Organizer	✓	✓	×	×	✓	✓
Timeline Support	✓	✓	✓	×	×	✓
Live Data Extraction	×	✓	✓	×	✓	✓
Backup and Image import	✓	✓	✓	×	✓	✓
Malware detection	✓	×	✓	×	×	✓
Supported Platform	W	i/A	A/i/ BB/ W	i	A/i	A/ W/ BB/ i, S

4.8 Network Forensics Tools

Network forensics is a new area in Digital Forensics that discovers, monitors and analyzes the network traffic and its events for gathering information, tracking communication, identifying intrusions, anomalous behavior in traffic and source of attack. This pro-active investigation is performed either standalone or along with computer forensics process. The harvested information from the suspected network traffic needs to follow legal and technical aspects as well as general forensic aspects. The tools used for performing Network Forensics with their features are highlighted in Table 8.

Table 8. Network Forensics Tools

Features/Tools	Network Miner [44]	Wireshark [45]	Security Onion [46]	Net VCR [47]	Xplico [48]	Omni Peek [49]	NIKSUN Netdetector [50]	Stenographer [51]	DSHELL [52]	Password Sniffer Console [53]
Intrusion detection	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Network Security monitoring	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Log management	✓	×	✓	✓	✓	✓	✓	×	×	✓
Offline analysis	✓	✓	✓	✓	✓	✓	✓	×	×	✓
Display Filters	✓	✓	✓	✓	×	✓	✓	×	×	×
GUI based	✓	✓	✓	✓	✓	✓	✓	✓	×	✓
Command Line based	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Full packet capture using WinPcap	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
IPv4 and IPv6 support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
VoIP call extraction	✓	✓	✓	✓	✓	✓	✓	×	×	✓
HTTP content extraction	✓	✓	✓	✓	✓	✓	✓	×	✓	✓
FTP login extraction	✓	✓	✓	✓	✓	✓	✓	×	×	✓
Web login extraction	✓	✓	✓	✓	✓	✓	×	×	✓	✓
Email extraction	✓	✓	✓	×	✓	✓	✓	×	×	✓
Supported Platform	W/L/M	W/L/M/U	L	W/L/U	L/W	W	W/L	W/L/U	L	W

5. CONCLUSION

The dramatic rise in digital technology gives rise to new avenues for digital penetrators to devise new and sophisticated attack methods in order to bypass security defense, trap the victim and breach the security setups. Across the globe, digital attacks performed by these determined cyber penetrators have impacted huge masses and nagged billions of dollars. The emergence of digital crimes and dependence on technology has lead to the development of Digital Forensics which acts as an armor in this battlefield. This paper provides a brief on digital forensics process, its evaluation metrics, and proposes a taxonomy of digital forensics tools which provides a detailed overview and comparison among different forensics tools based on different features in their categories. Furthermore, we identified several indispensable challenges in this fascinated area.

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ℓ −Hypergeometric Functions on Harmonic Univalent Functions

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Abstract:

In this paper, we study certain harmonic univalent mappings involving the l-Hypergeometric functions. We establish the characteristics connected with harmonic mappings and mention their sufficient conditions.

Keywords:

Analytic function, Univalent function, Convolution operator, Harmonic function, ℓ-Hypergeometric function, Simply-connected domain, Unit disk

1. INTRODUCTION

Let $\mathbb{C}$ be a complex plan and $\mathfrak{D}$ be a simply connected domain on it. Let u and v be real-valued harmonic functions in $\mathfrak{D}$, then we call $f = u + iv$ is a complex valued harmonic function in $\mathfrak{D}$. If $f = h + \overline{g}$, then $|g'(z)| < |h'(z)|$ is the sufficient condition for f to be locally univalent and sense-preserving in $\mathfrak{D}$. Let $\mathcal{A}(\mathbb{D}_1(0))$ be the class of analytic functions in the open unit disk $\mathbb{D}_1(0) = \{z \in \mathbb{C}: |z| < 1\}$. Let $\mathcal{C}$ be the class of all functions $f \in \mathcal{A}(\mathbb{D}_1(0))$ which are normalized by $f(0) = 0$ and $f'(0) = 1$ and have the form

$f(z) = z + \sum_{n=2}^{\infty} \alpha_n z^n, \quad z \in \mathbb{D}_1(0).$ (1)

In 1984, Clunie and Sheil-small [8] introduced a class $\mathcal{SH}$ of complex-valued harmonic maps f which are univalent and sense-preserving in $\mathcal{C}$. So, for $f = h + \overline{g}$, it can be expressed in the analytic functions h and g as

$$h(z) = z + \sum_{n=2}^{\infty} \alpha_n z^n,$$

$g(z) = \sum_{n=1}^{\infty} \beta_n z^n, |\beta_1| < 1.$ (2)

Let $\mathcal{S}$ be the class of normalized analytic univalent functions. Then $\mathcal{SH}$ reduces to the class $\mathcal{S}$ if the co-analytic part of its member is zero. Therefore, the function $f(z)$ ifor the class $\mathcal{SH}$ may be written as (1).

Also, let $\mathcal{NH}$ be the subclass of $\mathcal{SH}$ which consists functions of the form $f = h + \overline{g}$, such that(see [12]),

$$g(z) = -\sum_{n=1}^{\infty} |\beta_n| z^n,$$

$h(z) = z - \sum_{n=2}^{\infty} |\alpha_n| z^n, |\beta_1| < 1.$ (3)

Let $\mathcal{H}(a, b), (a \geq 0, 0 \leq b < 1)$ be the subclass of harmonic functions of the form (2) which satisfies(see [12]),

$$\mathcal{Re}\{(h'(z) + g'(z)) + 3az(h''(z) + g''(z)) + az^2(h'''(z) + g'''(z))\} > b. \quad (4)$$

Also, in [12] authors defined, the class $\mathcal{NH}(a, b)$ by

$$\mathcal{NH}(a, b) = \mathcal{NH} \cap \mathcal{H}(a, b).$$

Hypergeometric functions on Harmonic functions plays an important part in geometric function theory. In 2004, Ahuja and Silverman [1] studied the relationship between distinct hypergeometric functions and harmonic univalent functions. Later, in 2007, Ahuja [2] further investigated by applying certain planar harmonic convolution operators on various subclasses, the connections between the theory of harmonic mappings in the plane and hypergeometric functions. There are many other important studies in this connection, see [3, 4, 5, 6, 9, 10, 11].

In this paper, we study harmonic univalent functions associated with ℓ-Hypergeometric function(in short, ℓ–H function). For $z \in \mathbb{C}$, the ℓ–H function is defined as

$$H\begin{bmatrix}\alpha; \\ \beta; (\gamma: \ell)\end{bmatrix} z = \sum_{n=0}^{\infty} \frac{(\alpha)_n}{(\beta)_n (\gamma)_n^{\ell n}} \frac{z^n}{n!}, \quad (5)$$

where $\ell, \alpha \in \mathbb{C}$ with $\mathcal{Re}(\ell) \geq 0$, $\beta, \gamma \in \mathbb{C} \setminus \{0, -1, -2, \cdots\}$ and $(c)_n = \frac{\Gamma(c+n)}{\Gamma(c)}$. If we put $\ell = 0$ in (5), then ℓ-H function turns to well known confluent hypergeometric function,

$$H\begin{bmatrix}\alpha; \\ \beta; (\gamma: 0)\end{bmatrix} z = {}_1F_1\begin{bmatrix}\alpha; \\ \beta;\end{bmatrix} z. \quad (6)$$

The ℓ-H function (5) recently studied by M. H. Chudasama and B. I. Dave [7].

Next, let $\mathcal{H}(z) = \mathcal{H}_1(z) + \overline{\mathcal{H}_2(z)}$, in which

$$\begin{aligned} \mathcal{H}_1(z) &= zH\begin{bmatrix}\alpha_1; \\ \beta_1; (c: \ell_1)\end{bmatrix} z \\ &= z + \sum_{n=2}^{\infty} \frac{(\alpha_1)_{n-1}}{(n-1)!(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} z^n, \end{aligned} \quad (7)$$

$$\begin{aligned} \mathcal{H}_2(z) &= H\begin{bmatrix}\alpha_2; \\ \beta_2; (c: \ell_2)\end{bmatrix} z - 1 \\ &= \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{n!(\beta_2)_n (\gamma_2)_n^{\ell_2 n}} z^n. \end{aligned} \quad (8)$$

We organize the paper in the following way. In Section 2, we provide some definitions and lemmas which are useful in our main results. In section 3, we derive the

necessary and sufficient conditions for harmonic functions connected with ℓ-H functions to be in the classes $\mathcal{H}(a,b)$ and in $\mathcal{NH}(a,b)$.

2. PRELIMINARIES

In this section we present few definitions and lemmas which are useful in the sequel.

Lemma 1. [[7]] The ℓ-Hypergoemetric function is an entire function of z, provided $\mathcal{R}e(\ell) \geq 0$ and $\mathcal{R}e\left(c\,\ell - \frac{\ell}{2} + 1\right) > 0$.

Definition 2. [[7]] Let $f(z) = \sum_{n=1}^{\infty} a_n z^n$, $z \in \mathbb{C}\backslash\{0\}$, $k \in \mathbb{N} \cup \{0\}$ and $p \in \mathbb{C}$. Define

$$ {}_k\Delta_p^{\mathcal{D}} f(z) = \begin{cases} \sum_{n=1}^{\infty} a_n (p)_{n-1}^{k} (\mathcal{D}+p-1)^{kn} z^n, k \in \mathbb{N}, \\ f(z), k = 0, \end{cases} $$

where $\mathcal{D}$ is the Euler differential operator given by $\mathfrak{D} = z\frac{d}{dz}$.

From the above definition it can be seen that the ℓ-H function (5) satisfies the differential equation

$$ ({}_\ell\Delta_c^{\mathcal{D}})(\mathcal{D}+b-1)\mathcal{D}w - z(\mathcal{D}+a)w = 0, \qquad (9) $$

for $z, a \in \mathbb{C}$ and $c, b \in \mathbb{C}\backslash\{0,-1,-2,\cdots\}$ and $\ell = 0,1,2,\cdots$. It was established in [7].

Definition 3. [[7]] The ℓ-H exponential function is defined as

$$ e_H^{\ell}(z) = H\left[\begin{matrix}-;\\ -;(1:\ell)\end{matrix}\; z\right] = \sum_{n=0}^{\infty} \frac{z^n}{(n!)^{\ell n+1}}, \quad (10) $$

for all $z \in \mathbb{C}$ and $\mathcal{R}e(\ell) \geq 0$.

Lemma 4. [[12]] Let h and g be given by (2) such that $f = h + \overline{g}$ and the following condition holds:

$$ \sum_{n=1}^{\infty} [n + an(n^2-1)](|\alpha_n| + |\beta_n|) + b \leq 1, \quad (11) $$

where $0 \leq b < 1$, $\alpha_1 = 1, a \geq 0$ then f is harmonic univalent, sense-preserving in $\mathbb{D}_1(0)$ and $f \in \mathcal{H}(a,b)$.

Lemma 5. [[12]] Let $f = h + \overline{g}$ be such that h iand g are given iby (2). iThen i$f \in \mathcal{NH}(a,b)$ if and only if i

$$ \begin{aligned} &\sum_{n=2}^{\infty} n[1 + a(n^2-1)]|\alpha_n| \\ &+ \sum_{n=1}^{\infty} [n + a(n^2-1)n]|\beta_n| + b \leq 1, \end{aligned} \qquad (12) $$

in which $0 \leq b < 1$, $\alpha_1 = 1, a \geq 0$.

3. MAIN RESULTS

Theorem 6. If $a_i \leq b_i, c_i \geq 4$ and $\ell_i \geq 1$, for $i = 1,2$. Then the sufficient conditions for $\mathcal{H} = \mathcal{H}_1 + \overline{\mathcal{H}_2}$ to be harmonic univalent and sense-preserving in $\mathbb{D}_1(0)$ and $\mathcal{H}(z) \in \mathcal{H}(a,b)$ are that

$$ \gamma_2^2(\gamma_1^2 - 3\gamma_1 - 1) - \gamma_1^2(\gamma_2 + 1) \geq 0, \qquad (13) $$

$$ \begin{cases} 1 + \frac{2}{\gamma_1} + a\left[\frac{6}{\gamma_1} + \frac{27}{\gamma_1(\gamma_1+1)}\right. \\ \left. + \frac{256}{\gamma_1(\gamma_1+1)(\gamma_1+2)}\right] + \left[\frac{1+3a}{\gamma_1}\right]\left[\frac{1+\gamma_1}{\gamma_1}\right] \\ + \left[\frac{1+a}{\gamma_2}\right]\left[\frac{1+\gamma_2}{\gamma_2}\right] - a\left[\frac{3}{\gamma_1} + \frac{1}{\gamma_2}\right] \leq 2 - b, \end{cases} \qquad (14) $$

where $a \geq 0$ and $0 \leq b < 1$.

Proof. Let $\mathcal{H}(z) = \mathcal{H}_1(z) + \overline{\mathcal{H}_2(z)}$. Then

$$ \begin{aligned} \mathcal{H}(z) = z \quad &+ \sum_{n=2}^{\infty} \frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{z^n}{(n-1)!} \\ &+ \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{z^n}{n!}. \end{aligned} $$

Firstly, we prove $\mathcal{H}$ is locally univalent and sense-preserving in $\mathbb{D}_1(0)$. For this, consider

$$ \begin{aligned} |\mathcal{H}_1'(z)| &= \left|1 + \sum_{n=2}^{\infty} \frac{n(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{z^{n-1}}{(n-1)!}\right| \\ &> 1 - \sum_{n=2}^{\infty} \frac{n(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{|z|^{n-1}}{(n-1)!} \\ &\geq 1 - \sum_{n=2}^{\infty} \frac{n}{(\gamma_1)_{n-1}^{\ell_1(n-1)}}. \end{aligned} $$

Since $\gamma_1 \geq 4 > 1$ and $\ell_1 \geq 1$, it follows that $(\gamma_1)_n \leq (\gamma_1)_n^{\ell_1 n}$, for all $n \in \mathbb{N}$ and

$$ \begin{aligned} \frac{n}{(c)_{n-1}} &= \frac{n}{c(c+1)(c+2)\cdots(c+n-2)} \\ &< \frac{1}{c(c+1)^{n-3}} \quad \text{for } n \in \mathbb{N}\backslash\{1,2\}. \end{aligned} $$

So,

$$ \begin{aligned} |\mathcal{H}'_1(z)| &\geq 1 - \sum_{n=2}^{\infty} \frac{n}{(\gamma_1)_{n-1}} \\ &= 1 - \frac{2}{\gamma_1} - \frac{1}{\gamma_1}\sum_{n=0}^{\infty} \frac{1}{(\gamma_1+1)^n} \\ &= 1 - \frac{1+3\gamma_1}{\gamma_1^2} \\ &= \frac{\gamma_1^2 - 3\gamma_1 - 1}{\gamma_1^2}. \end{aligned} $$

On the other hand, by similar arguments, we have

$$ \begin{aligned} |\mathcal{H}'_2(z)| &= \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{|z|^{n-1}}{(n-1)!} \\ &\leq \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n^{\ell_2 n}} \\ &\leq \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} \\ &= \sum_{n=1}^{\infty} \frac{1}{\gamma_2(\gamma_2+1)(\gamma_2+2)\cdots(\gamma_2+n-1)} \\ &< \frac{1}{\gamma_2}\sum_{n=0}^{\infty} \frac{1}{(\gamma_2+1)^n} = \frac{\gamma_2+1}{\gamma_2^2}. \end{aligned} $$

From the condition (13), w have

$$ |\mathcal{H}'_1(z)| > |\mathcal{H}'_2(z)|. $$

Now to prove $\mathcal{H}$ is univalent in $\mathbb{D}_1(0)$, we suppose $z_1, z_2 \in \mathbb{D}_1(0)$ such that $z_1 \neq z_2$. As i$\mathbb{D}_1(0)$ is convex and simply connected, we have

$$z(t) = (1-t)z_1 + tz_2 \in \mathbb{D}_1(0),$$

where $0 \leq t \leq 1$. Therefore, we have

$$\mathcal{H}(z_1) - \mathcal{H}(z_2) = \int_0^1 [(z_2 - z_1)\mathcal{H}_1'(z(t)) + \overline{(z_2 - z_1)\mathcal{H}_2'(z(t))}]dt$$

such that

$$\begin{aligned}
&\mathcal{R}e\left\{\frac{\mathcal{H}(z_1)-\mathcal{H}(z_2)}{z_2-z_1}\right\} \\
&= \int_0^1 \mathcal{R}e\left[\mathcal{H}_1'(z(t)) + \frac{\overline{(z_2-z_1)}}{(z_2-z_1)}\overline{\mathcal{H}_2'(z(t))}\right]dt \quad (15) \\
&> \int_0^1 [\mathcal{R}e\,(\mathcal{H}_1'(z(t))) + |\mathcal{H}_2'(z(t))|]dt,
\end{aligned}$$

where

$$\begin{aligned}
&\mathcal{R}e\,(\mathcal{H}_1'(z(t))) + |\mathcal{H}_2'(z(t))| \\
&\geq 1 - \sum_{n=2}^{\infty} n\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}}\frac{|z|^{n-1}}{(n-1)!} \\
&- \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{|z|^{n-1}}{(n-1)!} \\
&\geq 1 - \sum_{n=2}^{\infty} \frac{n}{(\gamma_1)_{n-1}^{\ell_1(n-1)}} - \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n^{\ell_2 n}} \\
&\geq 1 - \sum_{n=2}^{\infty} \frac{n}{(\gamma_1)_{n-1}} - \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} \\
&\geq 1 - \frac{2}{\gamma_1} - \frac{1}{\gamma_1}\sum_{n=0}^{\infty} \frac{1}{(\gamma_1+1)^n} - \frac{1}{\gamma_2}\sum_{n=0}^{\infty} \frac{1}{(\gamma_2+1)^n} \\
&= \frac{\gamma_1^2 - 3\gamma_1 - 1}{\gamma_1^2} - \frac{\gamma_2+1}{\gamma_2^2} \geq 0.
\end{aligned}$$

Thus, by (15), we get $\mathcal{H}(z_1) \neq \mathcal{H}(z_2)$ and hence $\mathcal{H}$ is univalent in $\mathcal{D}_1(0)$. Finally, we prove $\mathcal{H} \in \mathcal{H}(a,b)$. iIn order to prove this, it is suffices to prove condition (11). i.e.,

$$\sum_{n=1}^{\infty} n[1 + a(n^2-1)][\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}}\frac{1}{(n-1)!} + \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{1}{n!}] \leq 2 - b. \quad (16)$$

Under the given conditions, we have

$$\begin{aligned}
\frac{n^3}{(\gamma_1)_{n-1}} &\leq \frac{n^2}{\gamma_1(\gamma_1+1)_{n-3}} \\
&= \frac{n(n-3)}{\gamma_1(\gamma_1+1)_{n-3}} + \frac{3n}{\gamma_1(\gamma_1+1)_{n-3}} \\
&\leq \frac{1}{\gamma_1(\gamma_1+1)^{n-5}} + \frac{3}{\gamma_1(\gamma_1+1)^{n-4}}
\end{aligned}$$

for $n \in \mathbb{N}\backslash\{1,2,3,4\}$,

$$\begin{aligned}
\frac{n^2}{(\gamma_2)_n} &= \frac{n(n-1)}{(\gamma_2)_n} + \frac{n}{(\gamma_2)_n} \\
&\leq \frac{1}{\gamma_2(\gamma_2+1)^{n-3}} + \frac{1}{\gamma_2(\gamma_2+1)^{n-2}}
\end{aligned}$$

for $n \in \mathbb{N}\backslash\{1,2\}$,

$$\frac{n}{(\gamma_1)_{n-1}} \leq \frac{1}{\gamma_1(\gamma_1+1)^{n-3}} \text{for} n \in \mathbb{N}\backslash\{1,2\},$$

and $\frac{1}{(\gamma_2)_n} \leq \frac{1}{\gamma_2(\gamma_2+1)^{n-1}} \text{for} n \in \mathbb{N}$. Now, consider

$$\begin{aligned}
&\sum_{n=1}^{\infty} n[1 + a(n^2-1)][\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}}\frac{1}{(n-1)!} + \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{1}{n!}] \\
&= \sum_{n=1}^{\infty} (1-a)n\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}}\frac{1}{(n-1)!} \\
&+ \sum_{n=1}^{\infty} an^3\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}}\frac{1}{(n-1)!} \\
&+ \sum_{n=1}^{\infty} (1-a)n\frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{1}{n!} \\
&+ \sum_{n=1}^{\infty} an^3\frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{1}{n!} \\
&\leq (1-a)\sum_{n=1}^{\infty} \frac{n}{(\gamma_1)_{n-1}} + a\sum_{n=1}^{\infty} \frac{n^3}{(\gamma_1)_{n-1}} \\
&+ (1-a)\sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} + a\sum_{n=1}^{\infty} \frac{n^2}{(\gamma_2)_n} \\
&= (1-a)\left[1 + \frac{2}{\gamma_1}\right] + (1-a)\sum_{n=3}^{\infty} \frac{n}{(\gamma_1)_{n-1}} \\
&+ a\left[1 + \frac{8}{\gamma_1} + \frac{27}{\gamma_1(\gamma_1+1)} + \frac{256}{\gamma_1(\gamma_1+1)(\gamma_1+2)}\right] \\
&+ a\sum_{n=5}^{\infty} \frac{n^3}{(\gamma_1)_{n-1}} + (1-a)\sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} \\
&+ a\left[\frac{1}{\gamma_2} + \frac{4}{\gamma_2(\gamma_2+1)}\right] + a\sum_{n=3}^{\infty} \frac{n^2}{(\gamma_2)_n} \\
&= 1 + \frac{2}{\gamma_1} + a\left[\frac{6}{\gamma_1} + \frac{27}{\gamma_1(\gamma_1+1)} + \frac{256}{\gamma_1(\gamma_1+1)(\gamma_1+2)}\right] \\
&+ \left[\frac{1+3a}{\gamma_1}\right]\sum_{n=0}^{\infty} \frac{1}{(\gamma_1+1)^n} \\
&+ \left[\frac{1+a}{\gamma_2}\right]\sum_{n=0}^{\infty} \frac{1}{(\gamma_2+1)^n} - a\left[\frac{3}{\gamma_1} + \frac{1}{\gamma_2}\right] \\
&= 1 + \frac{2}{\gamma_1} + a\left[\frac{6}{\gamma_1} + \frac{27}{\gamma_1(\gamma_1+1)} + \frac{256}{\gamma_1(\gamma_1+1)(\gamma_1+2)}\right] \\
&+ \left[\frac{1+3a}{\gamma_1}\right]\left[\frac{1+\gamma_1}{\gamma_1}\right] \\
&+ \left[\frac{1+a}{\gamma_2}\right]\left[\frac{1+\gamma_2}{\gamma_2}\right] - a\left[\frac{3}{\gamma_1} + \frac{1}{\gamma_2}\right] \\
&\leq 2 - b.
\end{aligned}$$

This completes the proof.

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Define a function,

$$\mathcal{F}_1(z) = 2z - \mathcal{H}_1(z) - \overline{\mathcal{H}_2(z)}$$
$$= z - \sum_{n=2}^{\infty} \frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{z^n}{(n-1)!} - \overline{\sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{z^n}{n!}}.$$

Theorem 7. Let $a \geq 0$, $0 \leq b < 1$, $a_i \leq b_i, c_i \geq 4$ and $\ell_i \geq 1$, for $i = 1,2$ and $\alpha_2 < \beta_2 \gamma_2^{\ell_2}$. Then $\mathcal{F}_1(z) \in \mathcal{NH}(a,b)$ iff (13) and (14) holds.

Proof. By definition, it is clear that $\mathcal{F}_1(z) \in \mathcal{NH}$. Now suppose (13) and (14) holds. Then, by Theorem 3 $\mathcal{F}_1(z) \in \mathcal{H}(a,b)$. Hence, $\mathcal{F}_1(z) \in \mathcal{NH}(a,b)$.

Conversely, suppose $\mathcal{F}_1(z) \in \mathcal{NH}(a,b)$. Since $\mathcal{NH}(a,b) \subset \mathcal{H}(a,b)$, $\mathcal{F}_1(z) \in \mathcal{H}(a,b)$. So, $\mathcal{F}_1$ satisfies the inequalities (13) and (16) by Theorem 3 and hence (14) holds.

Theorem 8. Let $a \geq 0$, $0 \leq b < 1$, $a_i \leq b_i, c_i \geq 4$ and $\ell_i \geq 1$, for $i = 1,2$ and $\alpha_2 < \beta_2 \gamma_2^{\ell_2}$. Then the necessary and sufficient condition for $f \star (\mathcal{H}_1 + \overline{\mathcal{H}_2}) \in \mathcal{NH}(a,b)$, where $f \in \mathcal{NH}(a,b)$ is that

$$\frac{\gamma_1 + 1}{\gamma_1^2} + \frac{\gamma_2 + 1}{\gamma_2^2} \leq 1.$$

Proof. Let $f = h + \overline{g} \in \mathcal{NH}(a,b)$, in which h and g defined by (2). Then

$$f \star (\mathcal{H}_1 + \overline{\mathcal{H}_2})(z) = h(z) \star \mathcal{H}_1(z) + \overline{g(z) \star \mathcal{H}_2(z)}$$
$$= z - \sum_{n=2}^{\infty} \frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{z^n}{(n-1)!} - \overline{\sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{z^n}{n!}}.$$

By Lemma 2, $f \star (\mathcal{H}_1 + \overline{\mathcal{H}_2}) \in \mathcal{NH}(a,b)$ iff

$$\sum_{n=1}^{\infty} [n + a(n^2-1)n] \left[\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{a_n}{(n-1)!} + \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{b_n}{n!} \right] \leq 2 - b.$$

By Lemma 2,

$$\sum_{n=1}^{\infty} [n + a(n^2-1)n](a_n + b_n) + b \leq 2.$$

That is,

$$\sum_{n=2}^{\infty} n[1 + a(n^2-1)]a_n + \sum_{n=1}^{\infty} n[1 + a(n^2-1)]b_n \leq 1 - b,$$
$$n[1 + a(n^2-1)]a_n \leq 1 - b \text{ and}$$
$$n[1 + a(n^2-1)]b_n \leq 1 - b \quad (17)$$
$$a_n \leq \frac{1-b}{n[1+a(n^2-1)]} \text{ and}$$
$$b_n \leq \frac{1-b}{n[1+a(n^2-1)]}, (n \geq 1).$$

Now, from (17), we have

$$\sum_{n=1}^{\infty} n[1 + a(n^2-1)] \left[\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{a_n}{(n-1)!} + \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{b_n}{n!} \right]$$
$$\leq \sum_{n=2}^{\infty} (1-b) \frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{1}{(n-1)!} + \sum_{n=1}^{\infty} (1-b) \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{1}{n!}$$
$$= (1-b) \left[\sum_{n=1}^{\infty} \frac{(\alpha_1)_n}{(\beta_1)_n(\gamma_1)_n^{\ell_1 n}} \frac{1}{n!} + \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{1}{n!} \right]$$
$$\leq (1-b) \left[\sum_{n=1}^{\infty} \frac{1}{(\gamma_1)_n^{\ell_1 n}} + \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n^{\ell_2 n}} \right]$$
$$\leq (1-b) \left[\sum_{n=1}^{\infty} \frac{1}{(\gamma_1)_n} + \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} \right]$$
$$\leq (1-b) \left[\sum_{n=1}^{\infty} \frac{1}{\gamma_1(\gamma_1+1)^{n-1}} + \sum_{n=1}^{\infty} \frac{1}{\gamma_2(\gamma_2+1)^{n-1}} \right]$$
$$\leq (1-b) \left[\frac{\gamma_1 + 1}{\gamma_1^2} + \frac{\gamma_2 + 1}{\gamma_2^2} \right]$$

This completes the proof.

Theorem 9. Let $a_i \leq b_i, c_i \geq 4$ and $\ell_i \geq 1$, for $i = 1,2$ and $\alpha_2 < \beta_2 \gamma_2^{\ell_2}$. Then the necessary and sufficient condition for a function

$$\mathcal{F}_2(z) = \int_0^z H \begin{bmatrix} \alpha_1; \\ \beta_1; (\gamma_1 : \ell_1) \end{bmatrix} t \, dt + \overline{\int_0^z \left[H \begin{bmatrix} \alpha_2; \\ \beta_2; (\gamma_2 : \ell_2) \end{bmatrix} t - 1 \right] dt}$$

to be in $\mathcal{H}(a,b)$ is that

$$[1 + 3a] \left[\frac{\gamma_1 + 1}{\gamma_1^2} + \frac{\gamma_2 + 1}{\gamma_2^2} \right] + a \left[\frac{1}{\gamma_1} + \frac{1}{\gamma_2} \right] \leq 1 - b,$$

where $a \geq 0$ and $0 \leq b < 1$.

Proof. From Lemma 2, the function

$$\mathcal{F}_2(z) = z + \sum_{n=2}^{\infty} \frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}} \frac{z^n}{(n-1)!\,n} + \sum_{n=2}^{\infty} \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{z^n}{(n-1)!\,n}$$

is in $\mathcal{H}(a,b)$ if

$$\sum_{n=2}^{\infty} n[1 + a(n^2-1)][\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}(n-1)!\,n} + \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}(n-1)!\,n}] \leq 1-b.$$

So, consider

$$\sum_{n=2}^{\infty}[1 + a(n^2-1)][\frac{(\alpha_1)_{n-1}}{(\beta_1)_{n-1}(\gamma_1)_{n-1}^{\ell_1(n-1)}(n-1)!} + \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}(n-1)!}]$$

$$= \sum_{n=1}^{\infty} \frac{(\alpha_1)_n}{(\beta_1)_n(\gamma_1)_n^{\ell_1 n} n!} + \sum_{n=1}^{\infty} \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n} n!}$$

$$+a\sum_{n=1}^{\infty} n^2 \frac{(\alpha_1)_n}{(\beta_1)_n(\gamma_1)_n^{\ell_1 n} n!} + a\sum_{n=1}^{\infty} n^2 \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n} n!}$$

$$+2a\sum_{n=1}^{\infty} n \frac{(\alpha_1)_n}{(\beta_1)_n(\gamma_1)_n^{\ell_1 n} n!} + 2a\sum_{n=1}^{\infty} n \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n} n!}$$

$$\leq \sum_{n=1}^{\infty} \frac{1}{(\gamma_1)_n} + \sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n} + a\sum_{n=1}^{\infty} \frac{n}{(\gamma_1)_n} + a\sum_{n=1}^{\infty} \frac{n}{(\gamma_2)_n}$$

$$+2a\sum_{n=1}^{\infty} \frac{1}{(\gamma_1)_n} + 2a\sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n}$$

$$= (1+2a)\sum_{n=1}^{\infty} \frac{1}{(\gamma_1)_n} + (1+2a)\sum_{n=1}^{\infty} \frac{1}{(\gamma_2)_n}$$

$$+a\sum_{n=1}^{\infty} \frac{n}{(\gamma_1)_n} + a\sum_{n=1}^{\infty} \frac{n}{(\gamma_2)_n}$$

$$\leq [1+2a]\left[\frac{\gamma_1+1}{\gamma_1^2} + \frac{\gamma_2+1}{\gamma_2^2}\right] + a\left[\frac{1}{\gamma_1} + \frac{1}{\gamma_2}\right]$$

$$+a[\sum_{n=2}^{\infty} \frac{1}{\gamma_1(\gamma_1+1)^{n-2}} + \sum_{n=2}^{\infty} \frac{1}{\gamma_2(\gamma_2+1)^{n-2}}]$$

$$\leq [1+2a]\left[\frac{\gamma_1+1}{\gamma_1^2} + \frac{\gamma_2+1}{\gamma_2^2}\right] + a\left[\frac{2\gamma_1+1}{\gamma_1^2} + \frac{2\gamma_2+1}{\gamma_2^2}\right]$$

$$\leq [1+3a]\left[\frac{\gamma_1+1}{\gamma_1^2} + \frac{\gamma_2+1}{\gamma_2^2}\right] + a\left[\frac{1}{\gamma_1} + \frac{1}{\gamma_2}\right]$$

$$\leq 1-b.$$

Theorem 9. Let $a_i \leq b_i, c_i \geq 4$ and $\ell_i \geq 1$, for $i = 1,2$ and $\alpha_2 < \beta_2 \gamma_2^{\ell_2}$. Then the necessary and sufficient condition for

$$\mathcal{F}_3(z) = \int_0^z H\left[\begin{matrix}\alpha_1; \\ \beta_1; (\gamma_1 : \ell_1)\end{matrix}\; t\right] dt - \int_0^z \left[H\left[\begin{matrix}\alpha_2; \\ \beta_2; (\gamma_2 : \ell_2)\end{matrix}\; t\right] - 1\right] dt$$

to be in $\mathcal{H}(a,b)$ is that

$$\left[\frac{4a+\gamma_1+1}{\gamma_1^{1+\ell_1}}\right] + (1+4a)\left[\frac{1+\gamma_2}{\gamma_2^2}\right] + \frac{a}{\gamma_2} \leq 1-b,$$

where $a \geq 0$ and $0 \leq b < 1$.

Proof. From Lemma 5, the function

$$\mathcal{F}_3(z) = z - [\frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \sum_{n=2}^{\infty} \frac{(\alpha_1+1)_{n-2}}{(\beta_1+1)_{n-2}(\gamma_1+1)_{n-2}^{\ell_1(n-2)}} \times \frac{z^n}{(n-1)!\,n}] - \sum_{n=2}^{\infty} \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{z^n}{(n-1)!\,n}$$

is in $\mathcal{H}(a,b)$ if

$$\sum_{n=2}^{\infty} n[1 + a(n^2-1)] \times [\frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_{n-2}}{(\beta_1+1)_{n-2}(\gamma_1+1)_{n-2}^{\ell_1(n-2)}} \frac{1}{(n-1)!\,n} + \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{1}{(n-1)!\,n}] \leq 1-b.$$

So, consider

$$\sum_{n=2}^{\infty}[1 + a(n^2-1)] \times [\frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_{n-2}}{(\beta_1+1)_{n-2}(\gamma_1+1)_{n-2}^{\ell_1(n-2)}} \frac{1}{(n-1)!} + \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{1}{(n-1)!}]$$

$$= \sum_{n=2}^{\infty} \frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_{n-2}}{(\beta_1+1)_{n-2}(\gamma_1+1)_{n-2}^{\ell_1(n-2)}} \frac{1}{(n-1)!} + \sum_{n=2}^{\infty} \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{1}{(n-1)!}$$

$$+a\sum_{n=2}^{\infty} \frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(n^2-1)(\alpha_1+1)_{n-2}}{(\beta_1+1)_{n-2}(\gamma_1+1)_{n-2}^{\ell_1(n-2)}} \frac{1}{(n-1)!} + a\sum_{n=2}^{\infty} (n^2-1) \frac{(\alpha_2)_{n-1}}{(\beta_2)_{n-1}(\gamma_2)_{n-1}^{\ell_2(n-1)}} \frac{1}{(n-1)!}$$

$$= \sum_{n=0}^{\infty} \frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_n}{(\beta_1+1)_n(\gamma_1+1)_n^{\ell_1 n}} \frac{1}{(n+1)!} + a\sum_{n=0}^{\infty} n \frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_n}{(\beta_1+1)_n(\gamma_1+1)_n^{\ell_1 n}} \frac{1}{n!}$$

$$+3a\sum_{n=0}^{\infty} \frac{|\alpha_1|}{\beta_1 \gamma_1^{\ell_1}} \frac{(\alpha_1+1)_n}{(\beta_1+1)_n(\gamma_1+1)_n^{\ell_1 n}} \frac{1}{n!} + a\sum_{n=1}^{\infty} n^2 \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{1}{n!}$$

$$+2a\sum_{n=1}^{\infty} n \frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}} \frac{1}{n!}$$

$$+(1+a)\sum_{n=1}^{\infty}\frac{(\alpha_2)_n}{(\beta_2)_n(\gamma_2)_n^{\ell_2 n}}\frac{1}{n!}$$
$$\leq \frac{1}{\gamma_1^{\ell_1}}\sum_{n=0}^{\infty}\frac{1}{(\gamma_1+1)_n^{\ell_1 n}}+\frac{a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)_n^{\ell_1 n}}$$
$$+\frac{3a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)_n^{\ell_1 n}}$$
$$+a\sum_{n=1}^{\infty}\frac{n}{(\gamma_2)_n^{\ell_2 n}}+2a\sum_{n=1}^{\infty}\frac{1}{(\gamma_2)_n^{\ell_2 n}}$$
$$+(1+a)\sum_{n=1}^{\infty}\frac{1}{(\gamma_2)_n^{\ell_2 n}}$$
$$\leq \frac{1}{\gamma_1^{\ell_1}}\left[1+\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)_n}\right]+\frac{a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)_n}$$
$$+\frac{3a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)_n}+a\sum_{n=1}^{\infty}\frac{n}{(\gamma_2)_n}+2a\sum_{n=1}^{\infty}\frac{1}{(\gamma_2)_n}$$
$$+(1+a)\sum_{n=1}^{\infty}\frac{1}{(\gamma_2)_n}$$
$$\leq \frac{1}{\gamma_1^{\ell_1}}\left[1+\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)^n}\right]+\frac{a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)^n}$$
$$+\frac{3a}{\gamma_1^{\ell_1}}\sum_{n=1}^{\infty}\frac{1}{(\gamma_1+1)^n}+a\left[\frac{1}{\gamma_2}+\sum_{n=2}^{\infty}\frac{1}{\gamma_2(\gamma_2+1)^{n-2}}\right]$$
$$+(1+3a)\sum_{n=1}^{\infty}\frac{1}{\gamma_2(\gamma_2+1)^{n-1}}$$
$$\leq \frac{1+\gamma_1}{\gamma_1^{1+\ell_1}}+\frac{a}{\gamma_1^{1+\ell_1}}+\frac{3a}{\gamma_1^{1+\ell_1}}+a\left[\frac{1}{\gamma_2}+\frac{1+\gamma_2}{\gamma_2^2}\right]$$
$$+(1+3a)\left[\frac{1+\gamma_2}{\gamma_2^2}\right]$$
$$\leq \left[\frac{4a+\gamma_1+1}{\gamma_1^{1+\ell_1}}\right]+(1+4a)\left[\frac{1+\gamma_2}{\gamma_2^2}\right]+\frac{a}{\gamma_2}$$
$$\leq 1-b.$$

This completes the proof.

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Armed Unmanned Aerial Vehicle

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Abstract:

The emergence of Unmanned Aerial Vehicle (UAV) has created a very important need due to their features including stability, long range communication, their robustness and their compact size. All these creates suitable opportunities that are needed to be fulfilled. A single UAV can be deployed for various missions such as surveillance in unknown areas, structural monitoring, and in imperative need even show offensive behavior. The armed UAV's plays an important role in the defense and security application of the country. Another purpose for the UAV can be a certain monitoring in a warzone climate. In this research paper we have presented how the UAV can be applied in such scenarios. The UAV will detect the target object and compare it with the database stored in the memory of raspberry pi and whenever the target is detected, it will send the image of the target to the operator. who can manually send the signal from transmitter, to trigger the grenade from the UAV. For the UAV, the platform used is DJI NAZA mLite and for the enemy object detection it is Anaconda Software.

Keywords:

Unmanned Aerial Vehicle, NAZA-M Lite Controller, Raspberry Pi 3B

1. INTRODUCTION

A. History

The Unmanned Aerial Vehicle(UAV) has been originated from the beginning of World War I. Developed till cruising missiles like tomahawks and harpoons (no head missiles basically) and now the current family of the UAV Drones. A very old tactic used in an Austrian attack was the use of unmanned balloons with loaded explosives, some of them managed to drop but some of them were redirected from path dude to wind flow. [1]

During World War I came the advent of low radio control techniques, the Royal Flying Corps' Ruston Proctor Aerial Target was utilized in 1916. The concept was to build a small and simple yet effective aircraft packed with explosives and be guided to the target according to the User. [2].

World War II bought more of these unmanned aerial munitions including torpedoes which were built on the same radio-controlled(RC) principle.

Cold War was another event that brought along another ingenious application of the UAV which was in ISTAR (Intelligence, Surveillance, Target Acquisition, and Reconnaissance) Systems. [3]

B. Classification

In terms of Roles performed by the UAVs in military areas there can be the ISTAR, UCAV, multi-purpose, Radar communication relay, aerial supply delivery, and R&D.

- ISTAR UAVS

ISTAR is the acronym for information, surveillance, target acquisition, and reconnaissance. It's a method that joins sensory peripherals together to improve the functionality of UAV in the Warzone environment to provide aid in combat/battle force and manage the intel acquired. Again the ISTAR was succeeded by the IMINT (Imagery Intelligence) which used satellites for a broad display of the warzone. [4,5]

Fig. 1: The Iranian Mohajer-6 ISTAR Drone (Courtesy of UAV Road Map December 2002 edition)

- UCAVs

Abbreviation for Unmanned Combat Aerial Vehicles, UCAVs are essential in the eradication of the designated target. The other purpose of UCAVs was to bring the decrement in the risk factors of human pilots being behind the enemy lines. With their covert design and acute precision, the UCAVs can be capable of nullifying targets deep in the Battlefield with minimal collateral damage. [4,5]

Fig. 2: The Russian Okhotnik-B Combat Drone(UCAV) (Courtesy of UAV Road Map December 2002 edition)

- MULTIPURPOSE UAVs

As the name suggests they are combination of both ISTAR and Combat UAVs. Launched in 2002 their complexity was a tough engineering challenge. [4,5]

C. Peripherals Description

- Raspberry Pi Model 3B

The Model used here is the third generation/iteration of the raspberry pi. It is an ARM-based low-cost and a powerful credit card-sized single-board computer that is applicable in many applications. While preserving the original board format Raspberry Pi Model 3B provides a 10x faster performance compared to the first generation.

Addition to this, it also features LAN and Bluetooth connection making it perfect for UAV Communication. [6]

Fig. 3: Raspberry Pi 3B and Pi-Camera

- DJI NAZA-M Lite Controller

The NAZA-M Lite Controller is an All-in-One Design based Controller System which has inherited the high reliability and stability of its former NAZA-M. It also consumes lesser space and UAV Weight distribution is also balanced.

It will offer the Pilot to operate the UAV in GPS Mode (Most reliable/stable), Altitude Mode, Manual Mode and can also adjust according to the flight environment and conditions. The controller also comes with a GPS Module for further stabilization.

Fig. 4: The NAZA-M Lite Controller

- Li-PO Battery

The Lithium Batteries are preferred over here as they are used in most of the electrical devices today. With a higher discharge rate and a high weight vs stored energy ratio, they can be utilized for the task substantially. The charging issue is a tedious one and is not a negligible issue. [7]

Fig. 5: The standard issue 5000mAh LI-PO Battery

- Raspberry Pi-Camera

The Raspberry Pi-camera is a standard-issue camera that will be capturing the HD videos at 1920*1080 resolution. It provides enough convenience for use for typical usage operating on the UAV. The camera uses its own dedicated CSI Interface, designed especially for camera interfacing.

2. PROPOSED UAV DESIGN

The need for various applications in our Military Domain brings us to a Standard Issue UAV which comprises of data acquisition and processing unit for various feeds it will be capturing. It also includes an attacking initiative that is a grenade launching mechanism with high accuracy. The operation between the transmitter and receiver units works on the ISM 2.4 GHz band that is available to all. Moreover, the UAV has a superb feature of Home-Location landing where it will return to its take-off point whenever the connection between transmitter and receiver breaks.

A. Improved design parameters

The main aim was the building up of a UAV which will provide more stability and least vibration which may tend to occur due to the other peripherals (mainly the Brushless DC Motors). The Stability is increased with the use of the GPS Module on the UAV which drives on nominal ratings. The vibrations are also needed to be reduced significantly because they tend to jitter the live feed from the camera which is installed on the UAV. We have used an Anti-Vibration Shock Absorber to bring down those vibrations in the feed. The Grenade Launching mechanism is installed beneath the UAV. This mechanism uses a servo motor that is attached to a small baton that is used for gripping on the grenade. The servo motor is connected to the controller which will allow the operator to manually operate on the Servo Motor.

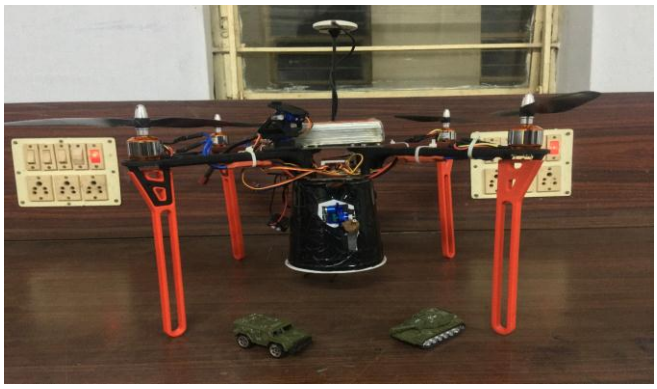

Fig. 5: Exterior display of the UAV

3. SOFTWARE IMPLEMENTATION

The UAV operates on the DJI NAZA-M Lite controller that needs to be programmed on application software DJI NAZA-M Lite Assistant version 1.00 which is very user-friendly with a configurable property and it also provides a clear graphical display of the calibration including but not limited to the Transceiver, Gimbal, GPS Module, and more.

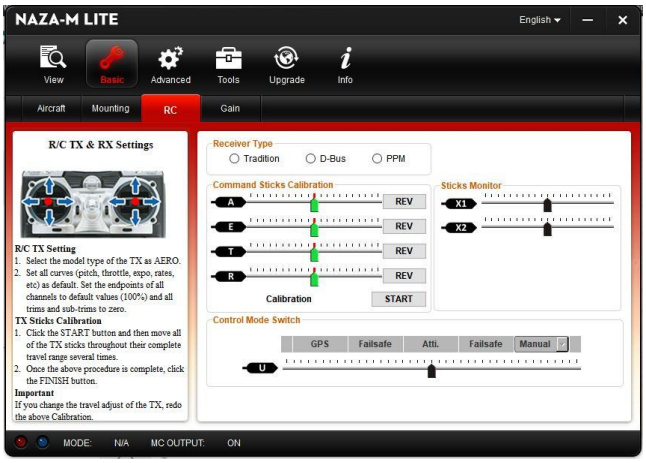

Fig. 6: Main Window of NAZA-M Lite Assistant (Courtesy of Naza-M Lite Assistant Software)

A typical RC Transceiver Calibration is displayed here in Figure 1 which can be checked while configuring with the transmitter. As for the Control Mode switch, it is preferred to use GPS mode for most stable operation. The Altitude mode allows the flight operation at a designated altitude.

The extra hardware for example Gimbal can also be configured via the software including its position relative to the altitude and the UAV.

Before altering with the various settings first of all the Operator has to select the orientation of the UAV in the software, for example, QuadrotorX or QuadRotorI.

The Controller location and orientation can also be configured with the Mounting settings. The UAV has Four types of movements that is Pitch, Roll, Yaw, and Vertical whose GAIN can be individually configured as per Operator's desire and ease.

With the Software we can also configure the motor speed from lowest to highest. Another feature of the software is the battery level indicator which will have protection levels set as per Operator's desire. The Battery used in the UAV was the 3S LIPO Battery with 5000mAh 12V Rating.

Another key feature of the Software is that in case of a misconnection between transmitter-receiver interface the UAV will safely return to the home location from where it took off.

4. OBJECT DETECTION ALGORITHM

The script for the algorithm is loaded in python language and with the aid of Jupyter notebook in Anaconda, it is executed. For the deep learning, the program uses Keras Libraries which will train the algorithm with succeeding operations on it. As the program deals with images the Numpy package is used which includes a Powerful N-dimensional array object and it also features the various processing tools in-built.

The test image is loaded from the designated directory and its pixel size is limited to 64*64 for faster processing. The Pi-Cam takes in the feed and sends it to the Raspberry Pi (Server) and shoots them forward to PC Client that is the Anaconda from there the Convolutional Neural Networks.[7]

A general CNN will consist of an input and output layer as well as many hidden layers inside. The hidden layers of a CNN typically comprise of multiple convolutional layers, pooling layers, fully connected layers, and normalization layers.[8]

In the Object detection each step executed is listed here:

1. Convolution: It is used to bring down the size of the image captured with next to none loss in its quality. It also helps in the sharpening of the image and edge detection of the image using multiple Kernels that are used to filtering the image.
2. ReLu Layer: The ReLu layer is one type of Kernel that works on maximum value function. Basically, it will bring down the image into binary values ie black and white.
3. Pooling: It is a type of image transformation where it will bring down the number of parameters when the images are too large. To bring down the dimension of the image Down Sampling is used which will also retain information. Again MAX Pooling is used which will train the program for images captured in a tilted position which is needed for the spatial invariant property of a CNN.
4. After Flattening and Full Connection the whole CNN Process is completed to train the Program.[9]

After the above process is finished training the Program the object detection and identification can be applied on the field for various test benches.

5. RESULT

We are designing a UAV system which will be used specifically for the defense purpose where one can carry lethal payload like a grenade and drop them upon the targets specified, with the help of Convolutional Neural Network (CNN).

Using live feed from the camera the UAV will be able to detect and send photographs of unidentified objects and comparing it with the one uploaded which will be enemy trucks, tanks and after confirmation with the data uploaded on the system will drop the grenade on it.

6. CONCLUSION

The current hardware/software integration is designed to be Operator-friendly. The grenade dropping is executable while hovering in mid-air. The program was executed successfully for binary object detection (Enemy Truck and Tank) which is performed on the basis of Convolution Neural Networks. The Operator will be able to observe the designated target on his/her screen. The Operator can manually trigger the grenade drop that is on the transmitter itself..

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Facial Expression Detection using Viola-Jones Algorithm

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Abstract:

An important topic in the field of Computer Vision and Artificial Intelligence is facial expression recognition. There are two medium of communication one is verbal and another is non-verbal. Among verbal and non-verbal means of communication, facial expression is a non-verbal means of communication. Facial expression plays a vital role which helps human to express their emotions, express their feelings, mental health, perspective etc. Understanding becomes easier when human and computer interact with one another if computer can response to non-verbal communication of human which is nothing but emotions expressed. In this paper, an algorithm is presented for object detection based on Viola-Jones Algorithm. This algorithm is widely used in object detection and the main property of this algorithm is that it's training is slow but detection is fast.

Keywords:

Computer Vision, Emotion Recognition, Facial Expression, Image Processing

1. INTRODUCTION

Image processing is the analysis and manipulation of digitalized image so as to improve its quality. It is the technique of changing an image into digital or computerized form and perform different tasks so as to upgrade or enhance the image and obtain useful data from it. In purpose of obtaining enhanced digital images various types of computer algorithms are used.[9]

Basically, Communication can be done in two ways: verbal communication and non-verbal communication. A very essential mode of communication is human facial expressions and this comes under non-verbal mode of communication. Face expression detection is the way toward characterizing assortment of looks of feelings or emotions such as sad, happy, anger, surprised etc. When there is a smile on human face, it shows their happiness which can also be expressed in an eye by having a curved shape. The sad expression is the inclination of detachment which is ordinarily communicated as rising slanted eyebrows and frown. The anger on human face is identified with horrendous and disturbing conditions which can be expressed with squeezed eyebrows, slender and stretched eyelids. [5]

2. METHODOLOGY

The facial expression detection system consists of the following steps as shown in the figure 1:[8]

a. Input: The input images are either obtained manually or the data are gathered from the internet.

b. Pre-processing: This is the second step where the input images are converted from RGB to Gray scale image and if there is presence of any kind of noise then it is removed in this step only.

c. Feature Extraction: In this step, a specific facial feature is extracted that is used for the identification of the given facial expression in the input image and also are used for training the model.

d. Classification: Various classification techniques are used here in order to classify the given extracted feature in its appropriate class.

e. Output: This is the final step where the classified expressions are assigned to a category of facial expression**.**

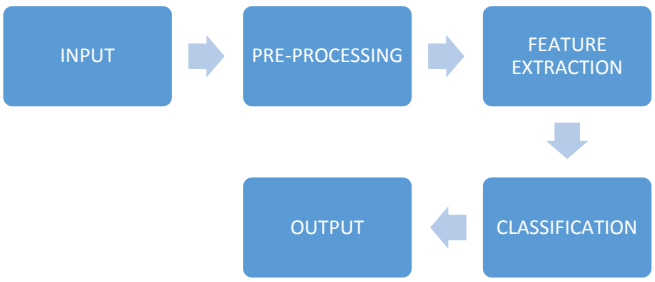

fig 1: Facial Expression Detection System Architecture

3. PROPOSED ALGORITHM

In this paper, we will be demonstrating Viola-Jones Algorithm to detect facial features. Steps for face detection in given the set of images are:

Step 1: An image is passed as an input image and based on this image the features are extracted.

Step 2: In this step, the faces are detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

Step 3: In this step, the nose of each face is detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

Step 4: In this step, the mouth of each face is detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

Step 5: In this step, the eyes are detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

The demonstration of the project detects face, nose, mouth and eyes using the MATLAB built-in class and function. This demonstration is done based on Viola-Jones face detection algorithm. The toolbox contains visionCascadeObjectDetector System Object which detects objects based on above mentioned algorithm.

Step 1: An image is passed as an input image and based on this image the features are extracted.

fig 2: Input Image

Step 2: In this step, the faces are detected from the given input image, using parameters like Position,Line width, Line style and Edge color.

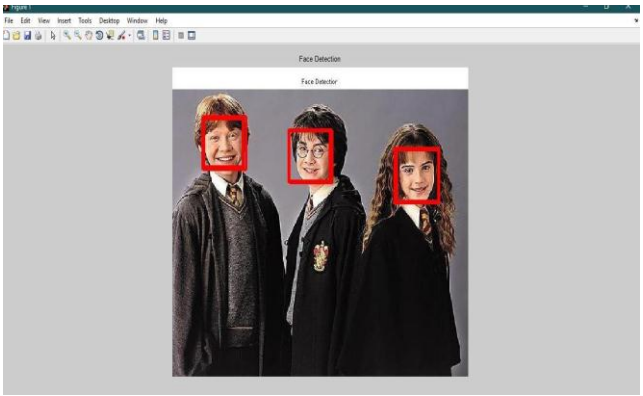

fig 3: Face Detection

Step 3: In this step, the nose of each face is detected from the given input image, using parameters like Position,Line width, Line style and Edge color.

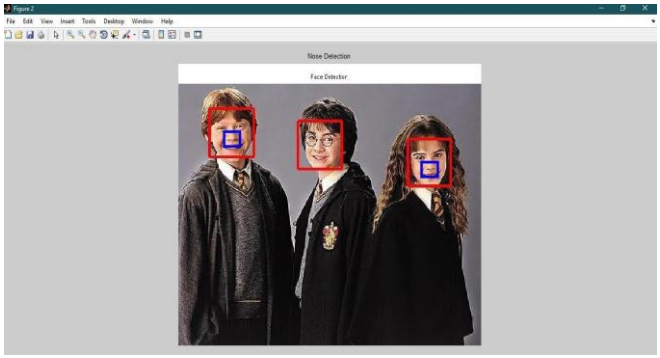

fig 4: Nose Detection

Step 4: In this step, the mouth of each face is detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

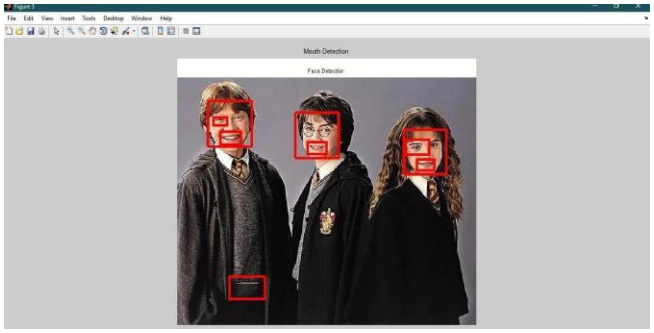

fig 5: Mouth Detection

Step 5*:* In this step, the eyes are detected from the given input image, using parameters like Position, Line width, Line style and Edge color.

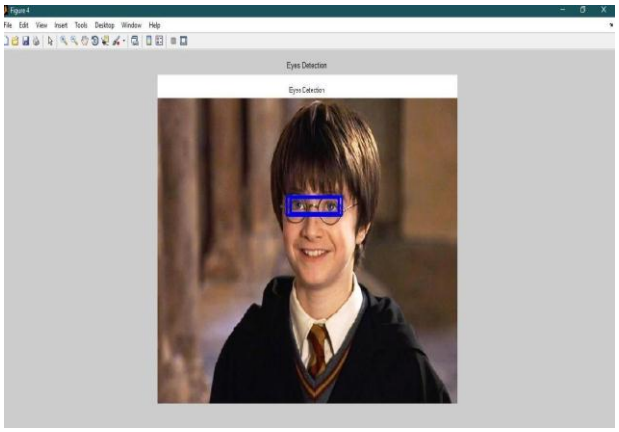

fig 6: Eyes Detection

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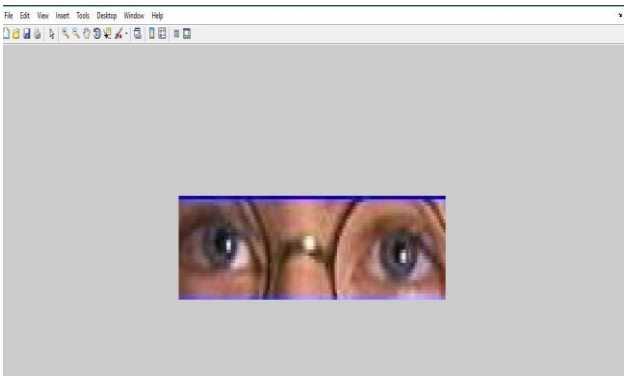

fig 7: Eyes Detection

4. RESULTS AND DISCUSSION

S.No.	Steps	Result Obtained
1.	Step 1: Read Image	The input images which is nothing but the target and reference images were loaded.
2.	Step 2 : Face Detection	The faces were detected from the given input image, using parameters like Position, Line width, Line style and Edge color.
3.	Step 3 : Nose Detection	The nose of each face was detected from the given input image, using parameters like Position, Line width, Line style and Edge color.
4.	Step 4 : Mouth Detection	The mouth of each face was detected from the given input image, using parameters like Position, Line width, Line style and Edge color.
5.	Step 5 : Eyes Detection	The eyes of each face were detected from the given input image, using parameters like Position, Line width, Line style and Edge color.
6.	Step 6: Detect another face	Similarly, other faces were detected using the above mentioned steps.

Table 1: Results and Discussion

5. CONCLUSION

There are large number of techniques used in recognizing and segmenting objects today. In this paper, the proposed algorithm provided good detection results and was effective in detecting the facial features in the given sample images. However, most sophisticated techniques can be used for object recognition and segmentation such that they deal with occlusions and luminous effects and give better results. Algorithmic techniques can be improved in the future if we work upon reducing their complexities and can also be used in hardware implementation

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Object Detection Using Point Feature Matching Algorithm

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Abstract:

Object Detection plays a significant role in areas of computer vision and image processing in order to analyze images and extract meaningful data from them. Object detection basically involves the process of identifying specific object in an image or video. It is the field that has been widely used and researched because of its various application and widespread usage. In this paper, an algorithm is presented for object detection based on point feature matching. Point Feature Matching works as an effective method to help detect a specific object in a cluttered scene. This method can be used to detect single objects in any given scene. This object detection method is most effective for objects showing non-repeating texture patterns, which gives rise to exclusive feature matches.

Keywords:

Computer Vision; Image Processing; Object Detection; Point Feature Matching

1. INTRODUCTION

Image processing is a method in which certain operations are performed in an image, in order to get an improved image or to extract some meaningful information from it [1]. Digital image processing is widely used for various fields and applications such as remote sensing, photography, medicine, film and video production, security monitoring. New innovative technologies have been rapidly progressing in the fields of image processing, especially in object recognition domain.

Object detection is a process in which specific objects are identified in an image or video sequence. Any object in an image contains many features which have interesting points on the object. A "feature" description of the object can be provided based on the above extracted points. This extracted description from a training image can then be used to identify the object, while making an attempt to locate the object in a test image containing many other objects [2].

2. METHODOLOGY

The object detection system usually comprises of the following steps as shown in fig 1. below [3].

1. In the first step, required input image is obtained from the dataset. The image acquisition process can be either manual or can be obtained from the internet.
2. The second step comprises of pre-processing which involves noise removal from the image. It also converts the image from RGB to grayscale.
3. In feature extraction step, a set of characteristic features are extracted from the object. These features can further be used to train the model to help identify specific objects in the given image.
4. In detection, the result of the previous stages are combined to determine whether the input image contains object of the given class.
5. The final output basically comprises of detecting target objects in the specified scene.

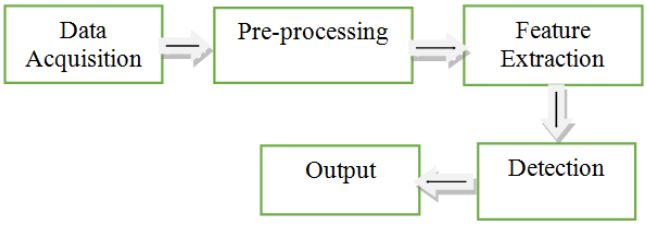

Fig 1. Block diagram of object detection system

3. PROPOSED ALGORITHM

In this paper we will be demonstrating Point Feature Matching Algorithm to detect specific objects in a cluttered scene. The steps involved are as follows:

Step 1: Read a set of input images.

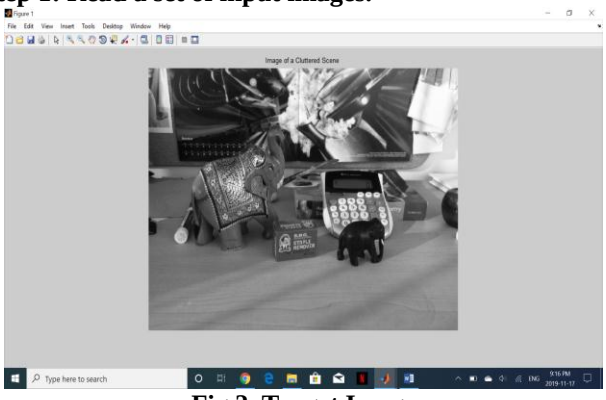

Fig 2. Target Image

Fig 3. Reference Image

Step 2: Detect Feature Points from the Image

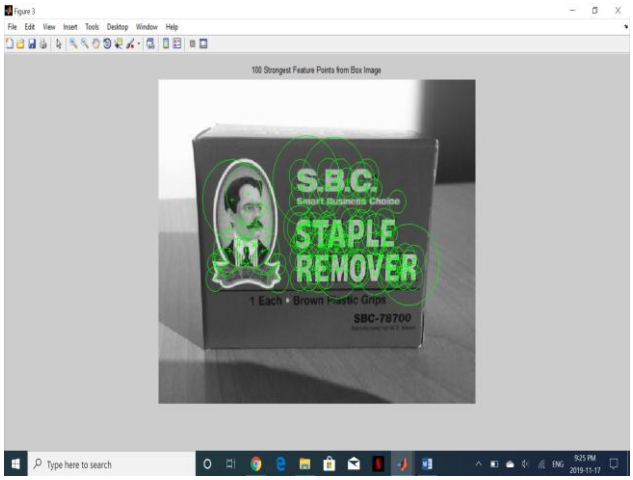

Fig 4. 100 strongest feature points from the reference image

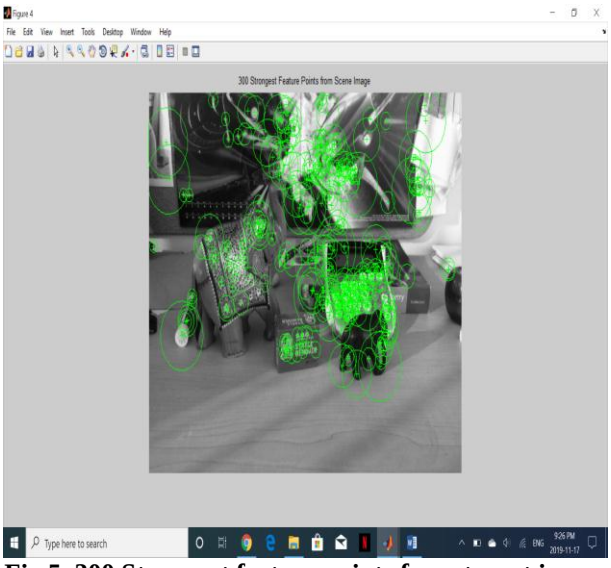

Fig 5. 300 Strongest feature points from target image

Step 3: Extract Feature Descriptors from the Image

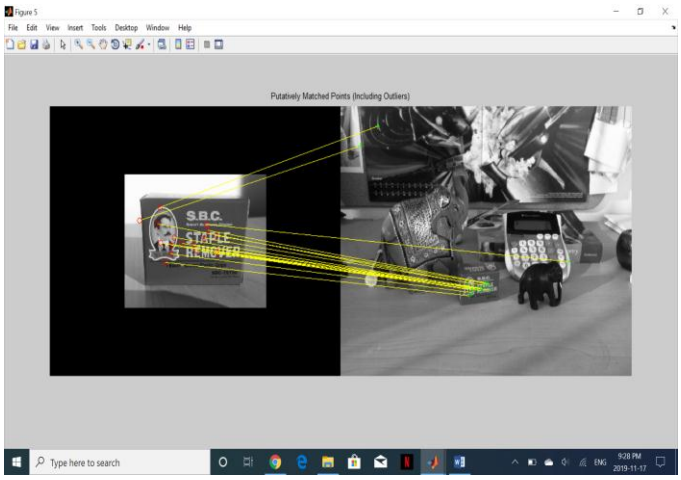

Fig 6. Matched points (May Include Outliers)

Step 4: Locate the Object in the Scene Using Matched Points

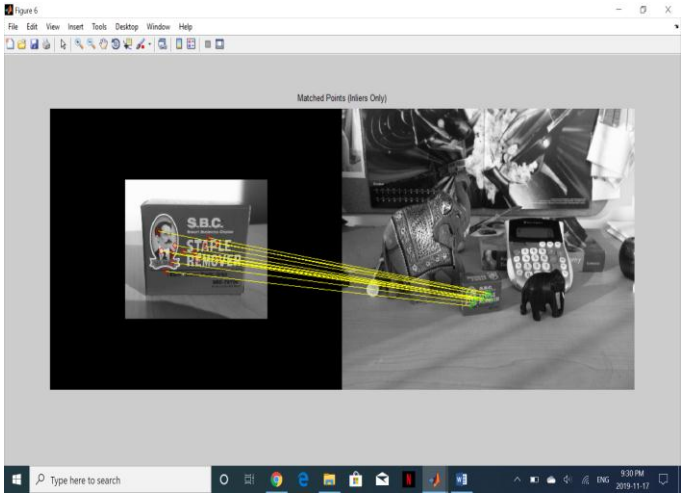

Fig 7. Matched points (Inliers Only)

Step 5: Display the detected object

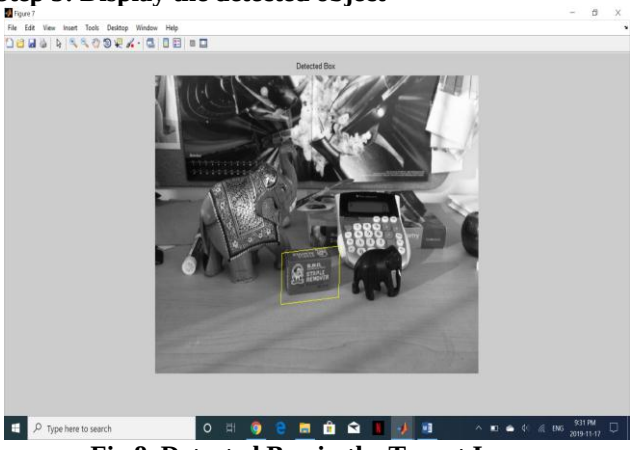

Fig 8. Detected Box in the Target Image

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Step 6: Detect another Object from the Target Image

Detect a second object by using the same steps as before.

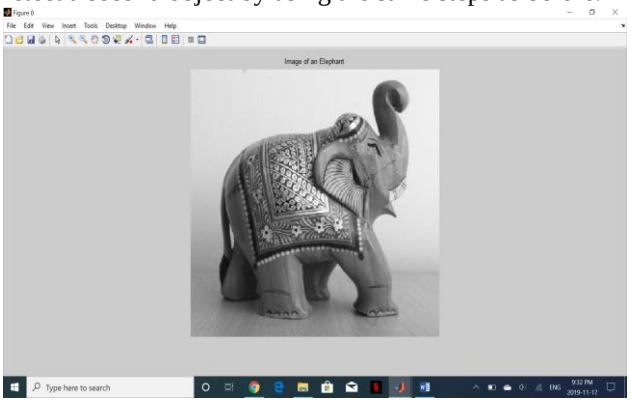

Fig 9. Image of an Elephant

Detecting and visualizing feature points.

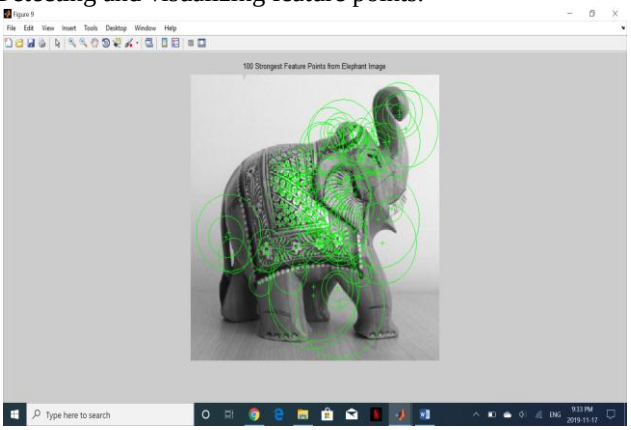

Fig 10. 100 Strongest feature points from Reference Image

Extract feature descriptors from the image.
Display putatively matched features.

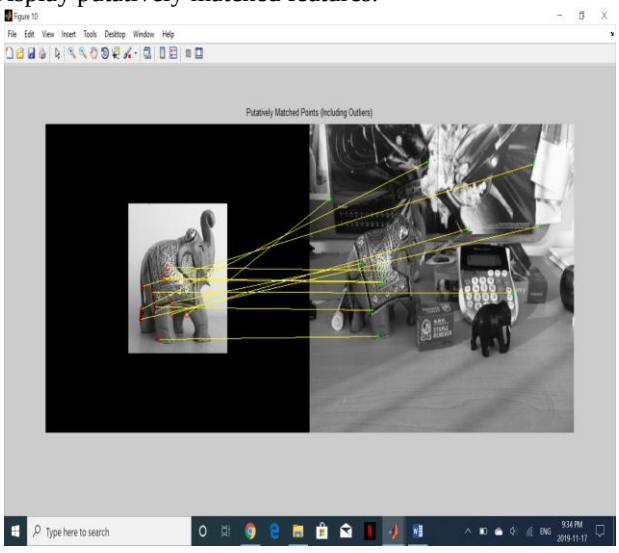

Fig 11. Matched Points (May Include Outliers)

Estimating Geometric Transformation and Eliminating Outliers.

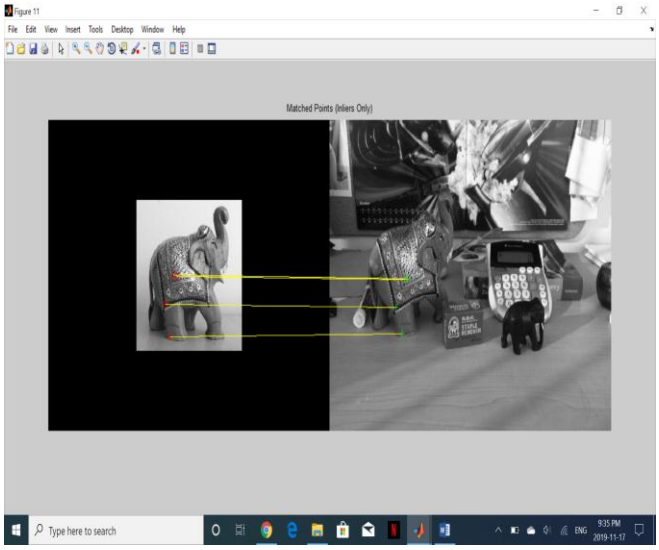

Fig 12. Matched points (Inliers only)

Display Both Objects.

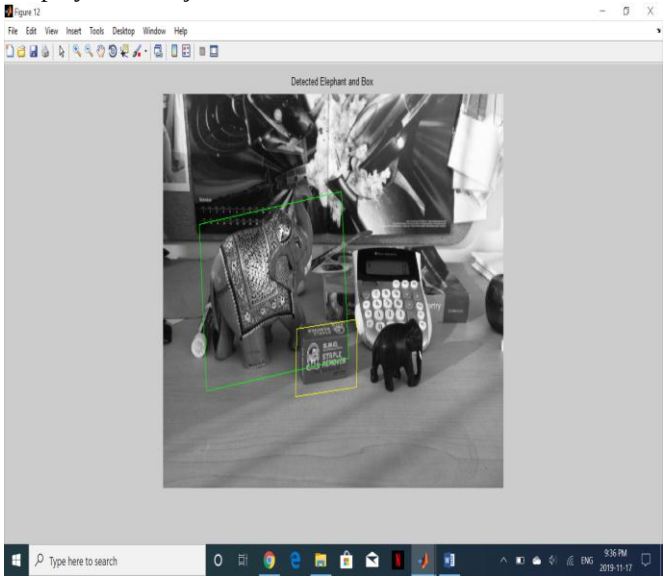

Fig 13. Detected Elephant and Box

4. RESULTS AND DISCUSSION

Table 1. Results

Steps	Result Obtained
1. Read images	At first the target and reference images were loaded.
2. Detect Feature Points	Firstly, 100 strongest feature points were extracted from the reference image. Then 300 strongest feature points were extracted from the target/scene image.
3. Extract Feature	After matching all the feature

Descriptors	point, lines were drawn to the matched points. (These matched point may include outliers.)
4. Locate the Object in the Scene Using Putative Matches	The specified object in the scene was then located using only putative matches. This also helped remove outliers in the matched points.
5.Display the detected object	The matched points were finally transformed to the target image, which in turn showed the location of the reference image in the target image. Features were matched in the images and the specified object was detected in the scene.
6. Detect another object	Likewise, the second object was detected using the same steps as mentioned above.

5. CONCLUSION

Since the detection results acquired using any technique basically relies upon the type of input image, information of the image as well as the level of noise in an image, it is inappropriate to expect one strategy to be superior to the next. For the work demonstrated in this paper, Point Feature Matching method proved to be quite effective in detecting the specified objects in the cluttered scene and it also gave good detection results. As new innovation develops, more sophisticated techniques can be used for object detection in such a way that they deal with occlusions and luminous effects and are capable of providing better results. In the future, algorithmic techniques can likewise be improved if we work upon reducing their complexities.

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Temperature Excursion Management in Cold Supply Chain of Pharmaceutical Products

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Abstract:

India's cold chain industry is currently estimated to be worth $8 million which is composed of a combination of refrigerated transportation and surface storage mechanism. Managing the quality of pharmaceutical product during cold supply chain and the distribution process is a complex challenges for the pharmaceutical industry. The Indian cold chain market is anticipated to be more organized in setting up the cold chain facilities across India in coming years. The temperature should be maintained for the storage and transportation of temperature sensitive goods during the entire product life cycle right from the receipt of raw material and its manufacturing till distribution. There is a need of special handling and monitoring of the refrigerated product to ensure the proper packaging configuration and transit methods meet the predetermined cold chain criteria. Improper handling might deteriorate the quality of the product thereby lowering the therapeutic properties. The study focuses on a system based quality management in pharmaceutical operations, quality assurance and enhancement, concerted efforts, concepts, consequences and handling mechanism to ensure product quality.

Keywords:

Temperature excursion, distribution, pharmaceutical products, transportation

1. INTRODUCTION

A cold chain can be defined as distribution and supply of those therauepetic drugs which are stored under specific temperature range. The product stored are those that undergo end to end transit to transport a sensitive product like pharmaceutical drugs and biologics materials. The proper maintenance, control and handling of such products is extremely important in pharmaceutical manufacturing and distribution. A cold chain maintains and preserves the usability of products, mainly pharmaceutical products which require constant refrigeration. Certain other biosimilar, therapeutic drugs also come under the ambit of cold chain. The cold supply chain distribution method also focusses on not only the packaging of insulated containers having appropriate quantity of refrigerant but also on the transportation and storage handling of the drug product. All the essential elements should be properly analyzed, understood and tested before the distribution process is carried on. This will ensure that the quality of the product and patient safety is not compromised.

The human negligence and the improper management of the environmental controlled parameter during storage and handling impact the quality of the drugs distributed. Such uncalled and uncontrolled situations call for lower efficacy and deteriorated drug quality resulting temperature excursion. Failures to store the medicines as per the set standards of manufacturer can invalidate the safety of medicines which are stored in large quantities and are temperature liable. This can cause an unavoidable waste to a large expense.

Objective: The study focuses to find out the various facets of temperature excursion in the transportation and distribution in cold supply chain of pharmaceutical drugs.

Methodology: The paper is based on the secondary database and exploratory study through various articles, journals and news portals.

1. Facets of Temperature excursion:

The pharmaceutical cold chain and managing transportation of temperature controlled products is one of the major complex challenge. Continuous growth has been observed in the temperature controlled products indicating tremendous growth globally. With the introduction of Goods Distribution Practices (GDP's) there has been clear demarcation for the storage of biologics and other products at a definite temperature. Use of refrigerants, insulated containers and temperature monitoring electronics are some logistics practices employed to monitor products when shipped. The pharma manufactures still follow the traditional practices of analyzing the environmental conditions and documenting the temperature stability of their product. But because of the safety regulators guidelines to be strictly adhered the pharma manufactures are now focusing to provide better quality assurance.

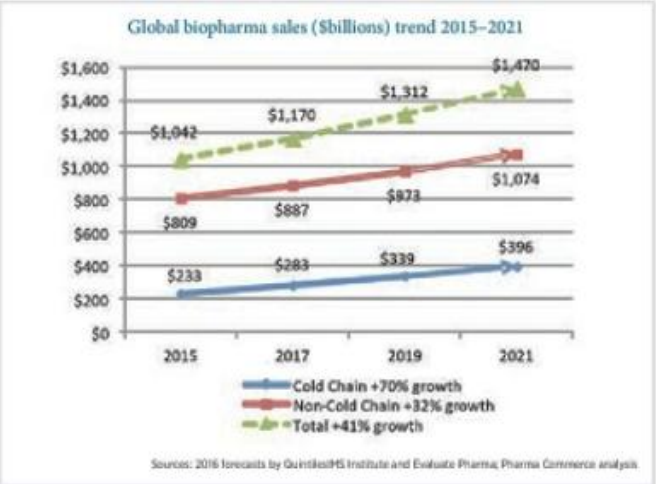

Fig. 1. Sales volume of cold chain products continues to grow at double the rate of non-cold chain

a. Handling temperature excursion:

The pharmaceutical manufactures dealing with the sensitive products having shorter shelf life, greater sensitivity needs to maintain the specified range of temperature to avoid the uncontrolled situations. If temperature range exceeds from the specified range the product experiences temperature excursion. If so is the case then the manufacturer should immediately follow the rules shown below and quick action should be taken to prevent the waste.

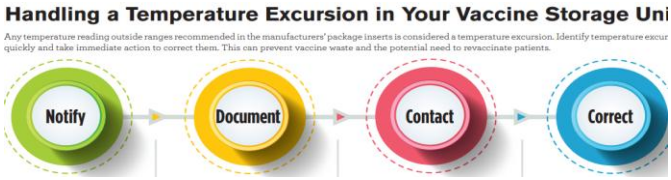

Fig: 2 Source :US Department of health and Human Sciences

The products which are temperature sensitive can deteriorate the active ingredients and decrease the content through transformation of degraded components by receiving thermal energy. The uncontrolled storage and distribution temperatures of the drug may lead to harmful side effect when administered by the customer.

b. Stability of pharmaceutical preparation:

The stability testing during pharmaceutical preparation is carried out to provide an evidence on the quality of drug substance over a time period where the identity, strength, quality and purity of the drug is not affected. The quality of drug varies with time under changing environmental factors and so the shelf life of the product is studied during stability testing .The manufacturer must provide the information on real time stability studies, chemical and microbial attributes along with the expiry date and storage condition which were previously projected. Within the specified limit of shelf life, lifesaving drug must possess the ability of retaining its physical, chemical therauepetic properties. Following the proper current regularity guidelines and understanding the changing climatic zones drug stability information should be sought, collected and analyzed thereby preserving its microbiological attributes.

c. Storage conditions and limitations:

For a pharmaceutical drug the shelf life always relates to its storage conditions along with its compliance with labelling. There are various types of storage conditions which are required for pharmaceutical drugs. The drug substances are stored in different required conditions and temperatures are set standards by manufacturers. There are certain specific chemicals and solutions which are required to be stored in specific conditions only. So, most of the drug substance experimental studies on storage conditions are performed at room temperature. 20 -25 C temperature is considered room temperature for pharmaceutical drugs. The excipients and APIs are stored under the controlled temperature. The 8 to 15 C temperature maintenance in the warehouses is known as the cold storage conditions. Some substances which are likely to degrade at room temperature are stored at specified storage condition maintaining the efficacy of the drugs. The storage conditions needs to be precisely indicated as a label:

- The drug substance to be stored under normal storage condition.
- The drug substances to be stored between 2 and 8 0C (under refrigeration, no freezing).
- Storage below 8 0C (under refrigeration).
- Storing the product/substance between -5 and -200 C (in a freezer).
- Store the product/substance below -18 0C (in a deep freezer).

2. Reasons for temperature excursion:

Temperature monitoring at every phase during cold supply, not only in manufacturing stage but also at all stages of storage and transport which is of utmost importance for the products which are temperature sensitive. The products which are exposed to higher temperature or moisture levels are prone to lose its efficacy. The integrity of cold chain is threatened during transportation by many risks, not limited to natural disasters, handovers and unforeseen delays. The EU GDP guideline explains that the drugs are expected to be held at right condition at all time throughout storage and transport. The quality needs to be ensured at all stages by the manufacturer and distributor. The inadequate air handling unit (AHU) are required to maintain the specific temperature, rupture of air duct, breakdown of power failure, insufficient cooling effect, the unexpected delay of transportation, environmental conditions, product if kept on heating zones of airports or yards also defunct the efficacy

of the products and are also some reasons for temperature excursion.

3. Transportation of cold supply chain products:

The lifesaving medication when transporting is arguably more important than manufacturing them. Shipping these products require extra level of care. Precautions are necessary like temperature control, environmental conditions and safeguarding drugs against adulteration. Many pharmaceuticals especially, controlled substances are highly covered because mismanagement can cause counterfeiting of drugs. The required temperature must be maintained for pharmaceutical safety and efficacy. The method and the time of transportation, the local seasonal temperature, size and control requirement of the loads should all be considered while the distribution of the cold supply products. For vehicles of little volumes of virus chain products protected compartment with ice packs must be utilized. Damaged products while freezing must not come in direct contact with these ice packs. Therefore the containers should have separate compartment. Transporting and distribution should be continuously monitored using data logging system. The data recording of temperature maintained is retrieved through these data logging devices shipped with the packed product. The thermostatic temperature on the transport vehicle should be set on specific requirement for recording and time to time tracking. The recorded data should be available for review. For larger volume of good to be supplied must be shipped with refrigerated transport system, specifically when the transit may prolong.

4. Controlled Temperature Storage:

The temperature controlled logistics specializes in storage, preservation and transportation of those products which are sensitive to atmospheric conditions and needs to be maintained at certain temperature. This is imperative for many pharmaceutical products as the spoiled dugs can have serious consequences on health. The elevated temperature can affect the chemical stability of the medicine and can later its physical properties. And so these products are transported via temperature controlled supply chain. There are certain considerations for a controlled temperature storage which need to be maintained while transportation:

- The acceptable temperature and humidity range.
- Margin of error of temperature.
- Backup for temperature controls.
- The layout of storage unit and airflow.
- Potential areas of risks and touch points.
- External temperature logging and data tracking.

Above all the temperature mapping to determine the temperature distribution under extremes of external temperature should be maintained in warehouses. All the conditions must be assured by all the parties including manufacturer, shipper and wholesaler**.**

5. Standards and Regulations for cold supply chain:

The companies operating within the pharmaceutical cold chain must be aware of all the set rules and standards for distribution of products in the market. These regulations can differ from country to country following it makes it complex. Specifically, manufacturer of products have direct control over the correct storage and handling of the product from the start of production till dispatch. Specific compliance is required for an effective cold supply chain structure and governance strategy are based upon combination of regularity requirements defined by corresponding regulatory bodies such as FDA, EMO, WHO, Health Canada etc.Goods Distribution Practice (GDP) is a part of quality system of warehouse and distribution process assuring that products are continuously stored, transported and handled with the set standards as required. However there are various other set protocols set to be followed at various levels during transportation, packaging and distribution of temperature sensitive products.

6. Cold Supply Chain Management Pattern:

a. **Importance of regulation is on rise:** For years the Pharma counterfeiting incidents are prompting factors for government to tighten regulations on production and supply chain. Harmonizing regulations and establishing preventive measures are some issues for pharmaceutical industries. Earlier the pharmaceutical mandates products were maintained within the manufacturer storage guidelines. The European Union guidelines (EU) established in November 2013 on goods Distribution Practices for medicinal products came into effect of extending temperature requirement to transportation. About 80 percent of pharma product now require temperature controlled transportation.

b. **Increased logistics outsourcing:** For a given cost and time to manage an efficient, and reliable cold chain, the manufactures are looking forward to outsourcing. Most of the pharmaceutical companies have turned to adopt custom design solutions and just in time packaging deliveries. The formulation of third party logistics aims to make necessary changes and investment in technology, infrastructure and system drive continuous improvement to gain a competitive market edge. Specialized in Automated Search and Retrieval System (SASR) and in- situ X-ray verification of sensitive products are evolving demand of cold supply chain.

c. **Training of professionals:** Learning how to maintain temperature throughout the entire cold chain and meet the GDP compliance has been a complex task for the professionals. An Intricate knowledge on all aspects of cold supply chain, validation and technical expertise are a must for handling the sensitive products.

d. Active and Passive Shippers: Passive thermal system are typically using phase change material such as dry ice, insulated with polystyrene, polyurethane or vacuum insulated panels. With this type of configuration gel packs or similar material are used to maintain the desired temperature. On the other hand the active thermal systems are powered by electricity or batteries and are considered to be more secure during transportation. These system use mechanical energy source to control and maintain proper temperature. As a result the design helps to reduce the risk by maintain regulatory compliance. The active shippers are adding cost and higher temperature accuracy than passive shippers are most basic and cost effective.

2. CONCLUSION

For keeping up a cold supply chain there are successful ways which provide computerized correspondence and information accumulation. This creates a platform which links all data stored in devices to an application and gathers real-time temperature of the products currently in transit and suggests corrective what's more, preventive activities, and connects the authentic exhibition of a particular bit of bundling hardware to any stamped shipment, all simultaneously holding fast to the major worldwide administrative authorities. Manufacturers must make it sure that the drug dispenses to the customers with right quality. In India, since manufacturers don't support power over the multi layered circulation framework, the supply chain manufacturing procedure keeps on being troublesome and costly. The manufacturers are progressively understanding the significance of a viable conveyance framework in the entire process. Thus ensuring an efficient cold supply chain is a crucial step for commercialization and distribution throughout supply chain the attention should be put on training, SOP's on cold chain processes, documentation, quality assurance and its maintenance, storage conditions, temperature profiles and quality packaging methods which needs to be periodically controlled and maintained.

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Distribution System Reconfiguration for loss minimization and voltage profile enhancement by using Discrete – improved binary particle swarm optimization algorithm

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Abstract:

Distribution system reconfiguration is done by altering the open / close position of two kinds of switches: usually open tie switches and sectionalizing switches usually closed. Its main purpose is restoration of supply via other route to improve reliability, sometimes for load balancing by relieving overloads. Feeder reconfiguration is very good alternative to reduce power losses and improve voltage profile to improve overall performance. Distribution system reconfiguration is a very cost effective way to reduce the distribution system power losses, enhance voltage profile and system reliability. This paper presents application of novel Discrete - improved binary particle swarm optimization (D-IBPSO) algorithm for distribution system reconfiguration for minimization of real power loss and improvement of voltage profile. The algorithm is implemented to a 16-bus, 33-bus system and a 69-bus system considering different loading conditions. The simulation results indicate that the suggested technique can accomplish optimal reconfiguration and significantly reduce power losses on the supply scheme and enhance the voltage profile.

Index Terms:

D-IBPSO, distribution system optimization, loss minimization, network reconfiguration

1. INTRODUCTION

Electricity is produced, transported and delivered to end customers in an electrical power system. The distribution network receives power from the transmission system and provides low voltage levels to customers. Residential, commercial and industrial are different kinds of consumer-related loads. The load on the power system changes according to consumer requirement throughout the day and is never continuous. Radial and ring main distribution structures are two kinds of distribution network. The feeders emerging from a single substation is the radial distribution structure, whereas the feeders in a circle or ring shape are ring main structure. The major drawback of radial systems is that it cannot feed the load in the event of power supply failure and is therefore less reliable. Each user is delivered power via two feeders or paths in the ring main scheme. This sort of scheme is more reliable and can be readily retained by isolating one segment and linking supply via another path to the loads. Radial distribution structures are therefore designed with sectionalization and tie switches to enhance reliability so that the structure can be reconfigured. Reconfiguring is the way to change a network framework by changing the position of ON / OFF switches.

2. RECONFIGURATION OF DISTRIBUTION SYSTEM

Merlin and Back [1] first revealed the reconfiguration technique to decrease losses in the distribution network. Several algorithms have been designed to fix this issue since then. These algorithms are mostly focused on methods, heuristic techniques, meta-heuristic and artificial intelligence. In this study, they suggested a heuristic algorithm to find out the minimum loss configuration of switches (setup) as a mixed non-linear optimization problem. They used a discreet branch and bound method; i.e. first, all switches are closed to establish a meshed network. These switches are then opened consecutively to maintain radial setup. It was suggested by Civanlar et al. [2] and Baran et al. [5] to use other heuristic approaches depending on the method of branch swap to identify the losses. The Merlin and Back technique has been enhanced by Shirmomohammadi and Hong [3]. As a consequence, it has the main advantages of this technique, convergence to the optimum or close optimum alternative, and independence of the final solution from the network switches ' original status. Simultaneously, this technique prevents all of Merlin and Back's significant drawbacks. Goswami and Basu [4] suggested an algorithm focused on the optimum flow structure obtained through a circuit by removing a switch usually accessed by opening a closed switch in the radial distribution system. To minimize the

power losses and balance the loads on feeders, Baran and Wu [5] provided a heuristic reconfiguration technique centered on branch swap. Two approximate load flow techniques for radial structured network with varying degrees of precision are used to help in the search. They are easy technique of power flow and updating the power flow method back and forward. Due to complex arrangements in larger systems and converging to local optimum solutions, the global optimum convergence is not ensured. The technique is very time consuming. Gohokar et al. [6] provided a network structure strategy using one-loop optimization centered on the highest voltage decrease for open switch configuration. Nara et al. [7] introduced the genetic algorithm to reconfigure an AI-based methods-based radial allocation scheme with minimal failure. Lin et al. [8], Zhu [9], Delbem et al. [10], Prasad et al. [11], Mendoza et al. [12], Enacheanu et al. [13] pursue various GA variations and modifications. Su et al. [14] presented to fix the issue of optimum distribution system reconfiguration to minimize the power loss, the ant colony optimization (ACO) algorithm was implemented. Lin et al. [15] implemented the immune algorithm to reconfigure a radial supply scheme for to reduce the power loss and to balance the load on distribution lines or feeders. Hsiao and Chen [16] implemented a multi-objective distribution system reconfiguration system by using evolutionary programming. Das [17] proposed an intrusive strategy with a heuristic rules framework for multi-objective feeder reconfiguration. Falaghi et al. [18] presented a methodology to reconfigure the radial distribution system by considering the distributed generation (DG). A fuzzy method is used for multi-objective variables. In order to create a multi-objective fuzzy system for optimal allocation scheme scheduling, the multi-objective tabu search algorithm of Ramirez-Rosado and Dominguez-Navarro [19] was provided. Ahuja et al. [20] suggested an artificial fusion model on the basis of immune system and optimization of ant colony to reconfigure the radial distribution system as a many objective task. In response to the issue of voltage control and energy loss reduction on distribution system, Augugugliaro et al. [21] employed a wide range of goal heuristic optimizations. The Particle Swarm Optimization (PSO) is influenced by a herd of migrating birds social conduct attempting to achieve an unidentified target. Each alternative in PSO is a bird in the herd and is called a particle. A particle is similar to a GAs chromosome. Unlike GAs, the PSO's evolutionary process does not generate fresh parent birds. Instead, the population's birds only develop their social behavior and their motion toward a target appropriately. Each bird appears in a particular direction, and then they recognize the bird in the finest place when they communicate together. Thus, each bird flies towards the finest bird using a speed depending on its present situation. Each bird then explores the search space from its fresh local place and performs the cycle until a required location is reached by the herd. Tamer M. Khalil and Alexander V. Gorpinich [22] used for loss minimization selective particle swarm optimization (SPSO). The binary particle swarm Optimization (BPSO) algorithm is a simple amendment. The algorithm's search space is a collection of branches (switches) that are usually closed or opened, search space can be different for distinct sizes. The reconfiguration issue solving method is organized into two phases. First, discover search area after all the switches are closed and then, use SPSO to locate open switches. The method described is implemented to a scheme with 33 buses and a scheme with 69 buses. To show the performance of the suggested algorithm, the outcomes acquired through SPSO are contrasted with some prior techniques.

The PSO search procedure depends on the past best particle solution and the best solution for updating particle data in the population. This implies that the particles share the best data and guide the particles towards the goal. Due to the PSO-designed search system, the probability of dropping into a local PSO algorithm alternative may be decreased. The PSO algorithm is easy and simple to execute. PSO can thus be a strong tool for helping and speeding up the decision-making method in finding the appropriate schedule for distribution system reconfiguration.

Problems with distribution system reconfiguration are non-linear problems with discrete optimization. However, the typical PSO is designed for continuous feature optimization issues; it isn't designed for discreet function optimisation problems.

While the BPSO solution to the discreet optimization problems can be used, problems persist when the BPSO application is applied to distribution system reconfiguration problems. There are number of tie-switches in the distribution system reconfiguration issues. In distribution systems, selecting randomly the locations of these tie-switches may possibly result in non-supply to some of the loads and or non-radial structure. Chang et al. [23], BPSO is presented to resolve the problem of distribution system reconfiguration and the method proposed prevented the problem of inappropriate tie-switch numbers.

This wok proposes a more practicable discrete – improved binary PSO algorithm from typical PSO for distribution system reconfiguration instead of the BPSO used in [23]. This study has modified the technique suggested to make binary particle swarm optimisation for reconfiguration of distribution system depending on the features of the switch position and the shifting operator.

3. MATHEMATICAL MODELLING

As stated in equation (1), the power loss reduction problem is expressed mathematically.

$$P P_{loss} = \sum_{l=1}^{NL} k_l \; R_{jk} \left(\frac{P_j^2 + Q_j^2}{V_j^2} \right) \qquad (1)$$

Where,

l is the j-k lines branch number.

Vj is jth node voltage.

Pj and Qj are the real and the reactive power flow in branch l.

kl is the status of the branches.

kl = 1 if branch l is closed and

kl = 0 if the branch is open.

NL is the number of branches in the system.

The preceding limits are imposed on the designed distribution system reconfiguration algorithm.

a. Current limit for branch

In any branch *l*, the current should be less than the rated branch current.

This is articulated and provided mathematically in Equation (2).

$$|I_l| \leq I_{lmax}\ l \in NL \quad (2)$$

b. Voltage limits for bus

The voltage at each node i should be within the suggested limit. This is developed and presented in equation mathematically (3).

$$\mathbf{Vimin} \leq \mathbf{Vi} \leq \mathbf{Vimax}\ \mathbf{i} \in \mathbf{N} \quad (3)$$

c. Topological limitations

The topological limitation is to guarantee that the distribution network is radially arranged.

- If the allocation scheme does not have separate nodes, the topological constraint will be encountered.

- No closed loops are available in the distribution system, i.e. radial distribution system structure.

4. DISCRETE – IMPROVED BINARY PARTICLE SWARM OPTIMIZATION (D-IBPSO)

In 1995, Eberhart and Kennedy developed the methodology of Particle Swarm Optimization (PSO). It is an algorithm of stochastic search influenced by flocking birds or social behavior in fish education. The PSO starts with a random-positioned search space population of particles. Each particle is a fitness-value problem-solving alternative. It will evaluate and optimize the fitness. Defines a speed that enables each particle's location and is changed in each iteration. Because of their optimal place and the greatest alternative that teams have ever encountered, particles are progressively moving towards the ideal solution. Furthermore, a restricted number of parameters must be adapted and a restricted reliance on the original values. The main advantage of the PSO is that it has to deal with a few parameters. Some of the PSO algorithm's parameters include particle size, search space size, particle size, termination criterion, and acceleration training factors or coefficients.

D-IBPSO algorithm for the distribution system reconfiguration

The D-IBPSO algorithm is created to reduce the actual energy loss in distribution schemes by reconfiguring the distribution system feeder. Using the following procedure, the D-IBPSO algorithm is implemented:

Step 1: Initialization of the parameters

Read the distribution scheme information. Initialize the parameters for the binary D-IBPSO. Initialize the location of the particles. Use the equation (4) to initialize the particle velocity.

$$\mathbf{velocity}(\mathbf{i}, \mathbf{j}) = \mathbf{vmin} + (\mathbf{vmax} - \mathbf{vmin}) * \mathbf{ran} \quad (4)$$

Step 2: Find the personal best position of the each particle. In this situation, the original location of particles is presumed to be the best place of particles. Then run the load flow depending on the personal best place of the particles and calculate the power loss.

Step 3: Discover the best global particle location provided in Step 2 from the best particle location set. In this scenario particle location with lowest power loss is the best global particle location.

Step 4: Calculate the distribution networks bus incidence matrix. This assists to find whether or not the structure of the network is radial. Initiate the method of binary D-IBPSO iteration and put the counter t to 1.

Step 5: Check the limitations of the topology. This phase guarantees that only viable distribution network topologies evaluate the power loss.

Step 6: Use the Newton-Raphson method to calculate the power loss in the given system.

Step 7: Revise the particles ' personal best using equation (5).

$$Pbest_i^{t+1} = \begin{cases} Pbest_i^{t+1} \\ Xi_i^{t+1} \end{cases} \begin{matrix} if\ fitness_i^{t+1} \geq fitness\ Pbest_i^t \\ otherwise \end{matrix} \quad (5)$$

Step 8: Revise the global best of the particle herd using equation (6).

$$Gbest^{t+1} = \begin{cases} Gbest^t \\ Pbest_i^{t+1} \end{cases} \begin{matrix} if\ fitness_{Pbest_i}^{t+1} \geq fitness_{Gbest}^t \\ otherwise \end{matrix} \quad (6)$$

Step 9: Determine the weight of inertia and update the speed of all particles with the help of equation (7).

$$\omega = \omega_{max} - \left(\frac{\omega_{max} - \omega_{max}}{t_{max}}\right) * t \quad (7)$$

Step 10: Update the position of the particles by using equation (8).

$$\mathbf{xi^k} = \begin{cases} \mathbf{1\ if\ r} < \mathrm{sig}(\mathbf{vi^k}) \\ \mathbf{0\ if\ r} \geq \mathrm{sig}(\mathbf{vi^k}) \end{cases} \quad (8)$$

Step 11: Increase count of the iteration for D-IBPSO search method and repeat step 5 to step 10 until the termination criterion has been reached.

Step 12: Output the search outcomes like best global alternative (ideal network structure), its respective fitness score (minimal energy loss) and the D-IBPSO algorithm's convergence rate.

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5. IMPLEMENTATION OF D-IBPSO ALGORITHM FOR THE DISTRIBUTION SYSTEM RECONFIGURATION

Three distribution systems of IEEE 16, 33 and 69 bus are used to assess the performance and effectiveness of the D-IBPSO algorithm. The assessment is done on the basis of power loss, voltage magnitude at bus and the topology of the distribution system. Comparison with the literature results is made for the suggested D-IBPSO algorithm.

The developed binary D-IBPSO algorithm's predefined parameters are as shown below.

D-IBPSO parameters

$W_{min} = 0.4, W_{max} = 0.9$, Coefficient of acceleration (c1 and c2) = 2, Maximum speed or velocity $V_{max} = 4$

Case Study 1: IEEE 16 bus system

The 16-bus distribution scheme is a radial distribution network of 12.66 kV, with base MVA 100. It comprises of three primary feeders, 13 set loads, seven shunt condensers, and 16 branches. Out of 16 branches 13 are sectionalizers , and three are tie lines. The complete actual power demands and reactive power requirements are 28700 kW and 17300 kVAR respectively. The technique of Newton-Raphson calculates the outcomes of the load flow in the MATLAB.

Table 1 provides a comparison of the outcxomes of the 16-bus distribution scheme with the D-IBPSO algorithm before and after feeder reconfiguration. Figure 1 provides the voltage profile in the distribution scheme.

Table 1: Results of the 16 bus system

Results	Base Reconfiguration	Optimal Reconfiguration
Open switches	14, 15, 16	7, 8, 16
P_{Loss} (kW)	514.02	468.33
% P_{Loss} reduction	-	8.89
V*min* (p.u.)	0.968	0.970

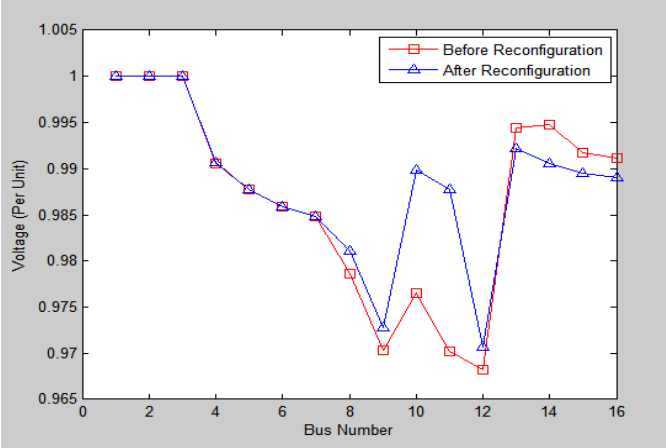

Figure 1: Voltage magnitude for the 16 bus system

Table 2: Results for the D-IBPSO compared with other algorithms for 16 bus system

Algorithm used		D-IBPSO proposed	Refined GA [24]	ACO [25]	SEM [26]
Base Reconfiguration	Open switches	14, 15, 16	14, 15, 16	14, 15, 16	14, 15, 16
	P_{Loss} (kW)	514.02	511.4	511.4	-
Optimal Reconfiguration	Open switches	7, 8, 16	7, 8, 16	7, 8, 16	7, 8, 16
	P_{Loss} (kW)	468.33	466.1	466.1	466.13
	% P_{Loss} reduction	8.89	8.85	8.85	-

Table 3: Results of the D-IBPSO for the 16 bus system at various load conditions

% Load		50%	75%	100%	125%
Base Reconfiguration	Open switches	14, 15, 16	14, 15, 16	14, 15, 16	14, 15, 16
	P_{Loss} (kW)	139.10	282.09	514.02	838.49
	Minimum voltage (p.u.)	0.991	0.980	0.968	0.955
Optimal Reconfiguration	Open switches	7, 8, 16	7, 8, 16	7, 8, 16	7, 8, 16
	Power loss (kW)	125.14	256.03	468.33	764.66
	V*min* (p.u.)	0.992	0.982	0.971	0.959
	% P_{Loss} reduction	10.03	9.23	8.89	8.81

Case Study 2: IEEE 33 bus system

Table 4: Results of the 33 bus system

Results	Base Reconfiguration	Optimal Reconfiguration
Open switches	33, 34, 35, 36, 37	7, 9, 14, 32, 37
P_{Loss} (kW)	208.43	138.92
% P_{Loss} reduction	-	33.35
V*min* (p.u.)	0.910	0.942

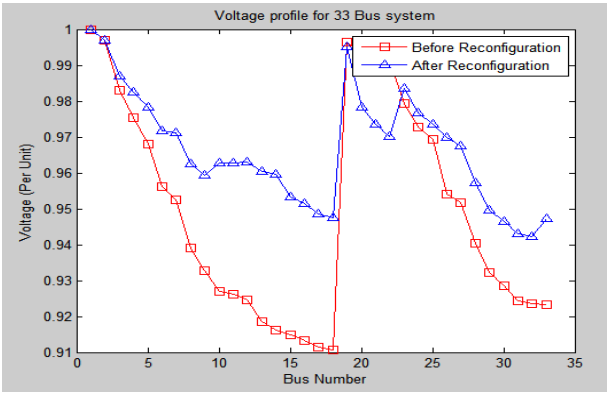

Figure 2: Voltage magnitude for the 33 bus system

Table 5: Results for the D-IBPSO compared with other algorithms for 33 bus system

Algorithm used		D-IBPSO proposed	SSOM [27]	Hybrid PSO [28]
Base Reconfiguration	Open switches	33, 34, 35, 36, 37	33, 34, 35, 36, 37	33, 34, 35, 36, 37
	P_{LOSS} (kW)	208.43	202.05	202.67
	V*min* (p.u.)	0.910	0.913	0.913
Optimal Reconfiguration	Open switches	7, 9, 14, 32, 37	7, 9, 14, 32, 37	7, 9, 14, 32, 37
	P_{LOSS} (kW)	138.92	139.21	139.53
	V*min* (p.u.)	0.942	0.937	0.938
	% P_{LOSS} reduction	33.35	31.10	31.14

Table 6: Results of the D-IBPSO for the 33 bus system at various load conditions

% Load		50%	75%	100%	125%
Base Reconfiguration	Open switches	33, 34, 35, 36, 37	33, 34, 35, 36, 37	33, 34, 35, 36, 37	33, 34, 35, 36, 37
	P_{LOSS} (kW)	49.08	113.01	208.45	338.72
	V*min* (p.u.)	0.957	0.934	0.910	0.885
Optimal Reconfiguration	Open switches	7, 9, 14, 32, 37	7, 9, 14, 32, 37	7, 9, 14, 32, 37	7, 9, 14, 32, 37
	P_{LOSS} (kW)	33.59	76.36	138.92	222.31
	V*min* (p.u.)	0.971	0.957	0.942	0.926
	% P_{LOSS} reduction	31.55	32.42	33.35	34.36

Case Study 3: IEEE 69 bus system

Table 7: Results of the 33 bus system

Results	Base Reconfiguration	Optimal Reconfiguration
Open switches	69,70,71,72,73	14,56,61,69,70
P_{LOSS} (kW)	224.98	98.59
% P_{LOSS} reduction	-	56.14
V*min* (p.u.)	0.909	0.949

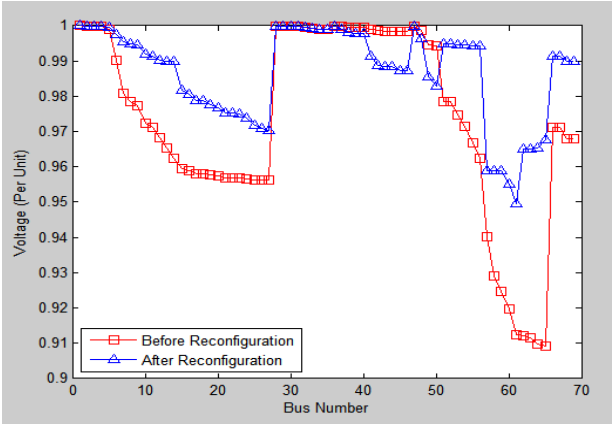

Figure 3: Voltage profile of the 69-bus system

Table 8: Results for the D-IBPSO compared with other algorithms for 69 bus system

Algorithm used		D-IBPSO proposed	Fuzzy multi-objective approach [29]	HAS [30]
Base Reconfiguration	Open switches	69,70,71, 72,73	69,70,71, 72,73	69,70,71, 72,73
	P_{LOSS} (kW)	224.98	224.95	225
	V*min* (p.u.)	0.909 (65)	0.909 (65)	0.909 (65)
Optimal Reconfiguration	Open switches	14,56,61, 69,70	14,56,61, 69,70	14,56,61, 69,70
	P_{LOSS} (kW)	98.59	99.59	99.35
	V*min* (p.u.)	0.949 (61)	0.948 (63)	0.942 (63)
	% P_{LOSS} reduction	56.14	55.72	55.85

Table 9: Results of the D-IBPSO for the 69 bus system at various load conditions

% Load		50%	75%	100%	125%
Base Reconfiguration	Tie switches	69,70,71,72,73	69,70,71,72,73	69,70,71,72,73	69,70,71,72,73
	Power loss (kW)	51.60	121.01	224.98	369.02
	Minimum voltage (p.u.)	0.956	0.933	0.909	0.883
Optimal Reconfiguration	Tie switches	14,58,61,69,7	14,58,61,69,7	14,58,61,69,7	14,58,61,69,7
	Power loss (kW)	23.60	54.25	98.59	157.61

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	Minimum voltage (p.u.)	0.975	0.962	0.949	0.936
	Power loss reduction (%)	54.24	55.16	56.17	57.28

6. RESULTS

D-IBPSO optimization algorithm has been developed in this paper to solve the problem of reconfiguration of the distribution scheme. The problem of distribution system reconfiguration was intended at minimizing the energy loss in distribution systems. To check the performance and effectiveness of the designed D-IBPSO algorithm, the IEEE 16, 33, and 69 bus distribution systems were used. The simulation outcome reveals that the D-IBPSO algorithm created is effective in addressing the issue of reconfiguration. As the load on the power system is variable, the losses and ideal solution for different load circumstances are also found.

Results following the comparison research verify that the D-IBPSO algorithm developed is consistent with the literature techniques present. For the 16 bus system, the reduced losses are close to 9%. The voltage is increased from 0.968 to 0.970 p.u. after reconfiguration of the distribution system. The losses are decreased for different operating (loading) circumstances in the case of 33 bus system after reconfiguration nearly 32 to 34 %. Voltage is increased from 0.910 to 0.942 p.u. after reconfiguration.

The power losses for 69 bus scheme are reduced by 55 to 56 % relative to the original setup with variation in loading conditions and the voltage profile is enhanced from 0.909 to 0.949.

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Annular Ring with Diamond Patch UWB Printed Monopole Antenna

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Abstract:

Annular Ring with Diamond Patch UWB Antenna has been presented, that produces large bandwidth. This configuration shows the bandwidth for VSWR = 2, or for corresponding S_{11} of 1.4GHz - 11 GHz, which includes UWB. This proposed configuration shows, approximately, Omni-directional radiation pattern on azimuthal plane for the entire range of frequency band. The measured and simulated results are shown, they promise for agreeable similarity. The impedance bandwidth ratio for presented antenna is achieved better than 7.85: 1 for S_{11} < -9.6 dB. This antenna combines two resonators, i.e. annular ring and diamond shaped patch, within FR4 substrate of dimension 80mm x 80mm. This low profile compact antenna can be very useful for many embedded systems

Index Terms:

Annular ring patch, Diamond patch, Multi-resonating antenna, Printed Monopole Antenna, Ultra wideband, Wideband

1. INTRODUCTION

In present day, the applications under wireless communications have been increased. The wireless communication system requires high data rate transfer. To support high data rate, antenna plays vital role, it must be broadband. For implementing broadband antenna either multi-resonating or multi-mode antenna can be used [1-2]. Therefore, requirement for multi-resonating antennas, that is antenna which have larger bandwidth and smaller area, is tremendously increasing. All these are showing broad/ultra wide band characteristic and they are working on multi-mode principle; whereas multi-resonating can also provide the broadband/ultra wide band characteristics [3-7].

In the presented paper, a multi-resonating printed monopole antenna(MPMA) is planned, leading to a new configuration. This configuration of MPMA consist of a diamond which is enclosed by a ring and out of the four vertices of the diamond shaped radiator, two vertices are overlapped or merged with the ring and remaining two edges are connected to the ring via thin strip of conducting material. The proposed antenna has been analyzed for the parameters like parameters like gain, efficiency, impedance BW, and radiation patterns. This MPMA Antenna has numerous applications such as, the presented antenna can cover frequency bandwidth from 1.40 GHz to 11 GHz and beyond, so that all the presently available wireless communication systems can be included such as GPS, GSM1800, PCS1900, WCDMA / UMTS (3G), 2.45 /5.2 /5.8-GHz-ISM, U-NII, DECT, WLANs and UWB (3.1–10.6 GHz) [1-8].

2. DESIGN OF ANTENNA

The annular ring antenna with a diamond patch within it is shown in Fig. 1. The current vectors are spreading on the edges of the patch [3-4]. From this one can conclude that the performance is not reliant on the central part of the patch. Hence this central part of circular is cut, making it an annular ring. Annular ring resonates at lower frequency and to excite higher order modes at high frequency the diamond shape patch has been inserted within the annular ring which will excite the higher order modes [8]. Circular patch with radius of R1 is converted into annular ring with the radius of R2 selected for inner part, R2 decide the lower end frequency resonance. When difference of (R1—R2) is kept on decreasing then the impedance of feed point will be increasing and it is not easy to equal the 'fifty' Ohm line. A diamond shaped geometry is introduced inside the annular ring, that may deliver good match and provide considerable reduction of the size of the radiating patch at the same time it helps to excite the higher order modes. The presented antenna has 2 resonators, with sufficient bandwidth, to ensure the achievement of ultra wide bandwidth. The presented antenna geometry is developed in the laboratory with low priced glass epoxy (FR4) substrate with the loss tangent, tan δ =0.01, relative dielectric constant of $\in r$ = 4.3, and the thickness of the substrate is h=1.59 mm.

Diamond Patch within Annular Ring

Fig. 1 shows the geometry of presented antenna with physical dimension of size of 80 mm x 80 mm. The dimension of the proposed patch radiator is linked with lower end of frequency bandwidth. For this proposed antenna the outer radius R1 = 25 mm, inner radius R2 = 23 mm, which has been optimized with ring width of 2 mm.

The diamond shaped patch has been incorporated within annular ring with dimension of, long diagonal is 50 mm and short diagonal is of 30 mm. The feed, microstrip line, along with the lower edge of annular ring or the radiating antenna and partial ground plane, behaves as quarter wavelength transformer to match the impedance. For appropriate impedance matching between the patch and the microstrip line feed, is provided with feed-width=3 mm. The dimension of ground plane of 80 mm x 10 mm as partial ground plane on back side and the feed gap (= p) of microstrip line feed is optimized to be, as 0.5 mm. For maximum power transformation to the radiating patch from the microstrip line feed one may provide better coupling among both the radiating patches. Hence the bandwidth is enhanced.

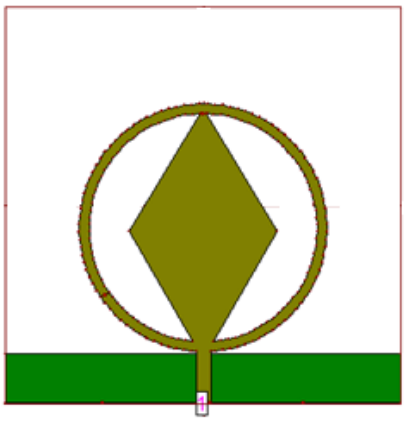


Fig. 1: Annular Ring combind with Diamond Patch

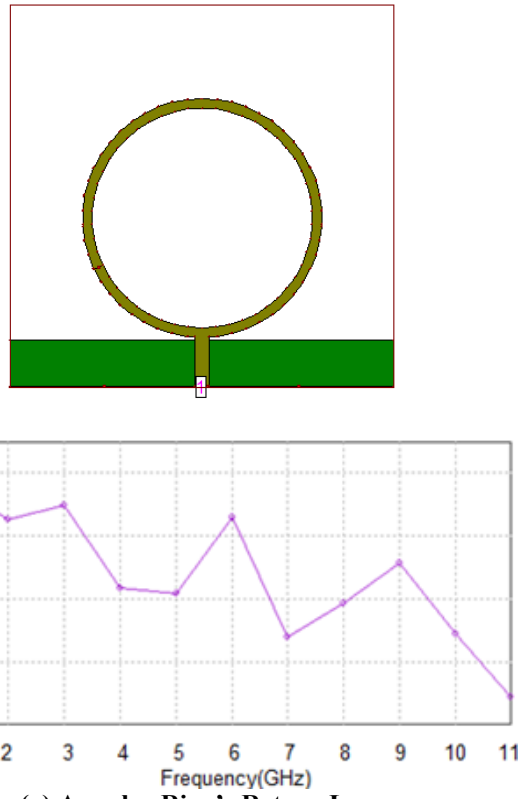
3. RESULTS AND DISCUSSION

The lower band edge frequency (f_L) for VSWR < 2 or S_{11} = -9.6 dB is given by:

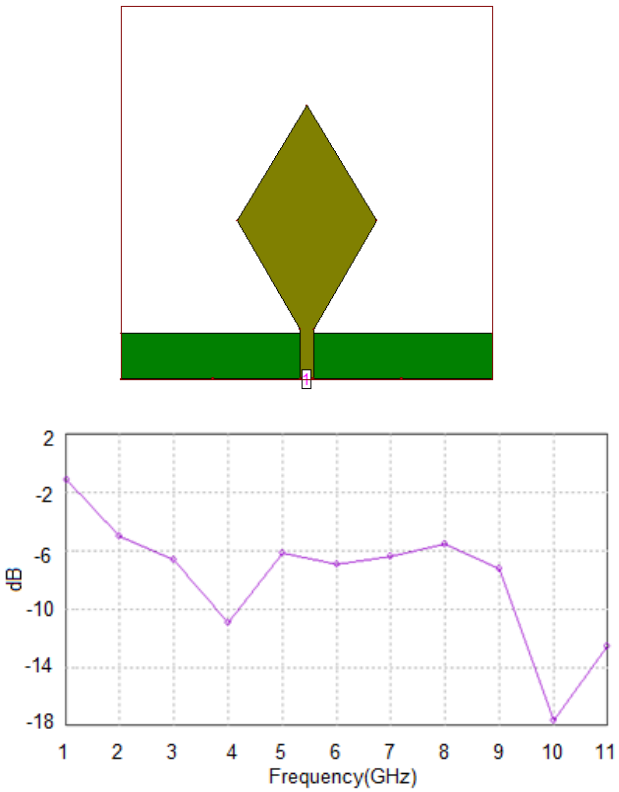
$$f_L = c / \lambda = [7.2 / (l + r + p)\, k\,] \quad \text{GHz} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

In given equation 1, length l, which decides lower edge frequency of printed antenna, in which r is the effective radius of an equivalent cylindrical monopole antenna and feed gap is specified by p and the correction factor k has been selected as 1.1 for the substrate glass epoxy [4-8]. All parameter l, r and p are in cm which produces f in GHz. Different parameters of designed antenna have been optimized to achieve impedance bandwidth in the span of 1.4 GHz to 11 GHz.

The characteristics of the presented antenna have been simulated by using IE3D software [9]. Different geometries and corresponding return losses S_{11} are shown in fig.2. The optimized configuration is fabricated and the photograph is shown in fig. 3.



(a) Annular Ring's Return Loss



(b) Diamond's Return Loss

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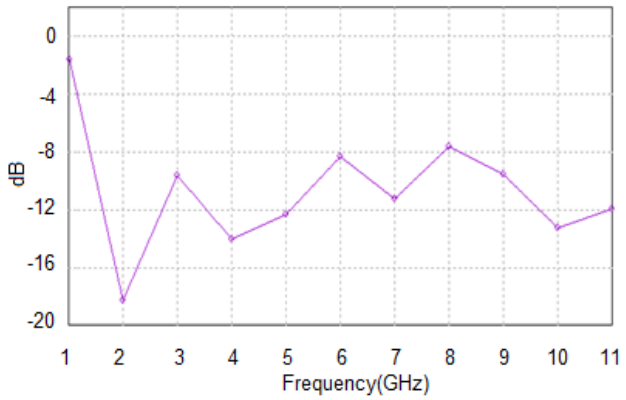
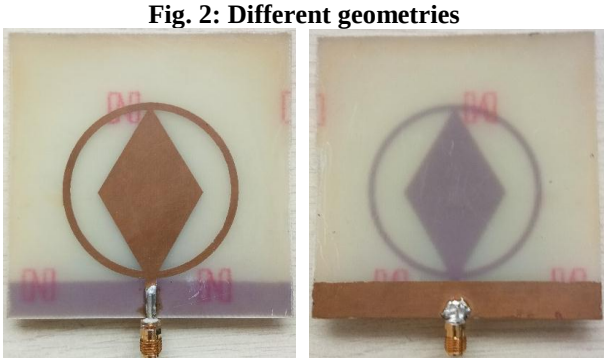


(c) Annular Ring combind with Diamond Patch's (Fig.1) Return Loss

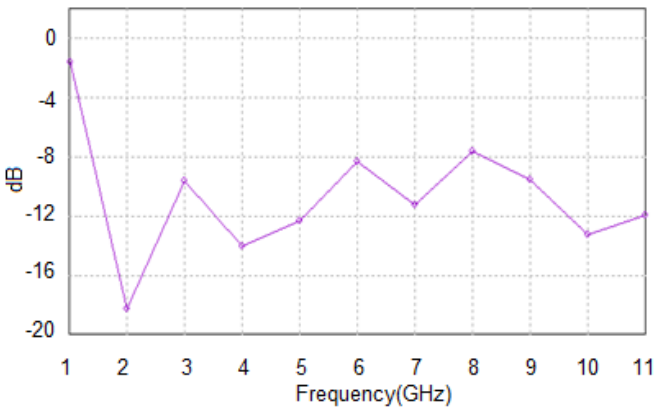
Fig. 2: Different geometries



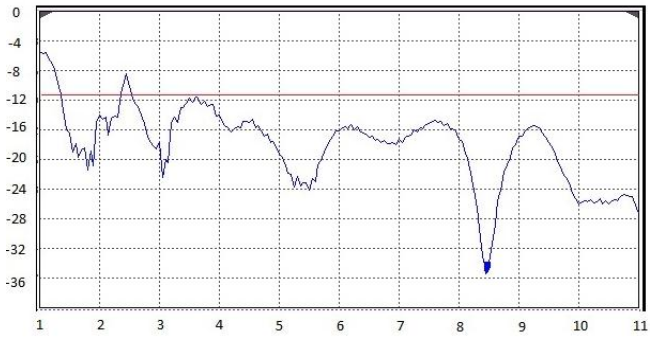
Front View **Back View**

Fig3: Photograph of prototype

The simulated return loss is shown in fig. 4 and measured results are shown to validate the same. The bandwidth has been checked for proposed antenna, found to be over 1.4 GHz to 11 GHz.



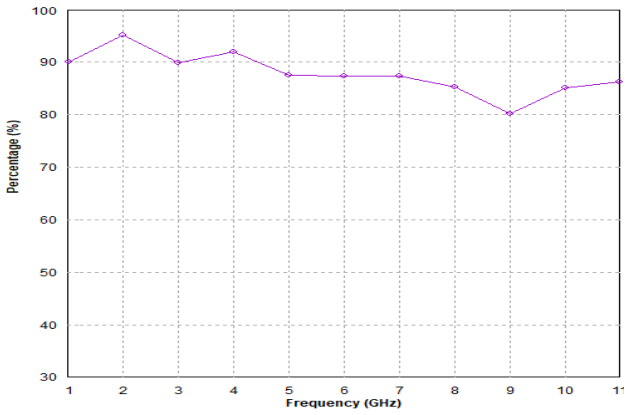
Simulated S_{11} in dB wrt to frequency in GHz



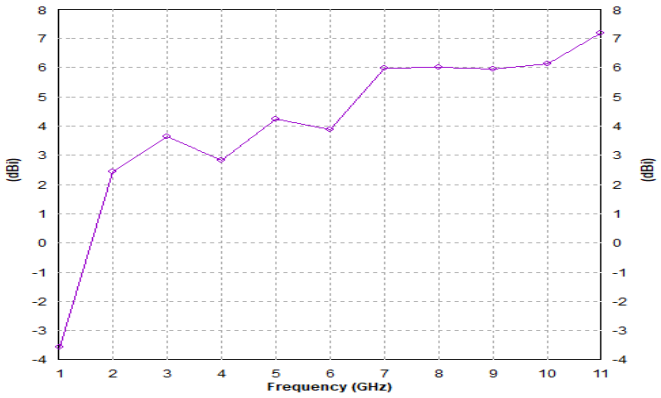
Measured S_{11} in dB wrt to frequency in GHz (of Fig. 1)

Fig 4: S_{11}The measured and simulated results

The simulated radiation efficiency and maximum gain is shown in fig. 5. The gain found to be around 4 dBi between 2 to 7 dBi for the entire required bandwidth and for the same frequency range radiation efficiency varies between 80 to 95% , So this antenna is efficient enough for the entire band of frequency from 1.4 GHz to 11 GHz.



Radiation Efficiency



Maximum gain

Fig5: simulated radiation efficiency and maximum gain

The simulated 3D-radiation pattern is observed for entire bandwidth and the experiment had been performed over one frequency at 3 GHz. The radiation patterns are shown in fig. 6.

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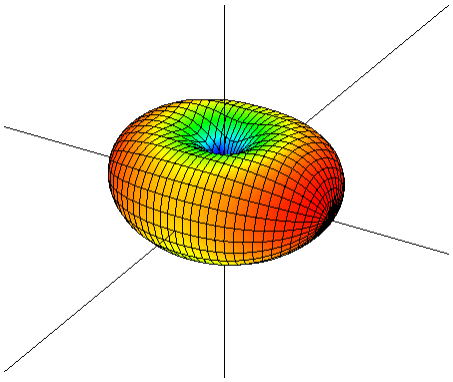
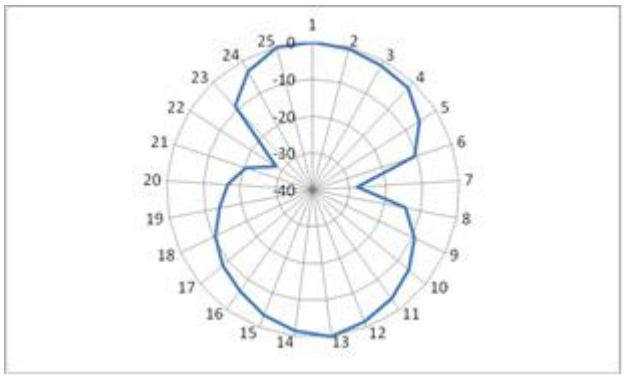
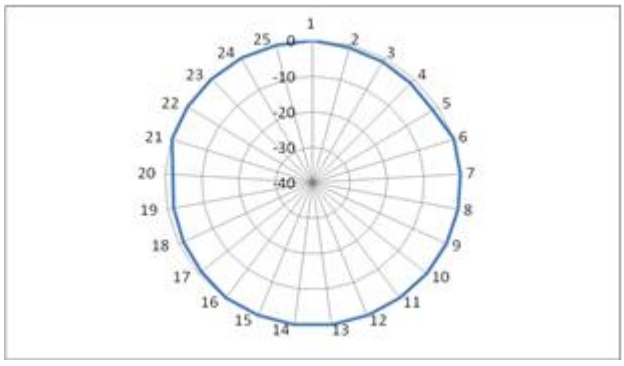


(a) 3D simulated radiation pattern at 3 GHz

The presented antenna shows radiation pattern as omni-directional on azimuthal plane and the radiation pattern is 'Figure of Eight' on elevation plane. The measured and simulated radiated field patterns are in good agreement.



On elevation plane



On azimuthal plane

(b) Measured radiation pattern at 3 GHz
Fig 6: Radiation pattern at 3 GHz

CONCLUSION

To improve the bandwidth of antenna a simple way is to use multi-resonators with overlapping of multi-resonance with better impedance matching. The proposed antenna has been designed, optimized with help of simulator then fabricated the prototype. The simulated results were validated in the laboratory. The designed antenna is showing good radiation characteristics over the entire UWB and beyond. This is very handy band for many wireless systems including the UWB.

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Dual Polarized Printed Monopole Antenna

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Abstract:

A dual polarized printed antenna for operation of dual polarization is proposed. The proposed antenna comprises of two ports connected to the square shape path. By using IE3D software simulation and measurement shows horizontal polarization and vertical polarization simultaneously with a gain of around 2dB covering a frequency range from 900 kHz to 6GHz which include ISM band, Bluetooth, Wi-Fi, and GPRS. Return loss of -10dB is achieved within the above mentioned Bandwidth for proposed antenna. The overall dimensions of antenna small in size with patch (15*15mm) and dielectric substrate (50*50mm).

Index Terms:

Antenna types, polarization techniques, radiation pattern

1. INTRODUCTION

In telecommunication, a printed antenna is normally fabricated over the dielectric substance like FR4 with partial ground plane [1]. The printed monopole antenna is fed through microstrip line feed to perfectly match the source/destination. IEEE standards definition for antenna is a way of radiating or receiving radio waves. There is another way of considering antenna as coupler between the transmitter/ receiver and the free space for transferring the electromagnetic energy [2]. There are many geometries available for printed monopole antenna (PMA) such as hexagonal, pentagonal, circular, square. For an efficient communication system, one needs guided medium. In the modern day wireless communication systems have been reduced in their size and so PMA became an important component of communication system. The different shapes of antenna include rectangular and other regular shapes to have larger bandwidth and hence improves the capacity, speed, reliability and reduces the interference, cost, size etc. Secondly, to enhance the capacity of communication, one may use dual polarization techniques for PMA [3-6]. This also helps to reduce the side effects of multipath fading. There are many applications for dual polarization operation for wireless communication which covers S-band and C-band frequency applications [7-8].

Presently, wireless communication technology is increasing exponentially with requirement of multiband and broad band antennas. For an efficient high channel capacity communication system, one may need to have a broad bandwidth, light weight, low profile, high gain, capacity, speed, simple structure antenna to ensure reliability, reliability, mobility, interference, cost, size etc. The reduced size of PMA plays a very important role for small systems. To fulfill all requirements of antenna the geometry and simulation must be accurate otherwise the transmission and reception of signal can be affected. To enhance the capacity and efficiency of the antenna single polarization can be replaced by using dual polarization. To achieve vertical and horizontal polarization single polarization requires two antennas but this problem can be overcome using dual polarization which requires only single antenna [9-10]. The rapid growth of communication system need dual polarized antenna to handle the large capacity. To improve multimedia application larger data rates for mobile users are required. To increase data rate and gain various wireless standards are used for example MIMO system. The majority of the current applications such as, Wi-Fi, Bluetooth operates on s-band frequency [11].

To increase the capacity of communication, one prefers to use dual polarization. Earlier research shows that the dual polarization works with single feed. The major drawbacks of microstrip antenna is their narrow bandwidth due to surface wave losses and large size of patch and for better performance PMA has been used.

This paper presents the design of the printed PMA where return loss, gain, directivity have been discussed. The size of the radiating patch is determined by the lower edge frequency rather than the central resonance frequency. The performance parameters of antenna were measured by VNA (Vector Network Analyser) in the laboratory. PMA is, actually, planar antenna and having radiation patterns as omni-directional on one plane and figure of eight on another plane behaving like a dipole antenna. The fluctuation of input impedance between the higher order modes is reduced by proper coupling of two feed lines of the PMA. In the presented paper numerical analysis is performed using IE3D software.

In duplex communication, single antenna can be used for both transmission and reception. A single polarized antenna is one that provides only one polarization either horizontal polarization or vertical polarization. The presented PMA may respond to both horizontally and vertically polarized signals.

Polarization diversity is possible using dual polarized antenna.

- **Why dual feed antenna?**

A novel dual feed PMA is presented with good matching for radiating patch and considerable isolation among the ports. The radiated fields are omnidirectional with horizontal and vertical polarization. The implemented antenna has partial ground plane with microstrip line feed.

- **Why dual polarizations?**

A dual polarized antenna radiated the vertically and horizontally simultaneously so it can cover the larger coverage area in both directions. Single feed single polarization antenna radiated either vertically or horizontally and given the radiation pattern look like a figure of eight at one direction. The concept is validated with simulation and measurement results including resonance frequency and radiation pattern [6-7],[9-11].

Table 1. Comparison of various shapes of microstrip antenna

Sr.No.	Shape of antenna	Return Loss	Gain(dB)	Bandwidth(GHz)
1	Circle	-16.5	8.1756	0.63
2	Ellipse	-25	7.2326	1.06
3	Hexagon	-22	7.4406	1.24
4	Square	-21	8.2799	1.22

2. ANTENNA THEORY

A. Antenna Design

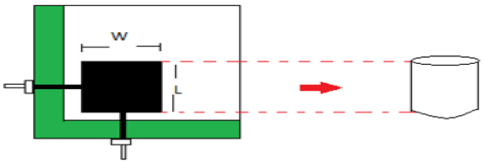

Fig.1 Basic structure of antenna

Assuming the same height for rectangular and cylindrical structure as L, hence their resonance frequency would be same for monopole antenna.

$$2\pi r\, L = W\, L \quad (1)$$

Gives,

$$r = W/(2\pi) \quad (2)$$

In the given equation, r is the radius corresponding to cylindrical monopole antenna and the resonant length is given as

$$L = 0.24\, \lambda\, F \quad (3)$$

whereas,

$$F = (L/r)/(1 + L/r) = L/(L + r) \quad (4)$$

By clubbing equation (3) and (4) the wavelength λ is obtained as:

$$\lambda = (L + r)/0.24 \quad (5)$$

Hence, fL, the lower band edge frequency is calculated by using:

$$fL = c/\lambda = 0.24\{c/L\}\ \{L/(L+r)\}$$

Assuming all the dimensions in centimetres:

$$fL = 7.2/\{L + (W/2\pi)\}\ \text{GHz} \quad (6)$$

But the monopole is fabricated on a substrate, thus

$$fL = 14.4\, \pi/(2\pi L + W)\, k\ \text{GHz} \quad (7)$$

Where,

k is the correction factor,

k=1.15 for FR4 substrate with εr= 4.3 and h = 0.159 cm [12,13]. If one includes the effect of feed gap p then the equation (7) can be re-written as

$$fL = 7.2/\{(L + p) + 0.159W\}\, k\ \text{GHz} \quad (8)$$

3. RESULTS AND DISCUSSION

In the proposed design two SMA connector are connected to antenna for feeding. The advantage of connecting two port is one can connect two applications to single antenna such as Bluetooth on port one and Wi-Fi on port two. Since it is polarized in both horizontal and vertical direction, the two applications can carry out their tasks successfully.

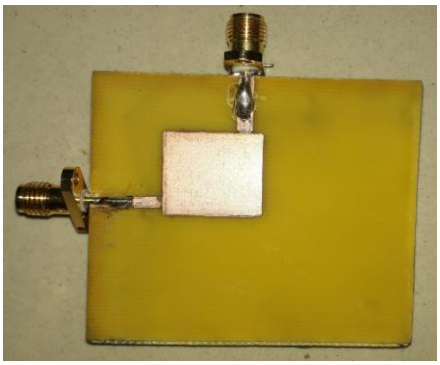

Fig.2. Hardware implementation of antenna

The designed antenna's radiation pattern was simulated for entire bandwidth which was observed as shown in Fig 3 and Fig 4. The radiation pattern is figure of eight on elevation plane and omnidirectional on azimuthal plane with two planes of polarization exactly perpendicular to each other. The corresponding measured radiation patterns for 3 GHz are shown in figure 5 and 6 on both the planes to validate the radiation with dual polarization.

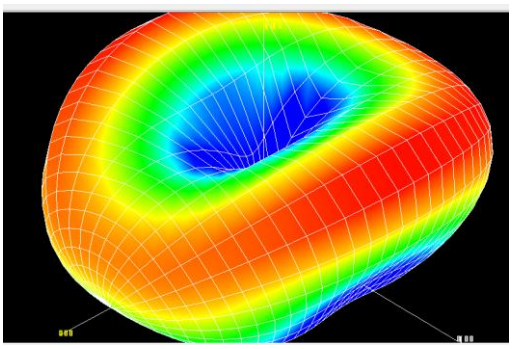

Fig 3. 3-dimensional radiation pattern

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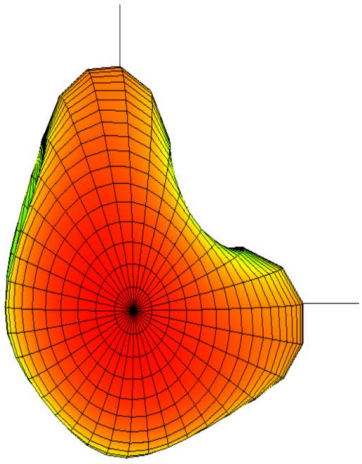

Fig 4. Radiation Pattern of Dual Polarization

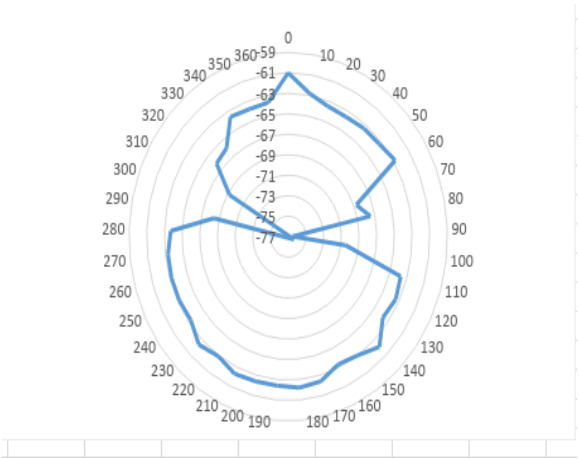

Fig.5. Monopole antenna's radiation pattern

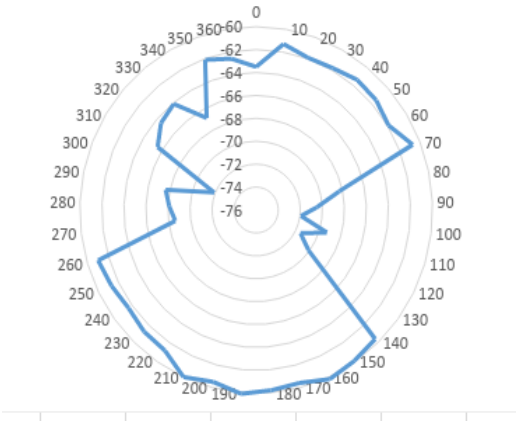

Fig.6. Monopole antenna's radiation pattern

The proposed prototype antenna is tested for various S parameters using Vector Network Analyser and the results observed are as shown in Fig. 7 and Fig.8.

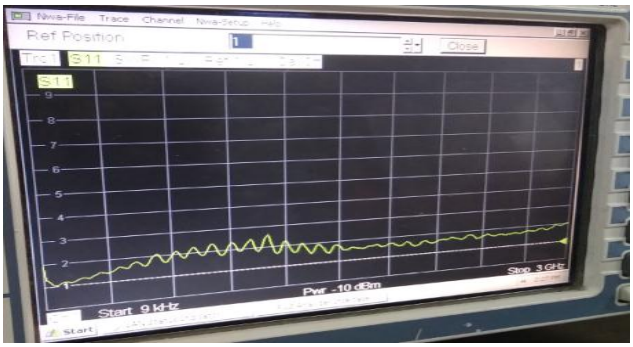

Fig 7. VNA Screenshot of VSWR at port one

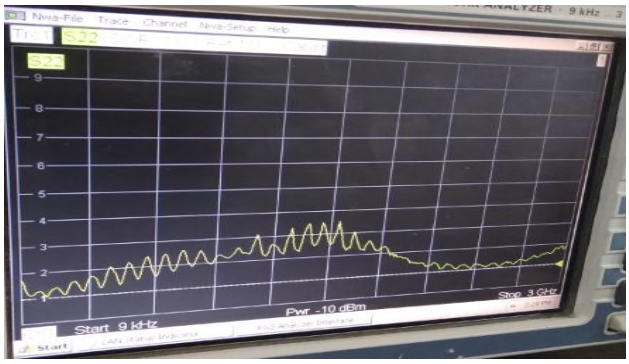

Fig 8. VNA Screenshot of VSWR at port two

Corresponding to the figure 7 and 8, the simulated VSWR is shown in figure 9, they are in agreement.

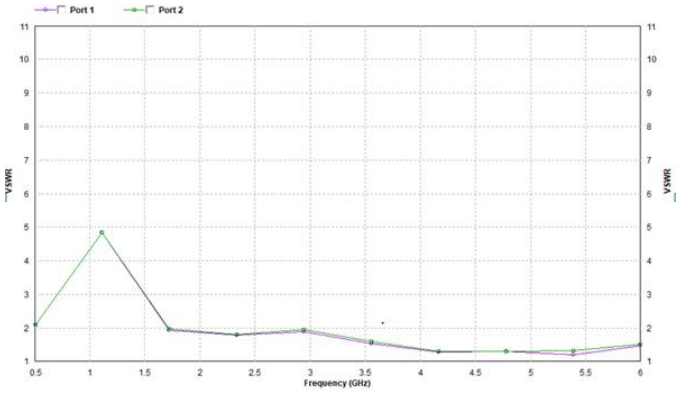

Fig 9. Simulation Graph Of VSWR v/s Frequency for port one and two

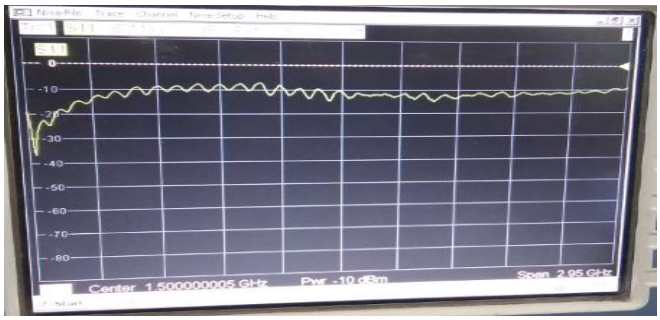

Fig 10. VNA Screenshot of S_{11}

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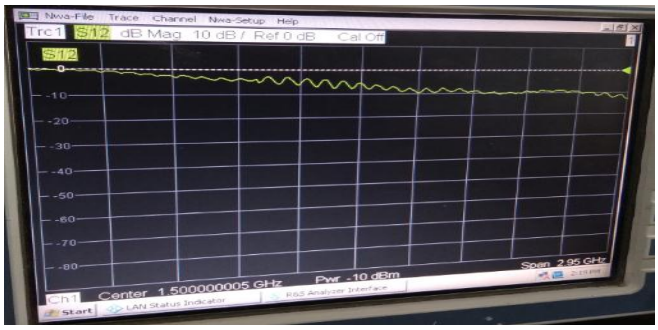

Fig 11. VNA Screenshot of S_{12}

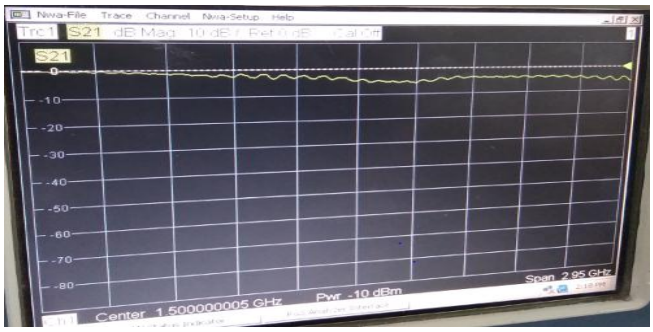

Fig 12. VNA Screenshot of S_{21}

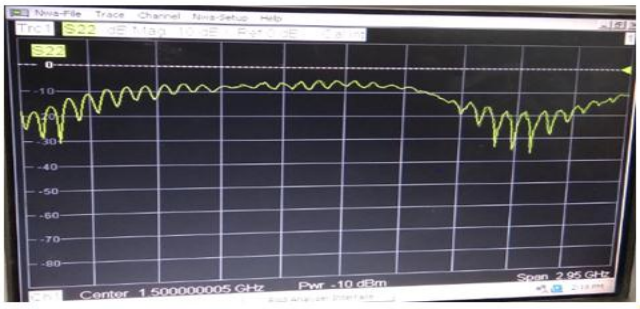

Fig 13. VNA Screenshot of S_{22}

From the figure 10 and 13 it can be seen that the values observed on S_{11} and S_{22} are similar, impedance bandwidth is having good matching. From the figure 11 and 12 it can be seen that the values observed on S_{12} and S_{21} are similar and showing good isolation between the two ports.

CONCLUSION

The proposed antenna was to implement a Dual Polarized Monopole Printed Antenna. For this studied reference and observed different antenna and their parameter. After the survey of antenna, the rectangular shape of the antenna is implemented with dual feed for dual polarization. To overcome the limitations of the single polarization the antenna with dual feed has been implemented. Hence the resulting parameter we got the impedance matching at both port and due to this we get the dual polarization which is radiating in both directions in horizontal direction as well as in vertical direction simultaneously successfully. The return loss is also at permissible level and got the Gain around 2db which assure the maximum efficiency and increases the capability of the antenna.

It is beneficial to MIMO technology where we can connect multiple applications to the single antenna. It also covers the maximum number of applications including ISM band, Wi-Fi, Bluetooth etc."

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Electronic System Design

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Abstract:

Electronic System is a setup of electronic components, devices used in electronics. Large number of topics, which covers analog and digital systems, which is being implemented by using discrete and integrated circuit. Also includes design techniques to cover Electronic Design Automation, authentication, endorsement, and system framework which implements real time embedded systems. Presented paper also includes an example of communication system design emphasizing on structures, characterization and system applications.

Index Terms:

Electronic System Design, Biometric, fingerprint recognition, proxy prevention, Student attendance system, application

1. INTRODUCTION

Field of electronics is being related to flow of charge of electron through any medium like conductor, semiconductor, vacuum, gas, air, water even through insulator like glass fiber. The history of electronics engineering is as old as human's civilized life. It began with safety and security of the mankind. A set of inputs and outputs form the electronics system comprising of one or many devices/components [1]. They are classified on basis of operations for e.g. communication system, medical electronics, instrumentation, control and computer system. Electronic circuit or system must communicate with an I/O device where the trigger signals are in form of electrical data/signals [1-2]. Electronic systems can also be classified as; Analog Electronics, Digital, Power and Micro Electronics, Communication systems. Electronic systems are, normally, design to perform certain functions. The performance of an electronic system is evaluated in terms of voltage, current, impedance, power, time , frequency and input and output of system. These parameters include transient specifications, distortions, frequency specifications, and DC and small signal specifications [1-3].

The Accreditation Board for Engineering and Technology (ABET) largely expresses engineering design as, "Engineering design is a process of devising a system, component or process to meet desired needs". Design is a decision-making exercise (often with multiple samples) in that the basic sciences, analytical/numerical and engineering sciences are used to modify resources optimally to obtain the stated objective. Among the fundamental elements of design process are the establishments of objectives, criteria, synthesis, analysis, construction, testing and evaluation" [4].

Engineering is all about establishment of devices, processes and systems, which are needed by the society. This is achieved with the help of engineering design. The engineering design component must include the following features; formulation of design problem may be open-ended problem statements and its specifications, improvement of system and application of design concepts and methodology, detailed system description, with concurrent engineering design, feasibility considerations with alternative solutions. The production process must include number of actual, practical factors such as reliability, safety, ethics, economic factors, social impact and aesthetics.

2. ENGINEERING DESIGN PROCESS

The primary objective of this work is to have an insight of engineering design process. As shown in figure 1, the block diagram of proposed engineering design process [5]. The elements of Engineering Design Process are as follows:

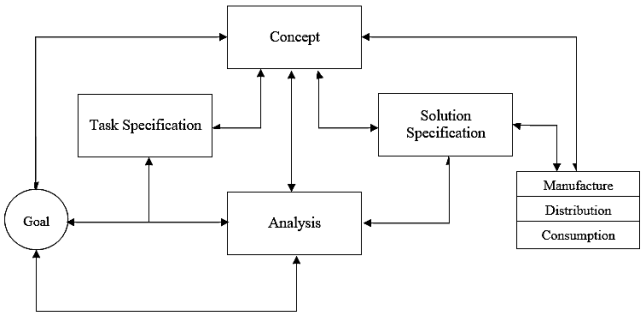

Figure 1: Block diagram of Engineering design process

Concept

Concept of obtaining the best results is the ultimate engineering experiment/hypothesis which rise in the beginning as mental image. These are noted initially as line diagrams/flowcharts then successfully validated, polished, systematized and eventually documented by standardized formats. The hypothesis are sometimes preceded or followed by acts of assessment, inferences and verdicts.

Goal

A process may be an assertion of the need to fulfil the desire of mankind that is known as goal.

Analysis

The procedure of analysing is intermittently instinctive and quality based but more often it is analytical/numerical, quantity based, cautious and unambiguous. In the light of analysis conducted, tasks specifications and even goals may be altered.

Solution Specification

It consists of all drawings, materials and parts list manufacturing information and so on necessary for construction of device system or process.

Task Specification

The prime responsibility of engineer is to develop more comprehensive, computable information that defines the task to realize in order to meet the goal. Now, the scope of problem is defined.

Manufacture/ Maintenance/ Disribution/ Consumption

The design process must envision and combine provisions for distributions, preservation and optimum substitute of products. Production consideration can have greater effects on design tactics particularly when mass production is foreseen.

3. PROPOSED SYSTEM

In digital modulation, discrete information signal is superimposed over the carrier, which is analog in nature. Digital modulation techniques may be taken as DAC whereas on the receiver side it may be considered as ADC [6-8]. Here we are proposing a system, which provides a simple modulation- demodulation technique using amplitude shift keying. The engineering design process for this system goes as following:

Concept

Achieveing ASK using linear modulator was a difficult task. So we desinged our concept to achieve ASK in simplest way possible.

Goal

Present case study goal is to achieve ASK using IC MC5014B, which helps digital data to be converted into analog form to pass through BPF channel by using finite number of amplitude samples.

Analysis

In ASK system two logic levels (1 and 0) of the data are represented by two carrier signals with different amplitude but constant phase and frequency signal. The mathematical representation of ASK is

V_{Ask} (t) = A Cos w_0t (when logic data = 1)

V_{Ask} (t) = B Cos w_0 t (when logic data = 0)

Modulating signal: Square wave (10 Vp-p , 200 Hz)

Carrier signal: Sine wave (2.5Vp-p , 1KHz)

In the given circuit, Square wave (modulating signal) is given as control input (pin no 11) to the IC 14051 (analog multiplexer). Sine wave (carrier signal ACosw_0t) is given at input line X_0 (pin no 13) and amplitude shifted carrier signal BCosw_0t (using potentiometer) is given at line X1(pin no 14).Due to the multiplexing action ASK is generated at the output of IC14051.

4. SOLUTION SPECIFICATION

MC14051B is a Motorola, low power, CMOS Analog Multiplexers and demultiplexers IC. It is an analog switch which is controlled by digital pulses, which can be configured as 8:1 multiplexer or 1:8 demultiplexers. It has low ON impedance and very low OFF leakage current.

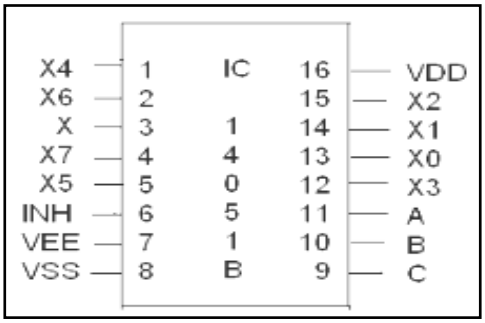

Figure 1: Pin diagram of IC 14051B

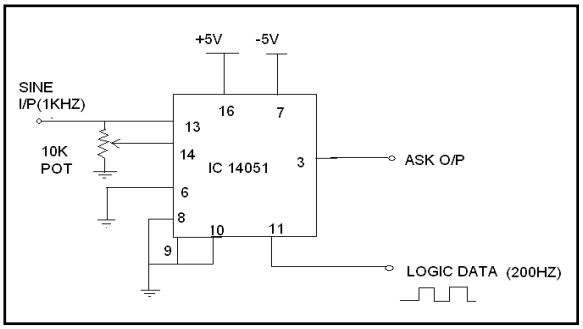

Figure 2: ASK modulator circuit

Peak diode detector is used as ASK demodulator with R-C LPF, is as shown in figure 4 with corresponding waveforms in figure 5.

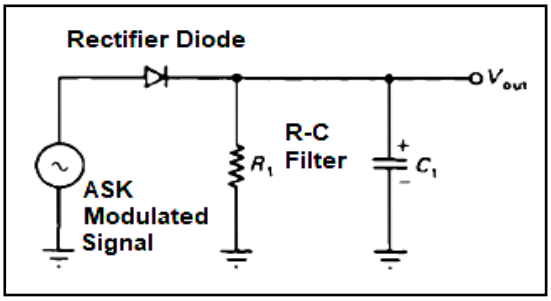

Figure 3: ASK demodulator circuit.

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5. RECYCLING OF DESIGN PROCESS

The broad outlines have been shown in figure 5; the details depend on the type of the system to be designed. Recycling of design process is to; Identify, Generate (- Idea, plan, layout, sketch), Refine (-Physical shape, weight, etc.), Analyze(- Engineering science, mathematics and logic), Decide(- Accept, reject, stop, rest) and Implement(- solutions specification model). The steps are repeated until desired specifications have been satisfied. Design engineer should be able to work with multidisciplinary team.

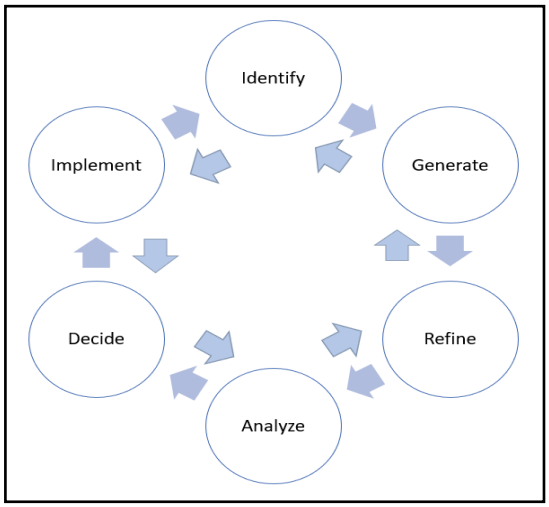

Figure 5: Recycling of design process

6. RESULT

As shown in figure 3, the modulator circuit which is linear multiplier, generates the ASK waveform. This device multiplies two signals, which are available at the two signal inputs as shown in figure 3. This circuit behaves as product modulator. The sinusoidal signal is selected as carrier since other signals creates the unwanted harmonics, hence increasing the bandwidth. The message is in the form of digital pulses, which is known as modulating signal.

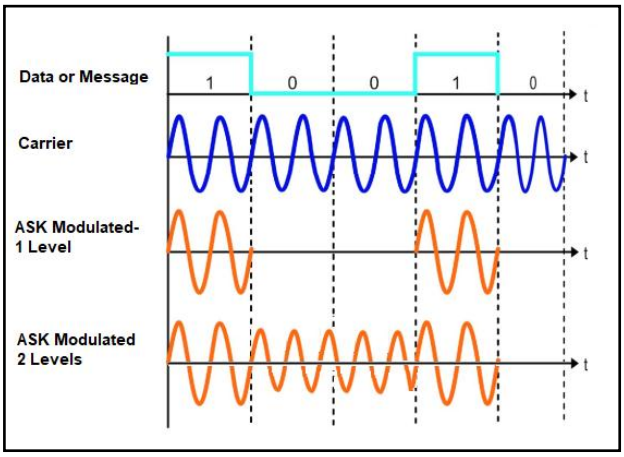

Figure 6: ASK modulation waveforms.

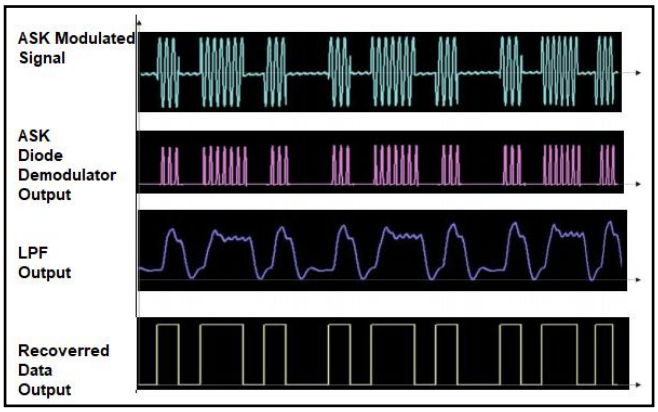

Figure 7: ASK demodulation waveform

7. CONCLUSION

In the field of Electronic Systems Design, one can apply the idea to many industries such as medicine, space technology, oil exploration, underwater technology, acoustics and microchip development. Future lies with High Density Electronics System Design and Electronic Embedded systems. Electronic System Design Automation helps in optimizing the system performance, especially timing optimization. This is made possible by proper synthesis of hardware and software.

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Novel Multisource inverter based energy management system in Electric Vehicle

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Abstract:

Day after day, natural energy sources are dwindling. Energy saving plays a crucial role in reducing the amount of pollution. Electric Vehicle consists of an energy storage system. Full car efficiency relies on energy storage system capacities. Driving cycle with high specific energy requirements that are met by the source of the battery. The battery will supply specific peak power demands with great current stress. Great present stresses directly affect battery life as a battery with less power density. It was discovered from the literature that supercapacitor has elevated power density and can be used as a specific power supply energy during the driving cycle's peak energy requirements. The supercapacitor can be used during car break to store dynamic power storage source. All power/energy requirements of the driving cycle have simultaneously regulated the operation of both sources.

A new multi-source inverter can be used to improve the vehicle's driving cycle. During an unstable case triggered by the power scheme, it can also use as a vibrant energy restore. Paper is a multisource inverter (MSI) analogy, MSI simulation, and multi-source inverter operation with hardware outcome debate.

Index Terms:

Multisource Inverter (MSI), Battery, Ultra capacitor (UC), Driving cycle, Efficiency, Energy storage system (ESS)

1. INTRODUCTION

A hybrid electric vehicle with a storage scheme of multisource inverter type is beneficial and responsive to dynamic variations in the electric vehicle's driving cycle. The battery used to meet long-term demand for energy and the ultra-capacitor meets particular maximum power requirements. This article involves applying multisource inverter-based ESS to regulate approach intended for source features based on the Ragon plot. The power-sharing towards load depends on the load torque and the state of charge of the UC and Battery controlled using inverter control. A simulation is performed using MATLAB/ SIMULINK environment. Novel inverter multi-source terminology validated by the prototype. Active sharing improves the driving cycle, weight reduction ESS effectiveness.

2. EXISTING STRATEGIES

Ragon graph created an idea for comparing different source with efficiency. From the Ragon chart it is clear that batteries have a relatively high density of energy but a lower density of power, on the contrary, the UC has a lower density of energy with a sufficiently high density of power. Moreover, UC's life is much higher than its battery life. Also, UC's have low-temperature performance compared to batteries. The general efficiency of the scheme improved by mixing both sources[1-4].

2.1. Passive parallel

It's the easiest ESS setup. Without any converter or inverter, the battery and UC bank was linked to the dc connection in this setup. The two sources of energy are connected here in parallel.

$$V_B = V_U = V_{DC}.$$

The benefits of this setup include ease of application, and the DC / DC converter or inverter is not needed. Wecan not efficiently use ultracapacitor with this analogy.

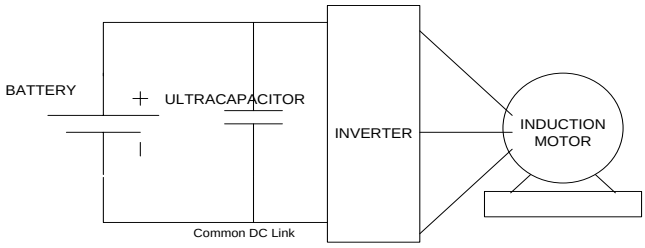

Fig.1 Basic passive parallel hybrid configuration

2.2. Battery/ UC configuration

The battery connected to the DC link via DC/DC converter and the UC is connected directly to the dc connection. The benefits of this are the voltage, or a battery can be kept lower or higher than the UC voltage.

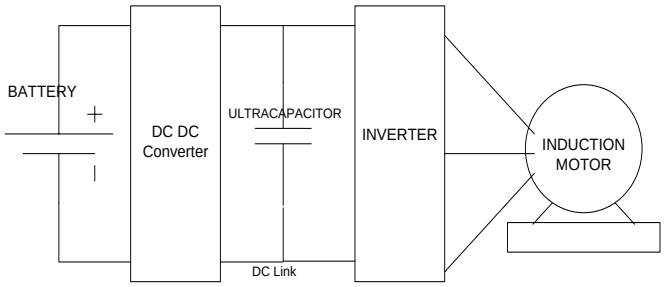

Fig.2 Battery/UC configuration

2.3. UC/ Battery configuration

In this configuration UC connected to the dc link through the DC/DC converter and battery is directly connected to the DC link. The advantage of this configuration is that the voltage of UC can be used with a versatile range, but the limitation of this configuration is that the converter needs to be the large size for handle the power of UC therefore, the adverse effect of a cost of the converter.

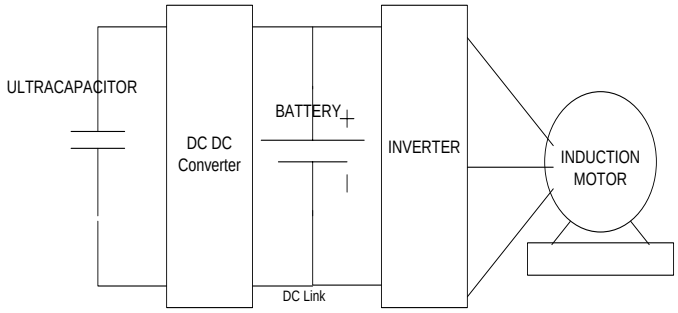

Fig.3 UC/battery configuration

The analogy is developed using MATLAB simulation

2.3.1. Simulation of the system

Basic simulation performed for UC / battery configuration with a simulation time of 1000 seconds with Battery connected to Load, whereas UC connected through a DC-DC converter. Gradually load increased with time intervals of 300 sec. Results are observed to identify the dynamic response of the ultracapacitor for stated analogy (3. 3.).

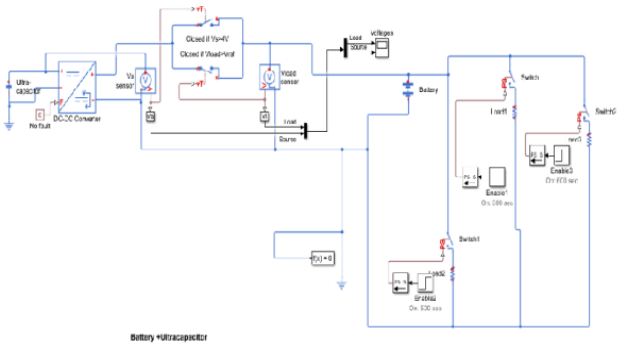

Fig.4 Simulation of UC/Battery Configuration

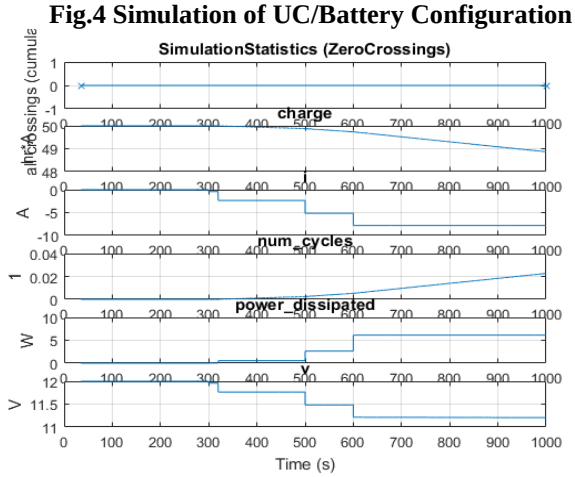

Fig. 5 Discharging of Ultracapacitor according to load

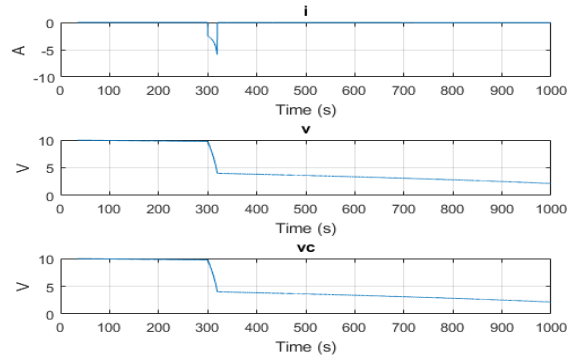

Fig. 6 Discharging of Battery according to load

Peak power demands (Fig. no. 6) at 300 sec and 600 sec is handled by ultracapacitor discharging. Peak current requirements are fulfilled by ultracapacitor whereas base requirements dealt with by Battery as an energy source.

Two converters were used in the existing system. Converter losses can be minimized using the direct connection of sources with 3 phase load, which is analyzed by the proposed method.

3. PROPOSED MULTI-SOURCE INVERTER[3]

This topology's primary aim is to cascade multiple dc sources with connection to the three-phase AC load. In this case, two DC sources are connected, namely Battery (VB) and Ultracapacitor (VU); this multi-source inverter consists of 12 microcontroller-controlled IGBTs. The primary benefit of this topology is that it does not add any additional stages between load and sources, resulting in improved electric vehicle efficiency by enhancing the fulfillment of energy and power demand. Source current regulated according to driving cycle torque demands in the suggested control approach. Three switching modes are chosen here with microcontroller based on Electric Vehicle acceleration,

cruising and breaking. There are three operating modes regarding switching states

- **Mode 1:** V_B is not used and switches S_{L1}, S_{L2}, S_{L3} and S_{U11}, S_{U12}, S_{U13} enable V_U to supply the motor;
- **Mode 2:** The switches S_{U1}, S_{U2}, S_{U3} and S_{U11}, S_{U12}, S_{U13} would allow V_B to supply the motor with charging V_U. The output voltage is equal to V_B-V_U ;
- **Mode 3:** The switches S_{U1}, S_{U2}, S_{U3} and S_{L1}, S_{L2}, S_{L3} enable V_B to supply the motor, and V_U is not used.

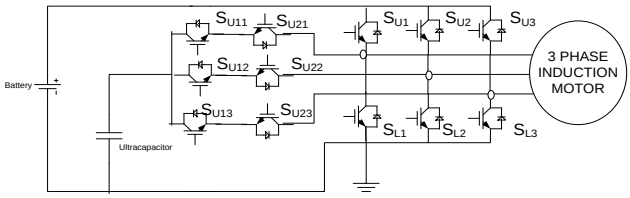

Fig No.7 Multisource Inverter

The voltages [V_{1O}, V_{2O}, V_{3O}] are functions of the state of the switches and input voltages:

$$V_{1O} = E_{SU1}V_B + E_{U11}V_U - Z_a i_1$$
$$V_{2O} = E_{U2}V_B + E_{U12}V_U - Z_b i_2$$
$$V_{3O} = E_{U3}V_B + E_{U13}V_U - Z_c i_3$$

Where, Z = impedance of load

$E_{SU1,2,3}$ and $E_{U11,12,13}$ = Switching functions

Similarly input currents [I_B,I_U] can be expressed as:

$$I_B = E_{SU1}.i_1 + E_{SU2}.i_2 + E_{SU3}.i_3$$
$$I_U = E_{U11}.i_1 + E_{U12}.i_2 + E_{U13}.i_3$$

Table 1- Switching Combinations of MSI[3]

Mode	States of Switches			Line Voltages		
	S_{U1} S_{U2} S_{U3}	S_{L1} S_{L2} S_{L3}	S_{U11} S_{U12} S_{U13}	V_{12}	V_{23}	V_{13}
1	Battery Open	0 1 1	1 0 0	V_U	0	$-V_U$
		0 0 1	1 1 0	0	V_U	$-V_U$
		1 0 1	0 1 0	$-V_U$	V_U	0
		1 0 0	0 1 1	$-V_U$	0	V_U
		1 1 0	0 0 1	0	$-V_U$	V_U
		0 1 0	1 0 1	V_U	$-V_U$	0
2	1 0 0	Switches Open	0 1 1	$V_B - V_U$	0	$-(V_B - V_U)$
	1 1 0		1 0 0	0	$V_B - V_U$	$-(V_B - V_U)$
	0 1 0		1 0 1	$-(V_B - V_U)$	$V_B - V_U$	0
	0 1 1		1 0 0	$-(V_B - V_U)$	0	$V_B - V_U$
	0 0 1		1 1 0	0	$-(V_B - V_U)$	$V_B - V_U$
	1 0 1		0 1 0	$V_B - V_U$	$-(V_B - V_U)$	0
3	1 0 0	0 1 1	Ultracapacitor Open	V_B	0	$-V_B$
	1 1 0	0 0 1		0	V_B	$-V_B$
	0 1 0	1 0 1		$-V_B$	V_B	0
	0 1 1	1 0 0		$-V_B$	0	V_B
	0 0 1	1 1 0		0	$-V_B$	V_B
	1 0 1	0 1 0		V_B	$-V_B$	0

4. PROTOTYPE DEVELOPMENT

The hardware consists of Buffer IC (74HC244) to control modes with adjustment of duty cycle using enable signal. EN1 is used to control upper switches S_{U1}, S_{U2}, S_{U3}. EN2 control S_{L1}, S_{L2}, S_{L3} whereas EN1* and EN2* are used to control S_{U11}, S_{U12}, $S_{U13}$and S_{U21}, S_{U22}, S_{U23} respectively. The low state (digital zero) of the latch is allowing input at latch output. Simulation is carried out using the Proteus design suit environment [27–30].

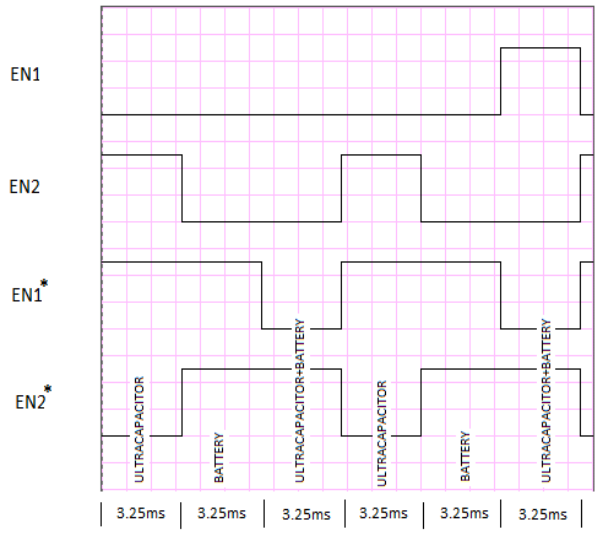

Fig. 8.Mode Control using Buffer

MOSFET switches controlled through Latch, explained as follows.

Table 2. Latch and switch the Enable States for mode-1, 2 & 3.

Control State	EN1 (S_{U1}, S_{U2}, S_{U3})	EN2 (S_{L1}, S_{L2}, S_{L3})	EN1* (S_{U11}, S_{U12}, S_{U13})	EN2* (S_{U21}, S_{U22}, S_{U23})
UC (Charging)	ON	OFF	OFF	ON
Battery (Discharging)	ON	ON	OFF	OFF
Battery (Discharging) + UC (Discharging)	ON	ON	ON	OFF

Switch controlled through SVPWM (Space Vector Pulse Width Modulation) technique shown in Fig. 9 below.

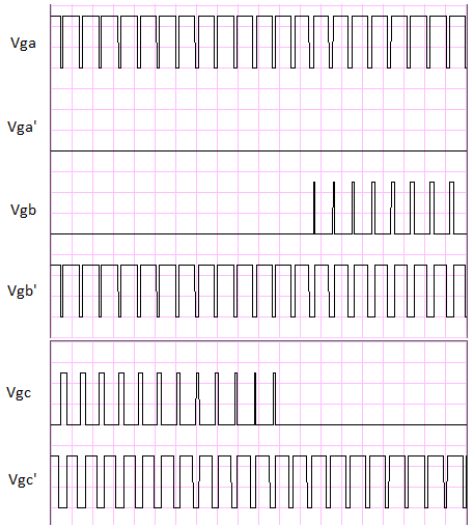

Figure 9.SVPWM Control signal generation in protease.

The operation of the circuit is explained with a flow chart (Figure 10) as follows.

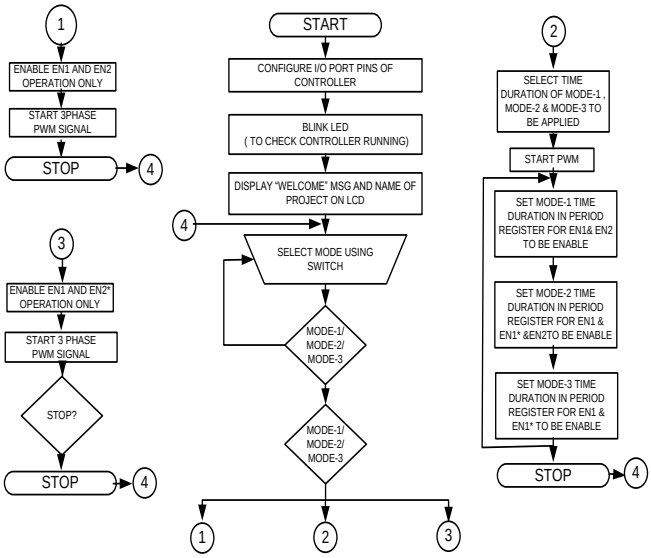

Fig. 10 Process Chart

In the Implementation of hardware, battery and ultracapacitor drive the load (Electric motor / Grid / RL Load) in which we observe the power and energy sharing conduct during dynamic loading scenarios. Observations are made for distinct combinations of three modes (i.e., mode-1: battery as a source only, mode-2: both sources simultaneously handling the dynamic power requirement condition and mode-3: ultracapacitor as a source).

Hardware is introduced using 6 IGBTs, the three-phase inverter that provides battery energy to the AC link and the ultracapacitor bank attached to the AC connection via 6 IGBTs. Thus, the implementation uses a total of 12 IGBTs.

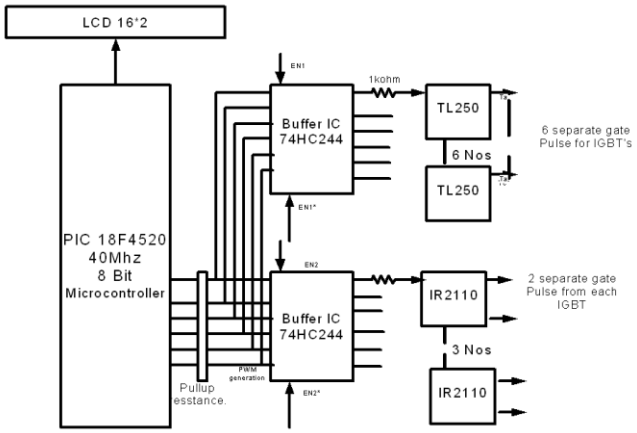

Fig. 11 Hardware implementation

Hardware is introduced using the three modes earlier indicated. PCB is built using express PCB software.

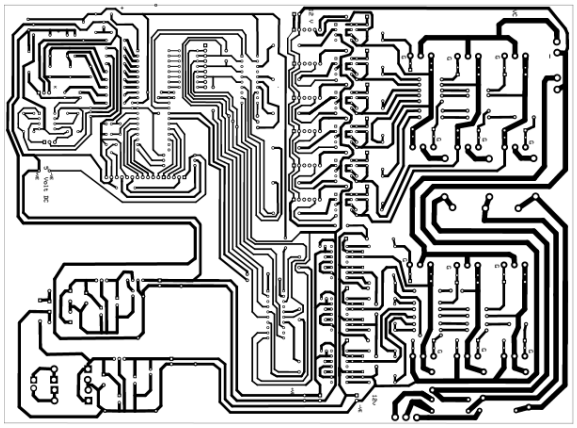

Fig. 12 .PCB layout

Single side PCB Itched and made with parts for fastening. Using the SVPWM analogy, the 18F4520 microchip processor is used with a control approach based on a lookup table with signal generation and using dqo vectors, digital control signals created in six sectors.

Look up table with 864 states is included to decrease the controller's computing time, so we get two-level inverter output. Buffer (74HC244) is used to select the modes.

5. RESULTS

In this chapter, experimental findings are discussed in detail with distinct combinations of three modes. Case-1: In this case, Battery functions as a source and offers a resistive load (mode-1). Inverter voltage and current for case-1 where SVPWM-based inputs are generated from the inverter.

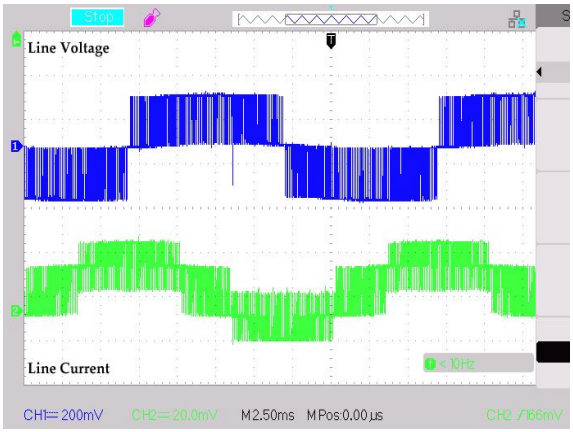

Fig.13.Line Voltage and current at the inverter output

Input voltage obtained from the battery to inverter is 24 V DC. The output obtained with the line to line voltage is 12volts with current 1.2 A (readings measured across 1-ohm resistor connected in line with RL load). Waveform below (Figure 33) shows phase displacement between different phase voltages of the inverter.

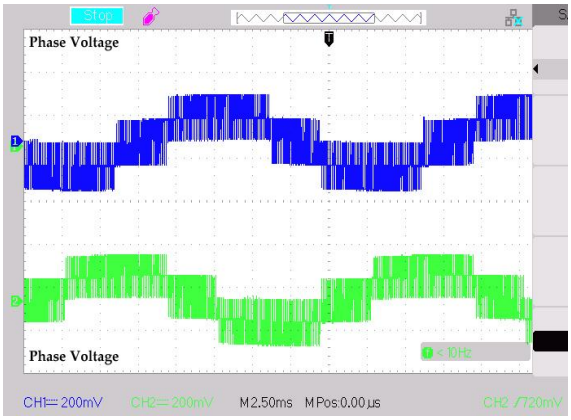

Fig.14.Phase voltages at the inverter output

Output with input for case-1 where battery supplies power to load is as follows. Readings of battery current are noted by variation in 3 phase load with continuous, intermittent switching of 10 s.

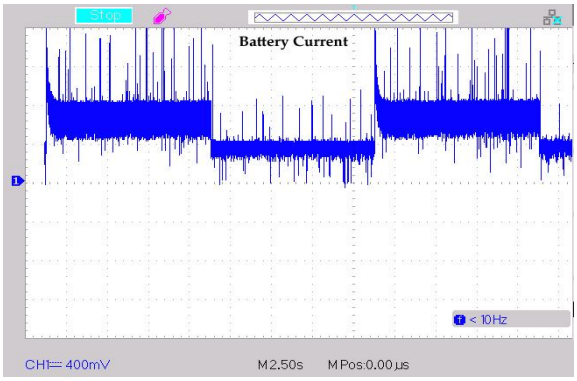

Fig.15. Battery Current

In this case, the battery source alone fulfills the complete energy requirement. In this case, the current from the battery is 4 A for 5 s and 2 A for the next five intervals, giving an average battery current of 3 A.

Case-2: You can change the mode by using latch enable signals. It is the suggested method for analyzing and interpreting results and conclusions by simultaneously implementing a mixture of distinct sources (mode-2, mode-3).

By adjusting the duty cycle of source utilization, the prototype is tested for different combinations of sources. With a potentiometer, the duty cycle adjustment provision is integrated into the hardware. For three distinct blends, the duty cycle is set, and the average battery current is calculated for a steady charge. Throughout the cycle, the battery alone and a mixture of battery-ultracapacitor are used together for 0.5 ms. The mode-2 battery current is 1.60 A, 0.04 A for mode-3. It is calculated that the average battery current achieved for 1 ms with two modes is 0.82 A.

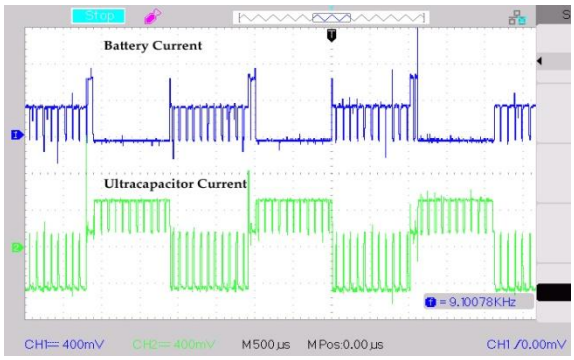

Fig.16. Battery and Ultracapacitor currentsmode-2 and mode-3 with t_1=0.5 mS, t_2=0.5 mS.

Case-3: In this case, the load is fulfilled through individual ultracapacitor, battery and ultracapacitor together, and a single battery for 0.5ms each. For mode-3, the battery current is 0.04 A, for mode-2 it is 1.6 A, and for mode-1 it is 2.8 A. Average battery current calculated turns out to be 1.48 A.

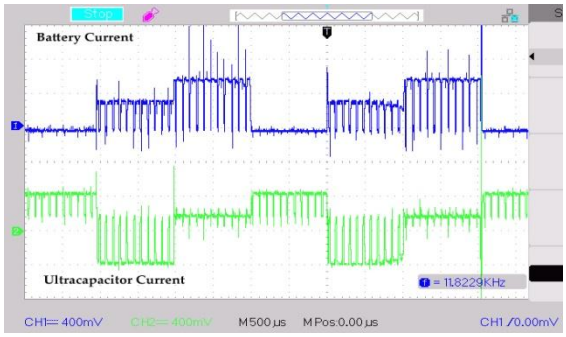

Fig.17. Battery and Ultracapacitor currentsmode-3,mode-2 and mode-1 with t_1=0.5 ms,t_2=0.5 ms, t_3=0.5 ms.

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Case-4 This case consists of the load is fulfilled through a battery, ultracapacitor together (mode-2) and individual battery (mode-1) for 0.5ms each.

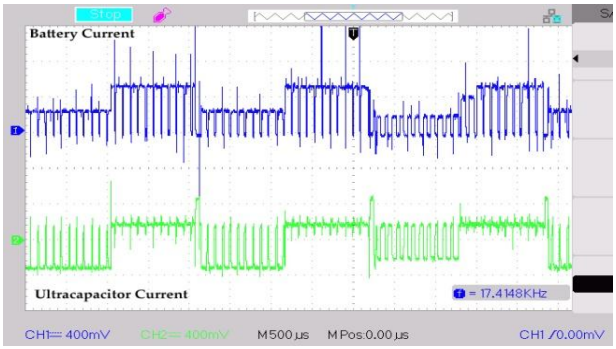

Fig.17. Battery and Ultracapacitor currentsmode-2, mode-1with t_1=0.5 ms, t_2=0.5 ms.

Above waveforms depict the load shared by battery alone, i.e., mode-1 (2.4A) and the load shared by battery and ultracapacitor, i.e.,mode-2 are used together (1.2 A). The average battery current obtained with these modes (mode-2 and mode-3) is 1.8 A.

As an ultracapacitor is used to supply power demands of short duration, thereby mode-3 can't be independently used for long term energy requirements.

Table 5.Current comparison for different cases

	Case-1 (Mode-1)	Case-2 (Mode-2&3)	Case-3 (Mode-1,2 & 3)	Case-4 (Mode-1&2)
Average Battery Current	3 A	0.82 A	1.48 Amp	1.8 Amp
Ultracapacitor Current (Discharging)	0 A	2 A	2 A	1.6 A

Here we use standard mode (energy-supplying battery) or blended mode in which ultracapacitor alone and battery-ultracapacitor sharing can be preferred to minimize average battery current. The minimization of battery current increases the electric vehicle's operating cycle/driving cycle (or any load). Mixed mode (case-2) provides an average current of 0.82 A compared to the individual battery mode, which provides an average battery current of 3 A, obviously showing an average battery current of 27.33 percent (0.82 A* 100/3 A) compared to tooth control modes (case-1), resulting in a much enhanced driving cycle range.

The experimentation work is performed using a small prototype energy management system composed of the differential probe Battery, Ultracapacitors, Control Board, Power Supply, Digital Storage Oscilloscope.

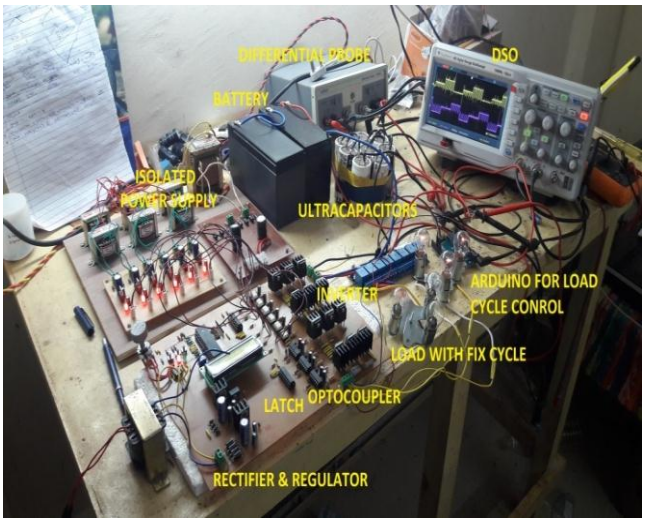

Figure 18.Experimental Setup

With experimental results hardware tested for different cases with mode-1-, mode-2, and mode-3.

CONCLUSION

Appropriate multi-source inverter topology was suggested for HESS in this paper. This topology has the primary benefit of not adding any new stages between grid/motor and battery. The result of the novel multi-source connection is improved energy demand load fulfillment, thus enhancing electric vehicle efficiency. Smooth present sharing and lower average currents are also accomplished with multi-source inverters. On the other side, the battery can drive an engine directly without any boost operation as per the DC / DC converter, thereby lowering the generic converter price and also improving the effectiveness of EMS. During dynamic load requirements acquired using the SVPWM-based control approach, which increases load stability as an induction motor, active power, and energy sharing between multisource is feasible. Finally, a scaled-down prototype is used to study the efficiency of multisource inverter topology. From experimentation, it is noted that with multisource topology, the higher driving range is achieved with a decrease of the average current to 27 percent compared to the current from the battery during standard methods of EMS control with higher heat stability, reduction in overall size and improvement of the life of the power storage system.

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IoT Based Dual Arm Tele-Robotic System

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Abstract:

The world has come close with the new technologies and one of it is the Internet of Things (IoT). This paper proposes a tele robotic vehicle with a pick and place dual arm and video surveillance application using Arduino Mega. The robotic vehicle at the application end is interfaced with the cloud and at the user end with mobile applications. Internet is used as a Wi-Fi as a medium. Previous systems used Bluetooth, Zigbee, LAN which has a short range, higher power consumption and systems are unable to operate in the real time. Tele – robotic system gives the idea where the user can control the robot without being present at the application area. The software itself is the core of IoT which defines each device identically. Dual arm soft catching gripper is designed for the pick and place application, it avoids the extra pressure on the suspected objects. Online surveillance is possible with the IP camera. ESP8266 Wi-Fi module is used as internet medium. Client manages the robotic vehicle from a distance through a remote – an android Blynk application to move forward, reverse, left, right, stop, pick and place. GPS is used to trace the location of the robot in the application area. Ultrasonic sensors detect the obstacles in the way of the robot and stops it from falling from a depth and also prevents it from colliding with the obstacle. Arduino Mega serves as the microprocessor as well as a server. The control of the robotic vehicle is performed by means of different commands and applications.

Index Terms:

Arduino Mega, Blynk, Internet of Things (IoT), Local Area Network(LAN), Tele-Robotic, Wi-Fi

1. INTRODUCTION

Growth in the advanced technologies has resulted in the reduction of the human efforts. Robots are playing an important role in our regular life. Robots has wide applications in the field of industries, agriculture, military, home automation and many more. Arduino is a open source, user friendly platform which provides the flexible development kits and schematics. Arduino can be used by anyone without having more knowledge of coding. Arduino is based on C and C++ coding. Arduino helps in making the interactive environment with the use of different sensors and different modules. It can also easily interface with the internet. Robotic vehicles can be carried by an individual as they are light in weight and portable [6]. Using Arduino has the lesser limitations and more reliability. It can be used in the real time operation.

The cloud service makes the interface more easy. There is no problem of jamming in cloud as it uses two queues for functioning one to transmit the data and another to receive the data. ESP8266 Wi-Fi module easily gets interfaced with the Arduino. Android Blynk application is used as remote control installed in a mobile and can be used at the user end to give the commands to control the movement of the robotic vehicle as well as pick and place operation. Cloud robotics is a centred technology used for the greater memory storage, operates in two way communication without jamming for the robotic applications [8]. The robot has its application in military. At present in the war like environment and in the hazardous situations robotics play a important role by saving the human life. These robots are helpful for object pick and place, obstacle and leakage detection [1]. The vehicle can be easily located in its user interface and the user can continuously fetch the feedback data related to the vehicle [3]. The use of Internet does not have any limitations of range as if we have the internet access, we can control the robot from anywhere as the project is totally based on IoT. The video captured by the IP camera should be processed very fast to provide real time visualization of the surrounding to the user. Also the pick and place operation is done in a clean manner with the use of soft catching gripper. The Internet of Things (IoT) is a wireless technology connecting everyday accessible physical objects to internet. IoT wide spreads the connectivity of internet through the mobile phones, sensors, laptops, actuators etc.

Paper [1] presents a synopsis on robot rescue in the application domain of the Human Robot Integration (HRI) and also present the HRI issues. Paper [8] presents a robotic vehicle able to move in multiple directions by means of commands using Raspberry Pi as master and Arduino Uno as slave and internet for Wi-Fi. Paper [9] presents a Internet of Things (IoT) robotic arm where the robotic arm is controlled by a nurse in the hospital in the guidance of a doctor by the time of operation and can also perform pick and place task.

2. FRAMEWORK OF THE SYSTEM

Arduino Mega is a open source microcontroller used to observe the tasks through sensors, actuators etc., send the commands to the user end and operate the robot according to the user commands. It is powered by micro USB cable.

The robotic unit consists of DC motors, Arduino, ESP8266 as a Wi-Fi medium, dual arm soft gripper, an IP camera, the H – bridge L293D motor driver module. The User end consists of a android mobile with internet, Blynk application and IP camera application. Blynk application is the intermediate remote between the user and the robotic vehicle. The user adds the virtual pins in the Blynk app according to the application, by pressing those virtual pins on the app firstly the commands go to the cloud and then to the Arduino through ESP8266 Wi-Fi modem and then for example to the DC Geared motors [7]. With the help of online video surveillance it is possible for the user to take the right decisions for the movement of robotic vehicle as well as can do the task of pick and place. And this is the presence of tele – robotic system in the project.

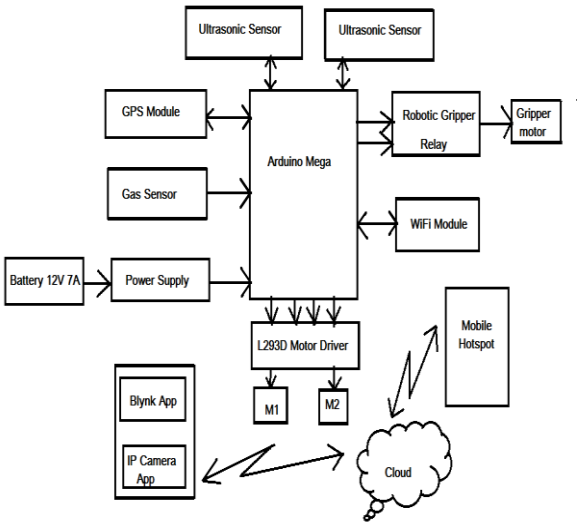

Figure 1 : Block Diagram of IoT Based Dual Arm Tele-Robotic System

3. CONSTITUENT SUB MODULES

Microcontroller:

Arduino Mega is used as a microcontroller. It is a user friendly mini-computer. Arduino is based on simple and user friendly basic programming languages such as C and C++. It has 54 digital inputs/outputs and 14 analog inputs/output pins. It has 3 serial ports which are necessary for our project to connect with Wi-Fi module, GPS module and the ultrasonic sensor.

Power Supply:

The robot requires 12V 7.5 A battery. As the DC geared motors operate on 12V and the IP camera requires 2A of current. By doing a research on the current and voltage distribution for the robotic vehicle we require this power supply battery. It is a rechargeable battery.

Sensor Module:

The sensor module comprise of the ultrasonic sensor and the MQ-6 gas sensor. Arduino takes the appropriate action according to the commands given by the user. For example: it continuously senses the forward and reverse distance to avoid any obstacles. GPS locates the location of the robot. Gas sensor continuously senses gas in the environment.

- Ultrasonic sensor: 2 ultrasonic sensors are used. One for the forward obstacle detection and another for the reverse depth detection. Ultrasonic sensor transmits the signal(triggers) and when obstacle detected receives(echo) the signal. It can detect the obstacle on 2cm to 400cm distance.
- MQ-6 sensor: MQ-6 is a gas sensor. It can detect the harmful gases like LPG, propane, iso – butane present in the application field.

Communication Module

Communication is possible with the use of ESP8266 Wi-Fi module. Cloud interface makes possible the Internet of Things. The Wi-Fi module enables both video as well as the data transmission by using Blynk and the camera app. GPS helps in tracing the location of the robot. The commands are send manually through the Blynk application. The Blynk app is installed in the mobile. It is interfaced with cloud to the robot which is present in the application area. Virtual buttons are present on the Blynk app just by pressing the buttons the action takes place in the application area via the internet medium. It can perform the operation of Forward, Backward, Left, Right, Pick, Place and Stop.

Robotic Car Movement:

L293D is used as a driving module. L293D is a H-bridge to drive two DC geared motors. The RPM of the motor decides the speed of the vehicle. 30 RPM motors are used to drive the robot.

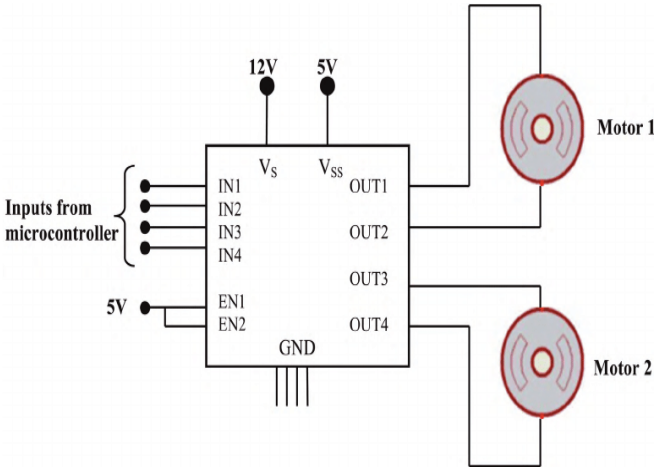

Figure 2 : Robotic Movement using H-Bridge L293D

Table 1: Robot Movement

Pin. No. / Sr. No.	18	19	20	21	Movement
1	0	0	1	1	Forward
2	1	1	0	0	Reverse
3	0	0	1	0	Right
4	0	0	0	1	Left
5	0	0	0	0	Stop

Pick and Place Module:

Object Pick and Place operation is most important rescue application in the field of robotics. It performs the jaw opening and closing of the dual arm gripper. A relay and a motor is assembled for jaw opening and closing. The working of a relay based DC motor is based on the H-bridge arrangement. The polarity within the load can be altered in both directions with the help of H – Bridge circuit. It works on the principle of Single Pole Double Throw (SPDT).

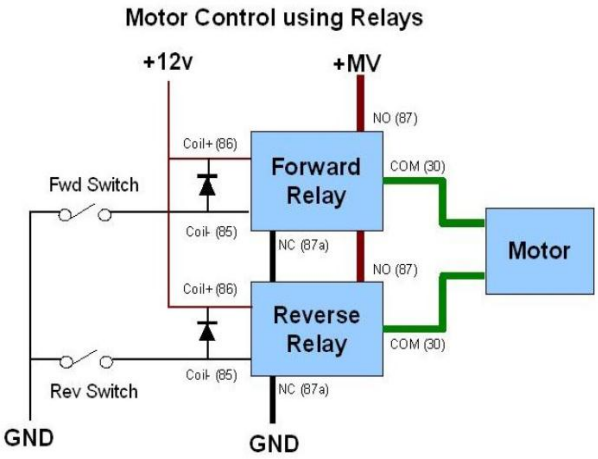

Figure 3: SPDT Working

The DC motor terminals in the motor driver circuit are connected between the common poles of two relay in the SPDT motor driver circuit. The Normally Open (NO) of both relay are connected to the positive terminal while the Normally Close terminal is connected to the ground or the negative terminal. Two PNP transistors are used in the circuitry connected to the coil carrying 5V supply.

Table 2: Modes of operation for jaw opening and closing

S1	S2	Motor Movement
0	0	Motor does not operate
1	0	Clockwise direction of motor means the Gripper jaw closes
0	1	Anticlockwise direction of motor means the Gripper jaw opens
1	1	Motor does not operate

Wireless Video Transmission Unit:

Wireless IP Camera is used for the surveillance purpose. It is mounted on the robotic car. An Internet Protocol camera is a high bandwidth digital video camera. It has its uses for online streaming, capturing and recording videos and for surveillance. Cameras which are capable to access surveillance over the internet connection are the Internet Protocol cameras or net cams. It is connected wirelessly through cloud service to the ESP8266 Wi-Fi module. Video can be continuously streamed on the camera application. Here in this project Mi Home security camera is being used. It provides with 360° horizontal view and 96° vertical view rotation. 1080 high resolution picture quality. It is a night vision camera with motion detection and can also record videos. It has the easy installation steps. Video can be streamed on the Mi Home application.

4. RESULT

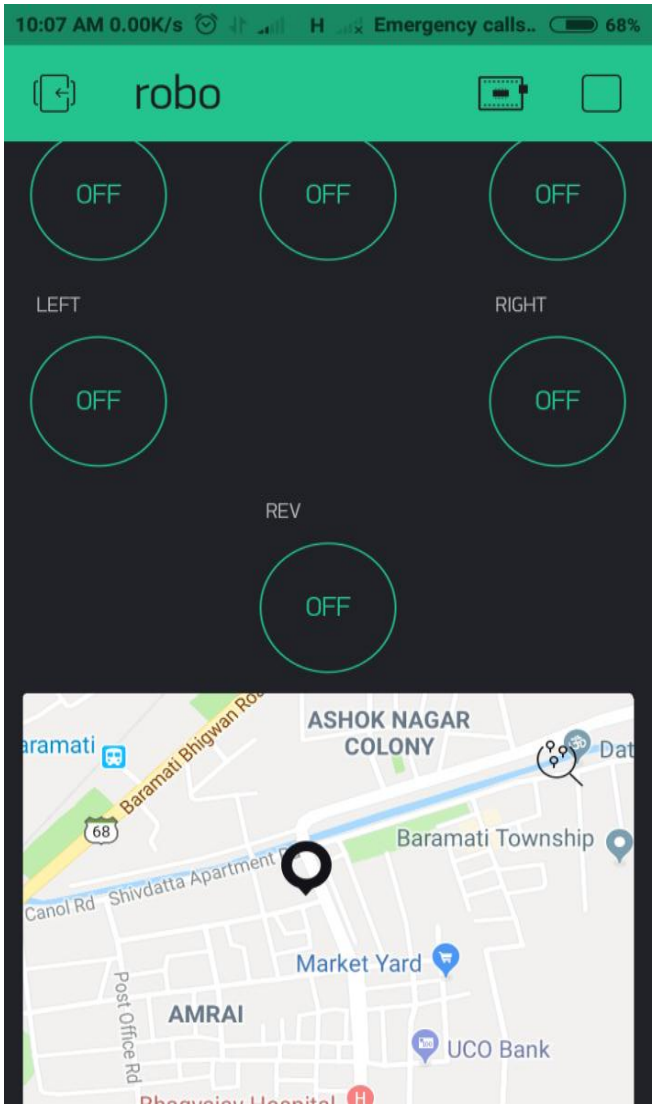

Figure 4: Screenshot of the Blynk application

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Figure. 4 shows the Screenshot of the Blynk application. It consists of different functional Virtual Buttons like forward, reverse, left, right, pick and place. It also shows the GPS map location in a single application.

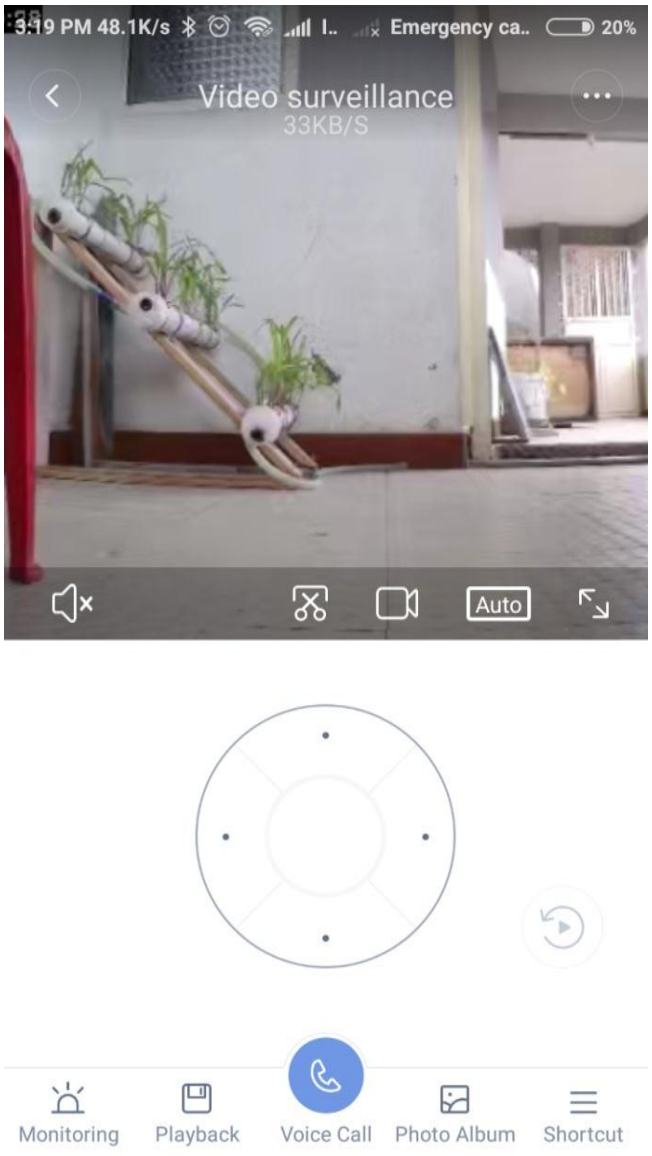

Figure 5: Screenshot of the camera app

Figure 5 is the screenshot of the camera application while capturing the online video.

Figure 6 : Image captured when pick command was given

Figure 6 shows the image captured when pick command was given. It holds the object in its gripper.

5. CONCLUSION& FUTURE SCOPE

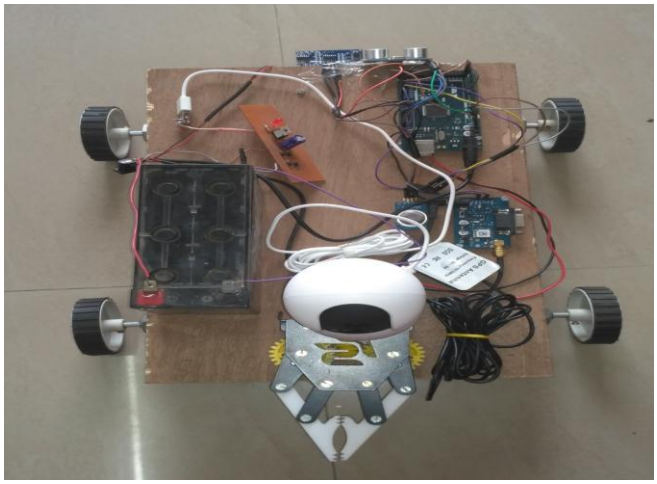

Figure 7: Image of the Proposed Hardware

In this paper, the framework for making a robot for pick and place and for surveillance purpose is successfully

implemented. The problem of limited range for surveillance is resolved by using the concept of IoT. The robot can be controlled with the help of mobile / laptop manually. Our proposed robot is small in size thus is portable into area where human access is impossible. Wireless technology is the most integral technology in the electronics field. This technology is used to serve our project as a supreme part of pick and place and surveillance act. This provides a cost efficient and highly effective robot that replaces human work and reduces human labour and performs monitoring works in a well effective manner.

In Future the project has advancement in implementing the following ideas:

- The robot can be implemented with a laser gun for the self defense and to protect our nation from enemies, the IP camera will do the surveillance immediately after detecting the enemy laser gun will shoot the enemy and this operation can be done automatically or manually.
- The robot implemented with artificial intelligence will be able to recognize the environment, the borders, the application field and if detects any intruders it can alert the human operators.

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A Comparison of SST Converter Topologies: Control & Modulation Techniques

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Abstract:

The Solid State Transformer (SST) is the emerging power electronics based key component of distribution system. In this paper a comparison of SST converter topologies with control and modulation techniques is presented. The main focus is on the use of SST for various applications based on the features offered by different converter topologies with different control techniques. The review is carried out by comparing these power electronics topologies based on their structure, advantages, limitations and their control techniques suitable for different applications such as green energy source integration to grid, traction, controlling of electrical machines, use as a Distributed Generators, due to powerful and attractive features of SST. The three stage SST is considered and compared for converter topologies with their control and modulation schemes which will help to identify the suitability of SST for the application.

Index Terms:

Solid State Transformer (SST), Conventional Transformer, Cascaded H- Bridge Converter (CHB), Dual Active Bridge Converter (DAB), Multilevel Converter, Smart Grid

1. INTRODUCTION

Before twentieth century, the development of distribution transformer by L. Gaulard and J. D. Gibbs got much prominence in ac power transmission and distribution systems. Liu G, Polis MP, and Wang B. have worked on this concept of Solid State Transformer and received patent in 1999. Consequently series of researches has been carried out with multifunctional, multilevel, power electronics transformer with different control strategies, switching and modulation techniques in 1999 [16] consequently in 2005, 2006 and 2011.

The conventional transformer preferably used to perform operations as voltage transformation as per system requirement and loading conditions and isolation purpose. But the conventional distribution transformers shows saturation in the core and generate harmonics which may results in huge inrush currents and can create power quality issues due to increased nonlinear loads in the distribution system. This leads to addition of power filters which make the supply system complicated and expensive. Moreover, the conventional distribution transformer, being static device, does not play any dynamic role in compensating for voltage sag or swell. It does not have facility to integrate renewable energy sources as PV cells and fuel cells (dc sources).

The more focus is being given to design the smart grids with improved power quality [22] [23] (by mitigating voltage sags, reducing failures or interruptions) with increased efficiency. The Solid SST is the key solution for the smart grid with increased renewable energy sources penetration and electric vehicle and traction loads.

Considering these limitations present day researchers are focusing more on advanced power electronics structured transformer, SST, to provide high speed power processing. The SST is basically introduced as high voltage, high frequency transformer along with many other components such as power electronic devices, gate driver circuits, heat sinks, cooling circuits, control circuits and other ancillary devices and systems.

The major scheme of SST is expected to provide various functionalities consist of potential features like power quality improvement at sensitive load, fault isolation, fault current limitation, instantaneous voltage regulation, etc along with availability of various ac and dc voltage levels to integrate DGs.

For the penetration of distributed green energy sources SST is being treated as one of the widely advanced modern research interest [8] [9] [10]. The research study is segregated in to two ways as one is to develop the architecture and modeling of SST and another is to determine the suitability of Solid state Transformer for various applications [13].

In recent years, most of the research is focused on the applications of SST with different power electronics converters build transformer as Solid State Transformer. Several researchers are finding the applicability and suitability of the SST for various applications. Edward R. Ronan et al. [17] have implemented prototype of SST to confirm the desirable features as improved power quality,

reduced size of system, power factor improvement, self protection which are unavailable in conventional transformer.

D. K. Rathod has presented the discussion about the extending Solid State Transformer (SST) through analysis of recent expansion in the field of power system [4]. The various SST configurations have presented with various converter topologies such as single stage, two stage and three stage SST for both LVDC and HVDC. They have identified future benefits of SST for integration with other systems and also used to enhance the use in MV and LV applications. The conventional transformer having disadvantages such as bulkiness, core saturation for variable load, low voltage regulation issues can be lowered by SST as an intelligent transformer. Subhadeep Paladhi and Ashok S. have discussed the application of SST for green energy as wind energy based distributed generation system [13]. The general traditional way of wind power integration to grid and SST interfaced wind farms have discussed with modeling of advanced SST system includes converter stages. The discussion has carried out by case study of practical data of wind farm with layout of the system. The system have analyzed with SST for active and reactive power control using simulation tools [11] [12]. Arindam Maitra et al. [20] have analyzed potential of SST as development of 100 kVA, 15 kV prototype of Intelligent Universal Transformer (IUT) with different features as high frequency AC service as well as DC service and discussed impact on a wide range of applications such as electrical vehicles, PV integration, distribution transformer, energy storage interfacing, with reliable and secure communication.

In this paper different multilevel converter topologies for SST have discussed and compared for different applications. Though the proper converter topology selection is important, it is most important to select suitable switching control techniques for acceptable performance of system expecting capacitor voltage balancing, switching of semiconductor devices, bidirectional power flow, efficient and reliable operation. The SST can be used alternative to conventional transformer having wider area of applications.

The discussion about various SST converter topologies, their control schemes, comparison on different basis has presented in different sections. The introduction of current scenario in the generations of power electronics converters has discussed in section 1. Followed with this, in section 2, the disadvantages of classical transformer, actual concept of SST and its advantages have explained and compared. The detailed descriptions of different converters with their controlling methods have reviewed in section 3. In section 4 concluding remarks have highlighted.

A. Disadvantages of Classical Distribution Transformer:

The typical distribution transformers have the following disadvantages:

1. Bulky size and heavy weight
2. Considerable voltage drop under load
3. Large inrush currents due to harmonics produced by core saturation
4. At average operation load produces relatively high losses.
5. Power quality issues
6. Poor voltage regulation at distribution side.

B. Advantages of SST over traditional transformer:

The SST provides superiority over conventional distribution transformer due to following feature:

1. Volume and weight reduction
2. Voltage sag compensation
3. Fault isolation, limiting fault current
4. DC Output
5. Power quality improvement at sensitive loads
6. Outage compensation
7. Instantaneous voltage regulation
8. Power Factor (PF) correction
9. Metering or advanced distribution automation
10. The above listed features can be accomplished by employing the conception of SST.

2. SOLID STATE TRANSFORMER STRUCTURE

The Solid State Transformer (SST) is a power electronics interface which combines converters, medium or high frequency transformers, and controlling circuitry. The primary thought is to replace the 50Hz or 60 Hz traditional transformer with a medium or high frequency transformer that can facilitates an important decrease in weight, size and volume.

The SST is an advanced component or system which consists of multistep converter isolated with high frequency operated transformer. The SST structure is illustrated in fig.1 consist of AC/DC, DC/DC and DC/AC converters from where integration to AC grid is possible.

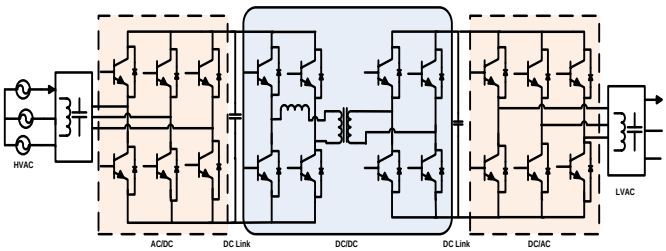

Fig. 1: Solid State Transformer Structure

The SST can be designed with various combinations of converter topologies such as Cascaded H bridge (CHB) converter, Dual Active Bridge (DAB) converters, Modular Multilevel Converters (MMC) etc as depending on the applications and suitability [15].

3. SST COVERTER TOPOLOGIES

The SST consists of multi-stage such as AC/DC, DC/DC and DC/AC. The SST can be formed by various ways using different combinations of these converters. In this paper Three stage SST is described. For these three different stages different types of converter topologies and their modulation schemes have discussed.

The first stage of SST consist an AC/DC converter stage may be designed with following converter topologies:

1. Diode Clamped or Neutral Point Clamped Converter (NPCC)
2. Flying Capacitor Converter (FCC)
3. Cascaded H Bridge Converter (CHBC)
4. Hybrid Modular Multilevel Converter (MMC)

The topologies are shown in fig 2(a - d). The Diode Clamped or Neutral Point Clamped Converter (Fig. 2a) has simplest structure due to only one isolated DC source requirement. This topology can regulate the reactive power and uses fundamental frequency for switching operation. But due to more number of diodes system becomes impractical and due to capacitor unbalancing the active power control is difficult. The similar topology is modified with clamped capacitor (Fig.2b) instead of clamped diodes. So that it reduces the THD and enables active power balancing and compensation of reactive power. But because of more number of capacitors the system becomes bulky, complex as well as expensive. The advanced converter is designed by connecting series full or half bridges providing separate DC source which offers more simple and scalable structure (Fig. 2c). In most of the power electronics systems such as integration of renewable energies to grid [7] [14], Solar and wind hybrid system, Cascaded H bridge multilevel inverter/ converters are used. The Modular Multilevel Converter is advanced hybrid converter topology (Fig. 2d) which consists of cascaded half H-bridge cells as submodules and two level converter combination. These submodules minimize the THD so that it eliminated the need of filters of large size. It provides the suitability for applications such as motor drives, HVDC etc. [5]

The control strategies for first stage of SST converters can be designed with the different schemes illustrated in fig. 3. The Phase Shifted PWM is particularly developed to control Cascaded H-Bridge Converter [6] which consists of multicells. The Level Shifted PWM provides better harmonic cancellation than Phase Shifted PWM. It is of three types as Phase Disposition PWM, Opposition Disposition PWM and Alternate Opposition Disposition PWM.

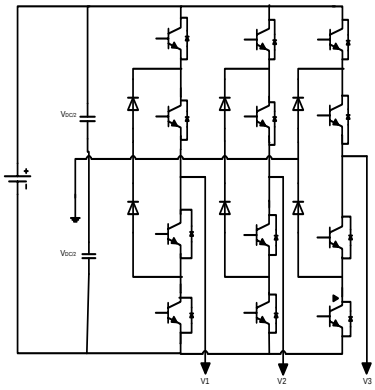

Fig. 2a: Neutral Point Clamped Converter

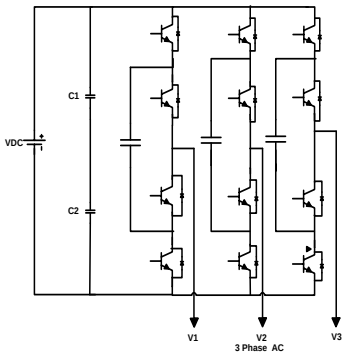

Fig. 2b: Flying Capacitor converter

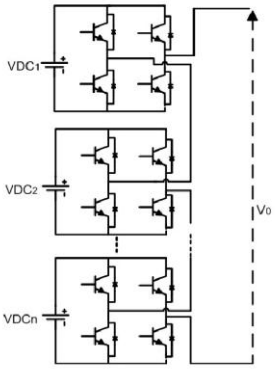

Fig. 2c: Cascaded H bridge Converter

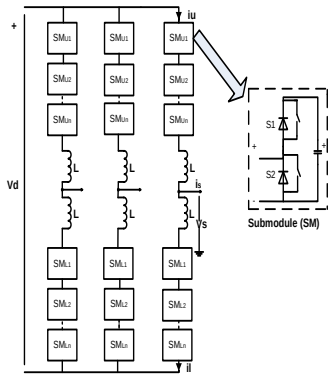

Fig. 2d: Modular Multilevel Converter

Fig. 2: First Stage: AC/DC Converters

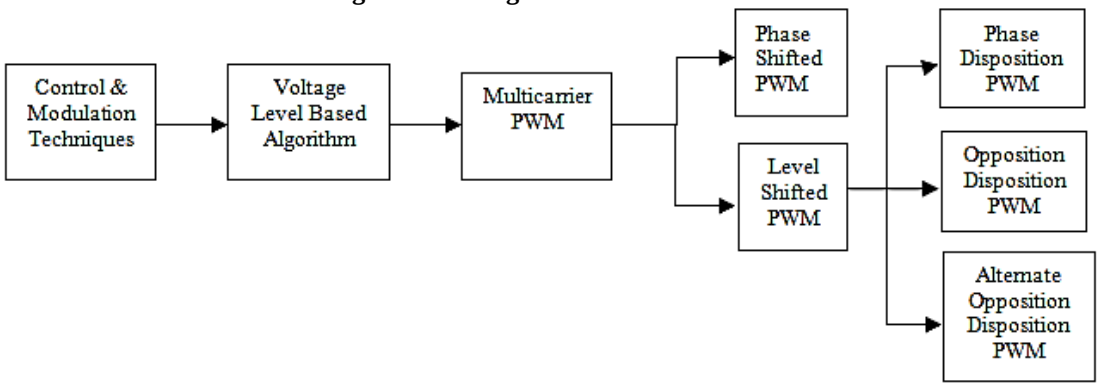

Fig 3: Modulation Techniques for AC/DC Converters

The second stage of SST comprised of DC-DC converter. This stage is generally developed with different converters such as Dual Active Bridge Converter (DAB), LLC Converter as illustrated in Fig. 4 (a & b). The Dual Active Bridge Converter is structured with 1 phase and 3 phase. It consists of two full H- bridges at primary and secondary of High or Medium Frequency transformer [1] [2]. It consists of lower number of passive devices, so employs soft switching properties. The 3 phase DAB converters achieve better efficiency than 1 phase DAB converter. J. Y. Lee et al. [18] have proposed SST as new Intelligent Semiconductor Transformer (IST) with bidirectional resonant converter. This system have tested with 2 kVA prototype which features as good voltage balancing with simple control for bidirectional power flow but the system performance efficiency improvement is the scope of future work.

The LLC converter is a DC-DC resonant converter consists of series connected capacitor with transformer leakage inductance to prevent the saturation of transformer. It provides better efficiency but the switching frequency becomes uncontrollable at no load condition.

These converters are operated with modulation schemes as shown in Fig. 5. The Phase Shift Modulation has simple operational algorithm and can transfer highest power but causes higher losses al low power levels. The Trapezoidal Modulation minimizes the switching losses but shows higher conduction losses and has complex control and modulation algorithm. As compared to Phase Shift Modulation the Triangular Modulation provides lower switching losses but requires complex switching control and modulation algorithm.

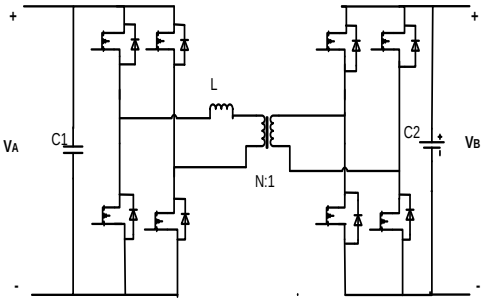

Fig. 4a: Dual Active Bridge Converter

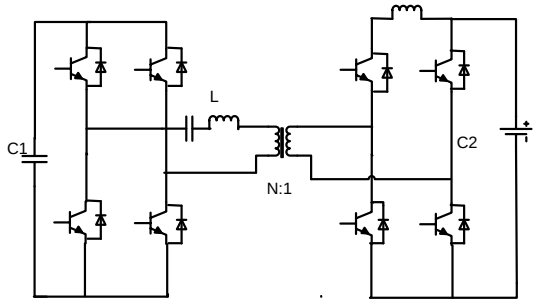

Fig.4b: LLC Converter

Fig. 4: Second stage: DC/DC Converters

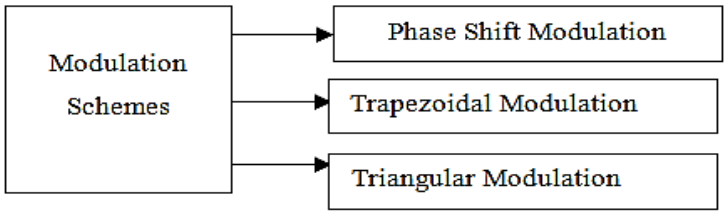

Fig 5: Modulation Techniques for DC/DC Converters

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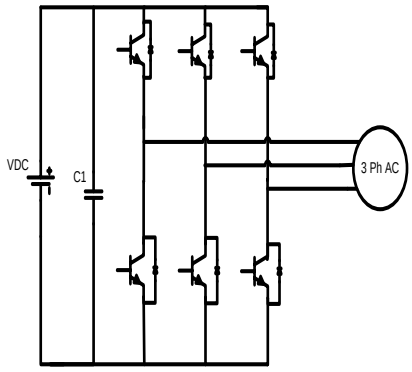

Fig. 6a: Conventional 3 phase converter

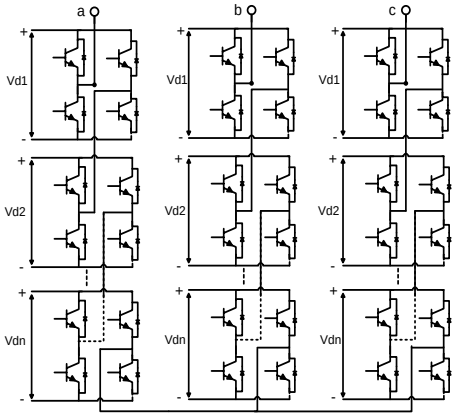

Fig. 6b: Three Bridge converters in Parallel

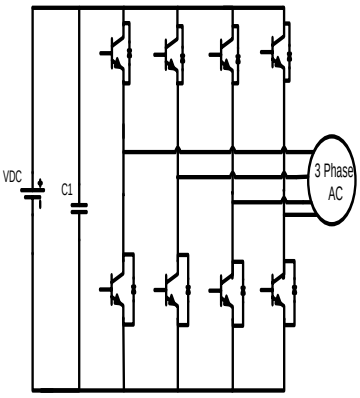

Fig. 6c: 3 phase 4-Leg converter

Fig 6: Third stage: DC/AC Converters

The third stage of SST consists of DC- AC converter. It can be employed with different converter topologies such as conventional 3 phase converter, 3 bridge converters in parallel combination, 3 phase 4-leg converter etc. as illustrated in fig (6a-c). The 3 bridge converters connected in parallel may be consisting of half bridge cells or full bridge cells. It requires lower number of switches and lower DC link voltage but causes voltage imbalance issues. The conventional 3 phase converter does not require separate DC source like CHB converters but causes voltage unbalance across capacitors. The 3 phase 4 leg converters minimize the problems of capacitor voltage unbalancing which is the disadvantage of conventional 3 phase converter by adding another switching leg. This topology requires complex control technique. This topology shows suitability for applications of unbalanced loads.

H. Iman Eini et al. have presented SST as Power Electronics Transformer (PET) with cascaded H bridge converter topology for critical loads. The results have analyzed for conferment of usefulness of PET for power quality improvement. The system provides the scope to research on improvement of efficiency at isolation and output stages. Yashan Liu, et al. [19] have proposed model predictive control for SST designed with two 3ph to 1ph matrix converter based SST. The system has analyzed carrying out simulation studies with variable voltage and load power variations. The control strategy employed reduces complexity of other traditional control and modulation strategies with improved performance of SST.

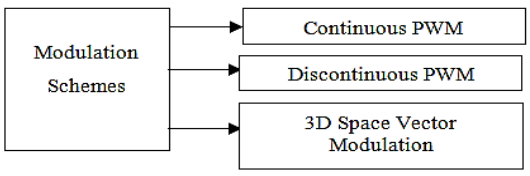

Fig 7: Modulation Techniques for DC/AC Converters

These converter topologies can be designed with different modulation techniques as shown in fig. includes Continuous PWM, Discontinuous PWM and 3D space vector modulation. The Continuous PWM provides easy and simple algorithm and implementation. The Discontinuous PWM enables low switching losses and low THD. The 3D Space Vector Modulation requires complicated calculations and control algorithm.

4. CONCLUSION

In this paper the various converter topologies with its control and modulation techniques have discussed with the structures. Thus the combination of converter topologies and its control and modulation schemes for SST suitable for various applications such as drives control, integration of renewable energy sources to grid, electrification, for fault tolerant applications depends upon the features, advantages and disadvantages of it. The most suited converter topologies for three stages of SST are Cascaded H Bridge converter, Dual Active Bridge Converter with Phase Shifted Modulation and 3 phase 4 leg converter with Continuous Pulse Width Modulation respectively for three stage SST suited to various purpose and applications. The SST offers various features which may leads the maximum research in various transmission and distribution applications.

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Design and Performance Analysis of Equal and Unequal Power Divider for ISM Band Frequency

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Abstract:

In this paper broadband and compact power divider is presented. The proposed circuit made up of two micro strip transmission lines. A pair of low and high impedance lines for equal and unequal power-dividing ratios. The proposed power divider exhibits arbitrary and non-arbitrary power divided ratios. Design equations for proposed circuit power division ratio cases are given. For the equal ratio case, two symmetric coupled Micro strip lines required. The unequal ratio case, two asymmetric coupled Micro strip lines required. Proposed power dividers has been study and investigated. The proposed Hybrid power divider operating at 2.4 GHz with power dividing ratio of 1:2 and 1:4 are designed, fabricated, measured respectively. The measured results are in good agreement with the simulated results. The power divider has been designed on FR4 dielectric substrate with relative permittivity εr=4.4 and thickness 1.6mm. The designed power divider miniaturized by using the T-shaped feed techniques. The overall size of the power divider is 42mm * 86mm*1.6mm3. The results shows that the isolation between output ports is found to be better than –15 dB and return loss at each port is less than -10dB.

Index Terms:

Power divider, isolation, insertion loss, ISM band, miniaturization, transmission lines, circuit design

1. INTRODUCTION

Power divider is passive device mostly used for power division or power combing. This feed line network has two stages, first stage for equal power dividing ratio and the second stage for unequal power dividing ratio. So it has total four output ports. Both first and second stage has developed using Wilkinson technology. Transmission lines between output ports and in series with the isolation resistor. FR4 substrate is used to design a feed line network. The power divider is designed, simulated and fabricated which works for ISM band. Here HFSS software used for simulation. Wilkinson power divider is an idea form of divider for RF application. It provides minimum loss and maintains a better isolation between ports.

The length of transmission line that must be derived and the output ports can directly connect to the power divider. T-shaped micro strip lines have also been proposed to design power divider with high power dividing ratio. This approach replace micro strip lines have been replaced by the T shaped micro strip lines. The ability divider created is associate degree equal split 2 port device, whereas antenna arrays generally utilize quite 2 antennas.

Within the RF and microwave community, power dividers have served a distinguished role for years. The most perform of an influence divider is to separate a given input into 2 or a lot of signals as required by the circuit/system. A typical application for an influence divider is to separate a symbol to feed multiple low power amplifiers, so have the signals from the amplifiers recombine into a high power signal. Another power divider application and therefore the inspiration for this paper work, is among a phased antenna array system. During this system a symbol is either fed through associate degree equal split power divider that includes a particular range of output ports, or a series of equal split power dividers. The split signals are then fed through section shifters so to associate degree array of transmission antennas. The section distinction between every signal being transmitted permits for electronic beam scanning, permitting the transmitted beam to be centered in numerous directions relying upon the section distinction. The ability divider created is associate degree equal split 2 port device, whereas antenna arrays generally utilize quite 2 antennas. Consequently, if this power divider style were ever employed in associate degree antenna array, multiple power dividers would possible have to be compelled to be accustomed split the signal into quite simply 2 signals (i.e. 4, 8, 16, etc.) and more slender or focus the beam.

2. POWER DIVIDER CONFIGURATION

Simple model of 1:2 mcro strip feedline network

Figure shows that unequal power divider is formed using Wilkinson power divider technology. It is commonly used in several power dividers.

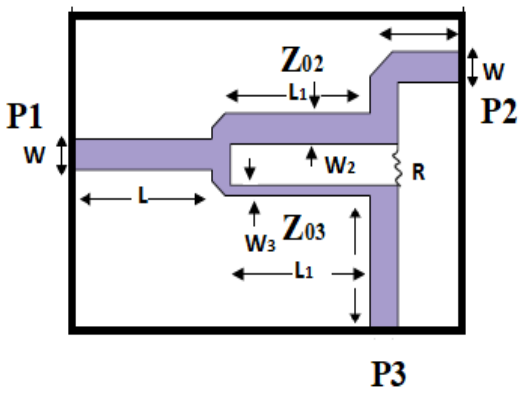

Fig.1 Design of unequal power divider

Figure 1 shows design of unequal power divider. Implemented by using an asymmetric micro strip transmission lines which is parallel to each other, including its various parameters and also shows the separated micro strip lines replaced by a uniform asymmetrical micro strip coupled lines.

F = 2.4GHz

εr = 4.4

h = 1.6mm

Guided Wavelength (λg) = c/f

λ= C/F ..... (1)

λ= (3×⟦10⟧^8)/(2.4×⟦10⟧^9)=125mm

Length of power divider (L1) is given by

$L1 = \lambda g/4\sqrt{\varepsilon r} = \frac{125}{4\sqrt{4.4}}$……..…..…..…(2)

sL1= 14.9mm

p3/p2=0.5(3dB)…..……(3)

$k^2 = \frac{p3}{p2} = \frac{1}{2} \rightarrow k = 0.707$……..……(4)

$Z03 = z0\sqrt{\frac{1+k^2}{k^3}}$……..(5)

$= 50\sqrt{\frac{1+0.5}{(0.5)(0.707)}} = 103.0\Omega$

$Z02 = k^2 Z03 = (0.5)(103\Omega)$……..(6)

$= 51.5\Omega$

$R = Z0\left(k + \frac{1}{k}\right) = 50\left(0.707 + \frac{1}{0.707}\right)$……..(7)

$= 106.1\Omega$

$Z0 = \frac{60}{\sqrt{\varepsilon}} \ln\left(\frac{8h}{W} + \frac{W}{4h}\right)(\Omega) \quad for \frac{W}{h} \leq 1$……..(8)

$Z0 = \frac{120\pi}{\sqrt{\varepsilon\left[\frac{W}{h} + 1.393 + 0.667\ln\left(\frac{W}{h} + 1.444\right)\right]}}(\Omega)$……...(9)

$for \frac{W}{h} \geq 1$

Zo is Impedance of microstrip line

Putting value of Z0=100 Ω in above equation we calculate

W3 =1.0mm

And putting Z0 =50Ω we Calculate W2 = 3.0mm

Table i. Dimensions of proposed power divider on fr4 milimeter

Dimensions	Values(mm)
L	15
W	3
L1	15
L2	13.5
G	4
LS	42
WS	68

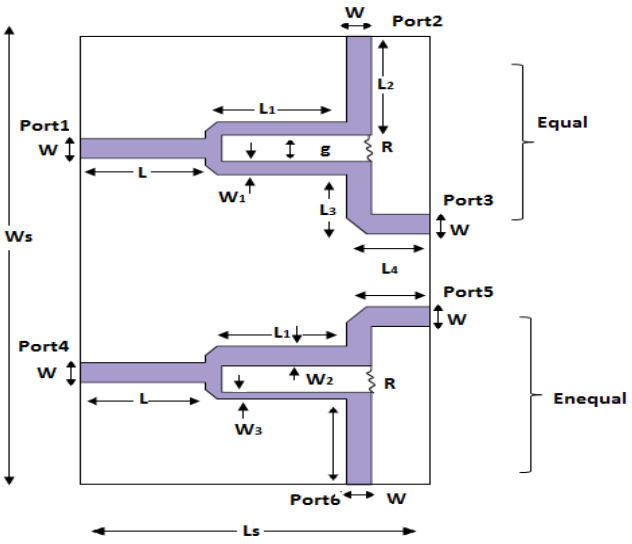

Fig.2. Design of a compact hybrid equal and unequal power divider

Figure 2 shows a compact hybrid micro strip power divider design using HFSS software. It has two different transmission lines .Maximum fractional bandwidth of designed power divider is 148% that can be achieved using wider the width of coupled line. In the power divider circuit design, resistor is placed between coupled lines to achieve good isolation between the output ports. When power incident at port1 then equal power ratio will be getting at port2 and port3 and power lunch into port 4 then unequal power will be getting at port4 and port6.

3. PHOTOGRAPHS OF FABRICATED CIRCUIT

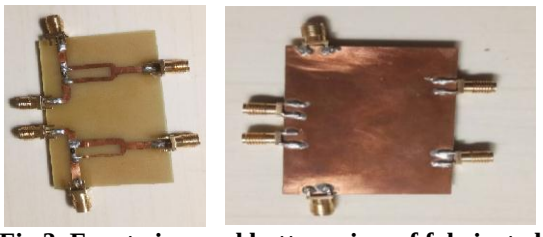

Fig.3. Front view and bottom view of fabricated circuit

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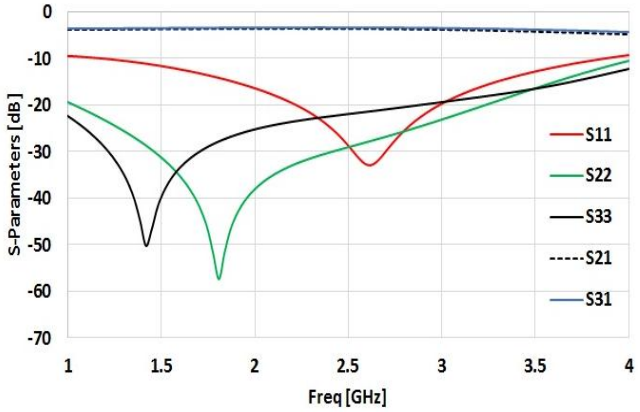

Fig.4. Simulated scattering parameters of designed equal power divider

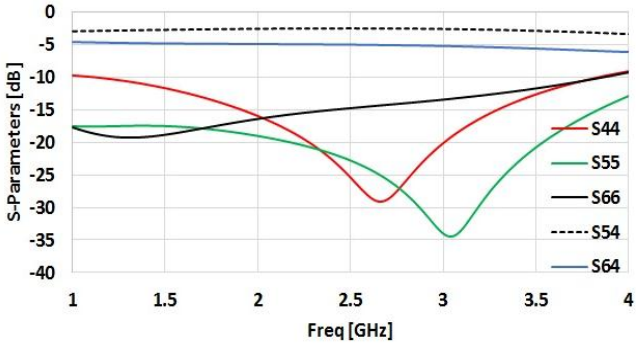

Fig.5. simulated scattering parameters of designed unequal power divider

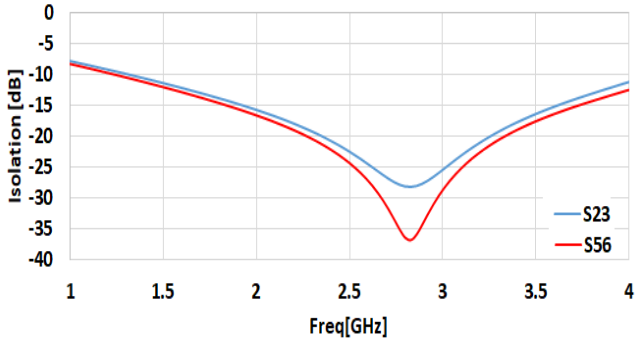

Fig.6. Simulated Isolation at scattering parameter (S23) and (S56)

Figure 6 shows simulated s-parameter unequal power divider using VNA for port (s_{23}) and port (s_{56}) at frequency 2.6 GHz isolation is above 25dB.

I(4,1)=-10log⁡[P4/P1]

4. EXPERIMENTAL RESULTS

On the other hand, PCB circuits are usually fabricated on FR4 which is cheap but on the expense of greater loss. Considering that substrates with varying thickness exhibit different loss and variations from the nominal dielectric constant, FR4 thin substrates with thickness h=0.5mm and h=1.6mm were tested

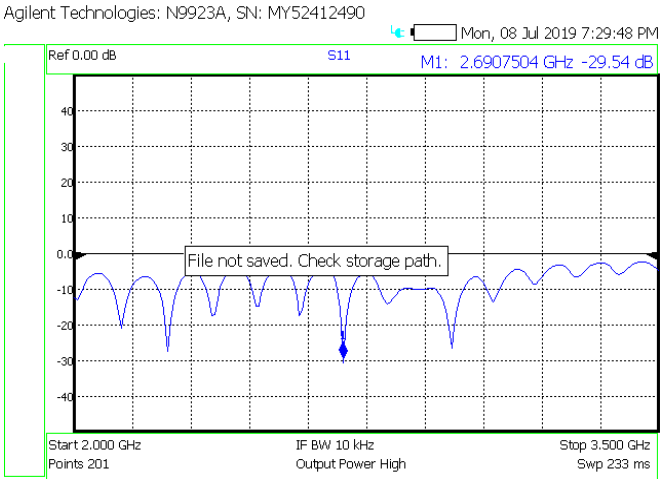

Fig.7. Scattering Parameter at Port (S_{11}) on VNA

Figure shows results of fabrication feed line network using VNA for port1 (s_{11}) at frequency 2.6 GHz return loss is -29.54dB. The return loss S (1, 1) is of 29.54dB at port 1

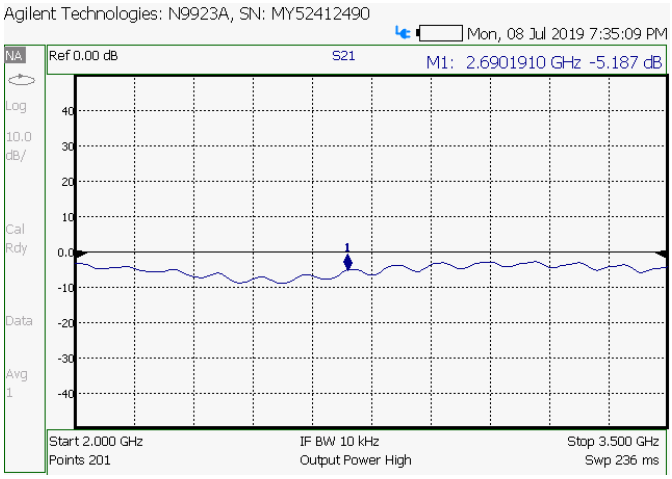

Fig.8. Scattering Parameter at Port (S_{21}) on VNA

Figure shows measured s-parameter of unequal power divider using VNA for port2 (s_{21}) at frequency 2.6 GHz insertion loss is -5.187dB.The experimental circuits were measured by the vector network analyzer.

5. CONCLUSION

This paper presents a Wilkinson power divider with equal and unequal power dividing ratio for high power applications. Based on theoretical analysis, power division ratio can be achieved by controlling the characteristics impedance of transmission lines. It can achieve good isolation between the output ports while maintaining a matched condition on all ports. The coupled power is 3.4dB at port2 and port3 over 1.2GHz to 3.2GHz at the output of

equal power divider and the coupled power is -3.4dB at port5 and -5.6 port6 over 1.2GHz to 3.2GHz at the output of unequal power divider. The proposed circuit can be utilized in related applications with power dividing requirements. Application of power divider is GPS, GSM, radar, distributed antenna system, real time location system, amplifier, filter, mixer, LNA, cellular, base station, radios, micro wave radio etc.

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Interactive Mirror

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Abstract:

This paper describes and explains the design and working of a mirror made smart called Interactive mirror built using raspberry pi. The visual representation of the product is similar to a regular mirror that can display weather details, temperature, time and daily news on voice commands. The smart mirror acts as a personal assistant, an enquiry center and displays important curriculum or college notices. It can answer basic questions, display class timetable and show directions to various places of an institute. It could be linked to google cloud for various IOT based tasks like home automation etc. It uses a proximity sensor to turn on the screen if in use and turn back off when not in use. Built on a strong speech to text engine, it understands various types of accents to understand predefined command clearly. The smart or interactive mirror designed by using a raspberry pi as the main controller and a led display that is placed behind the mirror, can serve a variety of endless application-based commands. With such a wide range of applications, this could certainly become an important part of technology in future times.

Index Terms:

Interactive mirror, notice board, personal assistant, enquiry center

1. INTRODUCTION

Mirrors are part of everyday used items that have been so far eluded from the idea of being smart. The idea of combination of mirror with intelligence and technology, discussing further possibilities and uses are some objectives of this paper. The smart mirror may seem to be similar to that of various other smart devices available like smart phones, smart televisions, smart lights etc. but have some certain and specific advantages because of its usage as a mirror. This interactive mirror is a still complex to that of an ordinary mirror, having a display inside a glass that one can interact with, using voice commands.

The mirror works with the help of a raspberry pi. There are several displays or notice boards present that are difficult to operate manually. The problem of finding places in new buildings were too a concern. This product acts as a solution for above problems. It also acts as an innovative and attractive object that can be placed in any surrounding.

A product that can inhibit all the qualities of a regular personal assistant on androids or laptops with application-based knowledge along with the above-mentioned problems with some suitable speech detection modules and speech convertor engines, all in a small processing power operating system as that of a raspberry pi (Debian).

Putting the tasks above in a simplified manner, three basic functionalities that would be fulfilled can be given as,

1. Personal Assistant

The mirror acts like a personal assistant. The mirror does various tasks like updating calendar, setting up reminders, updating date and time, displaying weather, daily news and other such general-purpose activities. It can respond to some of the commands like time, weather, news, Gmail, technology updates, college notifications, birthday, jokes, life.

2. Enquiry Centre

Basic questions related to any workspace are fed into the database. Such queries can be answered by the mirror. This enquiry center can be very helpful to people who are new to any workspace. These queries will be regarding finding the direction to any particular classroom, locating any professor etc. This can be an endless module as we can configure as many questions as we need. Thus, this can differ based on the workspace in which you are using this mirror.

3. Notice board

The mirror can be used for displaying various academic notices in the college. The product is linked with the android device of the administrator so that he can change the notice and information as and when required to be displayed. These notices are displayed according to various time slots.

2. LITERATURE SURVEY

Michael Teeuw's [1] was the first to build a smart mirror and first to use a raspberry pi for this purpose. The first smart mirror blog was posted back in 2014, since it was a very new product it gained a lot of attention back then. This mirror is built on raspberry pi 2 and uses monitor as the display. It displayed weather and time importing these from various modules which were linked to real time websites. It was just an information panel which didn't have the capability to interact with the mirror. A module-based interface was created and displayed weather, news, time or daily comic strip.

Ryan Nelwan [2] in the year 2016 gathered much interest and developed a smart mirror much similar to the

one developed by teeuw's. A new feature added to this was the touch feature which was a first of its kind. It serves mostly as a source of a entertainment system in which a user can use the touch controls to run different programs or control music, but did not have artificial intelligence.

Hannah Mittelstaedt [3] made a home mirror. It was posted on reddit website. The mirror used a smart phone as the display screen. Since it was an android tablet so features of android were used to display time, weather, date, remainders. The software made use of android widgets but can be modified easily as it is open source. Anyone can modify it and develop a new version. Home Mirror is a kind of smart mirror that is easier to build than other mirrors as it requires just two main components, any android mobile phone or a tablet and a mirror. However, this too lacked any kind of intelligence or interaction.

3. SYSTEM DESIGN

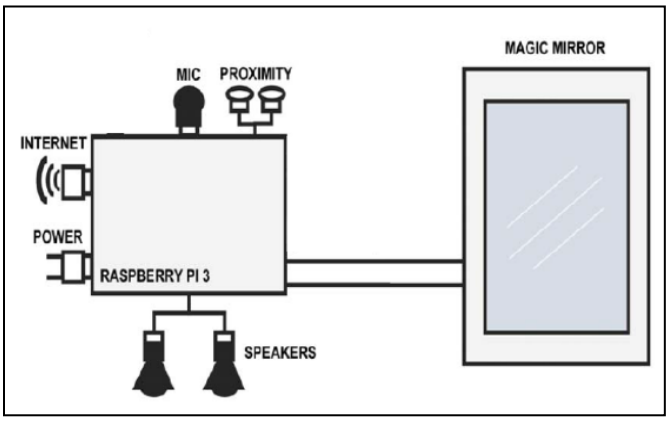

Figure 1-Block diagram

The software structure of the system is implemented and built using the web socket communication protocol. The architecture is modular and works on the basis of function designated modules which can be incorporated together on a single platform. With this, we can club many features such as clock, calendar, current weather, newsfeed etc., and many other third-party functionalities. The server module leads all the operations: interaction with the user through the sensors and the mirror user interface (UI), information visualization through the mirror UI etc.

A. Notice:

This module displays a random notice regarding any academic activities that are to be conducted in the college. The notification property contains an object with four arrays: 'morning', 'afternoon', 'evening' and 'anytime'.

B. Newsfeed:

This module displays news headlines based on a really simple syndication (RSS) feed. Scrolling through news headlines happens time-based (update Interval), but can also be controlled by sending news feed specific notifications to the module. An array of feed URLs are used as source. The URL of the feed is used for headlines.

C. Update Notification:

This will display a message whenever a new version of the Magic Mirror application is available.

D. Clock:

This module displays the current date and time. The information will be updated real time. It displays time in 24-hour time format. The time zone Asia/Kolkata is used for displaying time.

E. Current Weather:

This module displays the current weather, the sunset or sunrise time, the temperature including the windspeed and an icon to display the current conditions. The location feed for the weather information is Mumbai, Maharashtra, India. The weather information is obtained from OpenWeatherMap. It is an online service that provides weather data, including current weather data and forecasts.

F. Weather Forecast:

This module displays the weather forecast for the coming week, including an icon to display the current conditions, the minimum temperature and the maximum temperature. The URL used for this module is same as that of current weather module.

G. Weekly Schedule:

It displays today's timetable from a weekly recurring schedule of a timetable of particular class. It is intended for regular weekly schedules, which have a low update frequency and thus can be maintained manually.

H. Slide Changer:

This is an extension to the above modules, allowing the modules to be displayed in a rotating carousel instead of displaying all of them at once.

I. Alarm:

In this an array is created where all the alarms are treated as objects. These objects have properties like time, 24-hour format, days etc. A sound is set for the alarm and if the sound is not defined alarm will be fired with default alarm sound.

Along with these certain voice modules can be included which are accessible through voice commands. They are:

a. Technology news:

This module gives the latest technology news when asked by the user. Technology News is a social news website that caters to programmers and entrepreneur, delivering content related to computer science and

entrepreneurship. Jasper technology news will notify the user about the top 10 stories.

b. Status:

This module gives information regarding the status of the mirror like in which platform it is running, its current CPU utilization, current memory utilization etc.

c. Message queuing telemetry transport:

When triggered it publishes a simple message queuing telemetry transport (MQTT) event. The available devices are room, door and the available messages are on, off, true, false, open, close.

d. Reboot and Shutdown:

Used to reboot and shutdown the raspberry pi using voice

4. WORKING OF PROJECT

For the hardware architecture, a Dell computer monitor, a two-way mirror, a Raspberry Pi model 3B, USB microphones, jack speaker and a proximity sensor are used. Everything was put together in a wooden frame. The entire structure is divided into two wooden parts constructed as a box type structure. The behind part holds the display screen and the Raspberry Pi and is used to support the device so that it can be hung on a wall. The forward portion of the box type structure is made using the glass which is made to fit entirely in front the screen.

The major components that are used (the two-way mirror glass, display, Raspberry Pi, microphones, proximity sensors and frame) and how they are used is described in the following sections:

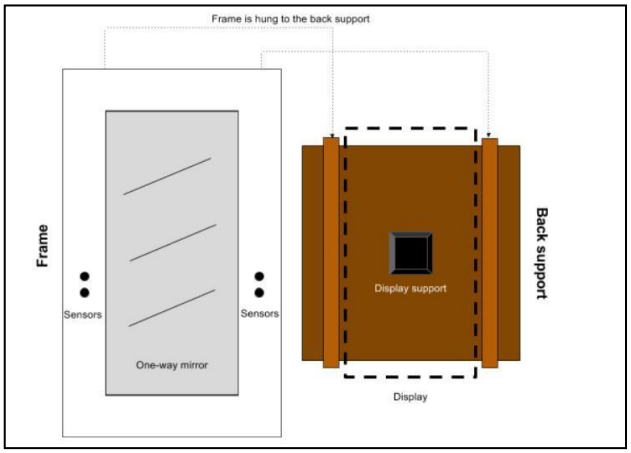

Figure 3-Hardware design

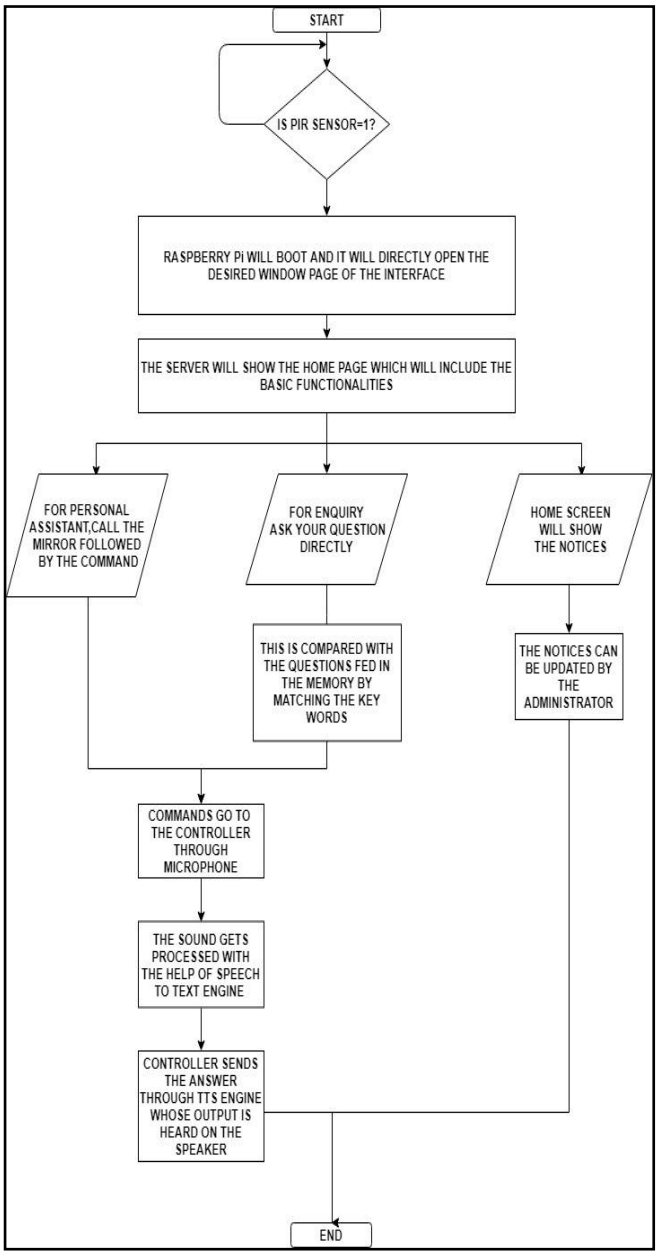

Figure 2 - Workflow diagram

1. One-way mirror

The glass used at the front end of the box is probably the most important part of the device or hardware as it is this that is responsible for creating the futuristic and artistic effect and is the biggest part of the smart mirror. Here for it to attain the qualities of reflection and refraction, a dark background surface is needed in which light parts or portions will be visible normally.

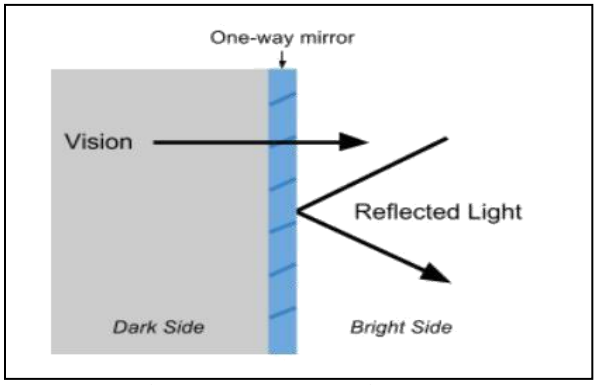

Figure 4-One-way mirror

2. Display

For the display a Dell monitor is used, comes with a remote control which is useful to easily turn off the device's screen. The monitor is much smaller than the mirror so a black sticker is used to cover the parts of the glass which are not covered by the display. An HDMI to VGA cable was used to connect the display to the Raspberry Pi for video and audio.

3. Raspberry Pi

The Raspberry Pi is a single board computer developed by the Raspberry Pi foundation in the UK. The Pi does not work out of the box. It lacks a hard drive and it does not come with a preinstalled operating system. To install an OS microSD card prepared with an OS image is needed. And because the software that runs on the mirror is coded on the same device at least a screen, a keyboard and a mouse are required.

4. Microphones and Speakers

One mode of interaction with the smart mirror is through microphones. USB microphones is used because the Raspberry Pi does not have a regular microphone input. Speaker can easily be connected with the output jack port of the raspberry pi.

5. RESULTS

Figure 5-Home screen

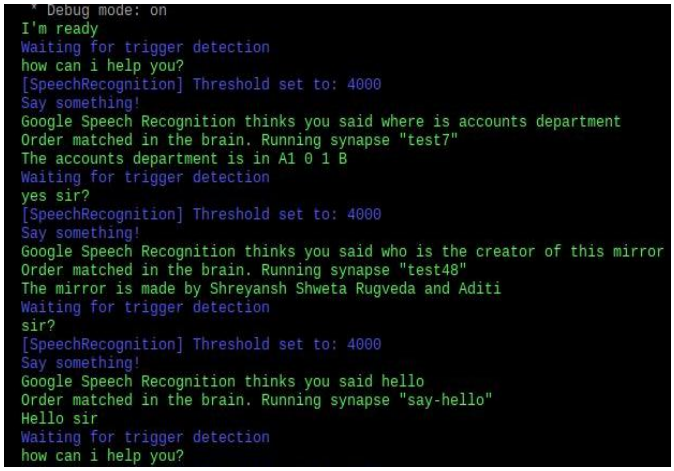

Figure 6- Voice interaction

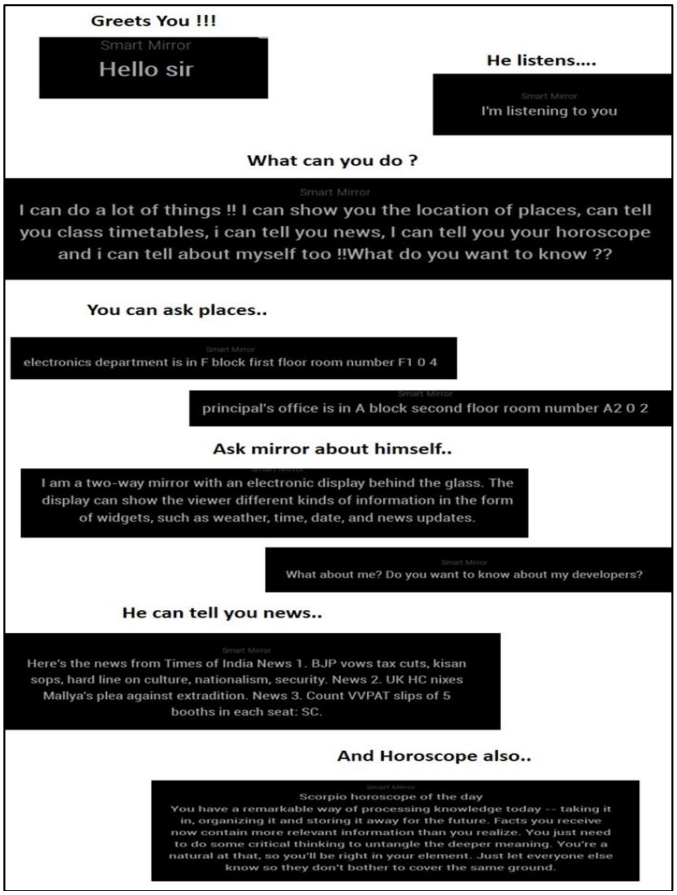

Figure 7-Voice interaction

6. CONCLUSION

The smart mirror which acts as a smart home control platform is a futuristic system that provides users with an easy-to-use mirror interface, allowing users access to customizable services in a highly interactive manner, while performing other tasks simultaneously. The main strengths are that this is a new kind of smart device that people don't see every day and it looks very spectacular. The mirror

works both as a normal mirror as well as a mirror showing daily notifications to the authorized user. There are lots of feeds or notifications that the user can view on the mirror like Facebook, Gmail, news etc. The mirror is also used to display time, weather, date etc. The mirror also acts as a personal assistant as well as displays important notices and is also an enquiry center. The user can interact with the mirror using voice commands. Also, a PIR sensor is attached which turns on the screen only when the user is in the proximity range of the mirror. This reduces power wastage. Smart mirror design has the advantages of small size, simple operation, low cost, high degree of user friendly, personalized user interface and many other advantages which is suitable for many applications like college, home, offices etc. Overall, the proposed smart mirror system incorporates various functionalities to grant users access to personalized information services.

7. FUTURE SCOPE

Nothing is perfect and complete and there is always a scope of improvement in each and every product. Everything needs to be updated or upgraded on a timely basis to cope up with the current technology. Apart from up gradation there can be many other features as well which could add up to the proficiency and ability of our smart mirror. There are many future scopes for this paper and hopefully it will emerge into biggest benefit in the field of artificial intelligence. The most basic feature can be smart mirror-based home automation which will provide a natural means of interaction by which we can control the household appliances like switch on/off light and fans through basic voice commands. Majorly, since we are using this mirror in college environment, basic functionalities like barcode scanner or finger print sensor can be integrated to fulfill basic tasks such as college attendance or program registrations etc. This could include registering in programs by scanning of ID cards.

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Energy Efficient Digital Circuit Based On Self Cascoding Positive Feedback Adiabatic Logic for Low Power VLSI Design

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Abstract:

Emphasis in VLSI design has shifted from high speed to low power due to the proliferation of portable electronic systems. The continuing decrease in feature size and corresponding increase in chip density and operating frequency have made power consumption as a prime concern in VLSI design. For ultra low power applications, the idea of self cascode positive feedback adiabatic logic (SC-PFAL) has reported as a promising candidate to reduce power dissipation at low operating frequency. To enhance the energy efficiency of the logic circuits, self cascoding of transistor is applied to charge recovery logic working in sub-threshold region. Based on this proposed technique, we design a basic MOS digital library cell. Simulation results are found using 70nm technology model file available from predictive technologies. At low clock frequency, the proposed logic i.e. SC-PFAL has significant improvement in terms of energy consumption than original PFAL.

Index Terms:

Charge recovery logic, PFAL, Self cascode, Ultra-low power

1. INTRODUCTION

Due to increase in complexity of the chips day by day the challenge to reduce the power dissipation results in limiting the functionality of the computing systems. With the advent in the era of communication system where multiple devices are continuously exchanging data with each other, technologies like IOT demands for ultra low power consumption. Portable and handheld devices needs high speed computation with low power consumption as most of the devices are battery operated. There must be a trade off between speed and power for optimization of a circuit as higher speed leads to higher power dissipation and vice versa. While focussing on the performance and area for VLSI chip design, power dissipation is a prime factor which must be given importance. Many techniques are used for optimization of power among which adiabatic logic is a promising technique to reduce dynamic power loss in digital systems. Reduction in energy loss is achieved by returning back the major portion of charge supplied by the power supply by restricted the charge to flow to the ground terminal. [1].

The charge flow in conventional CMOS logic is from supply to ground terminal through parasitic capacitances, while in case of adiabatic logic, a major portion of the energy supplied by battery is returned back to the supply as shown in Fig. 1[2]. We can also reduce the power consumption by keeping the system to work in sub-threshold region by reducing the supply voltage below threshold level (V_{TH}) of a transistor resulting in reduction of power without sacrificing noise immunity and driving ability [3]. These two techniques can work together to

accomplish ultra low power VLSI systems. These systems work at power clock frequencies range from a few Hundreds of hertz to a few Megahertz. The power consumption can be in range of few pico-watts. These systems are suitable for the domain where low power consumption is more important than the processing speed [4], such as biomedical application which typically works at clock frequency below one MHz [5].

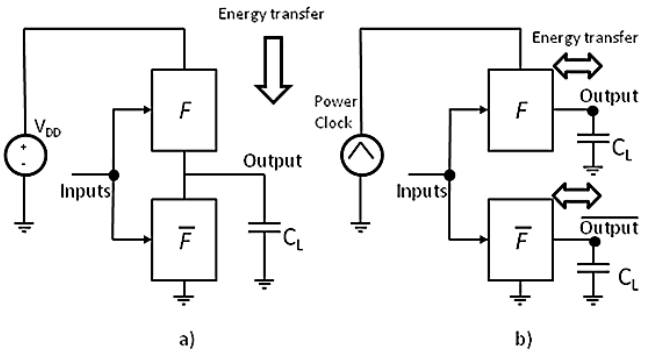

Fig. 1 The energy flow in a) conventional CMOS logic and b) Adiabatic logic

The adiabatic logic family has different members like 2N2N2P [6], ECRL [7] and PFAL [8]. These adiabatic circuits have latch based structure. The positive feedback in the latch ensures that system will attain either of the two stable states and avoid logic level degradation at the output

nodes [9]. The performance of the latch depends on its loop gain which is of the order of $(g_m r_o)^2$. The reduction in output impedance due to channel length modulation effect is a big issue for highly scaled devices [10]. This effect directly reduces the loop gain of the latch. The loop gain can be increased using cascoding of MOSFETs. The cascoding of transistors also reduces the leakage current and further improves the efficiency [11]. Regular cascode may not be suitable in highly scaled devices, as the supply voltage available may be of order of twice V_{TH}. Self cascode technique can be used to obtain cascoding of transistors without reducing the swing [12].

2. METHODOLOGY

The idea of self cascoding of transistor to adiabatic logic circuit used in sub-threshold region can reduce power consumption significantly [3].

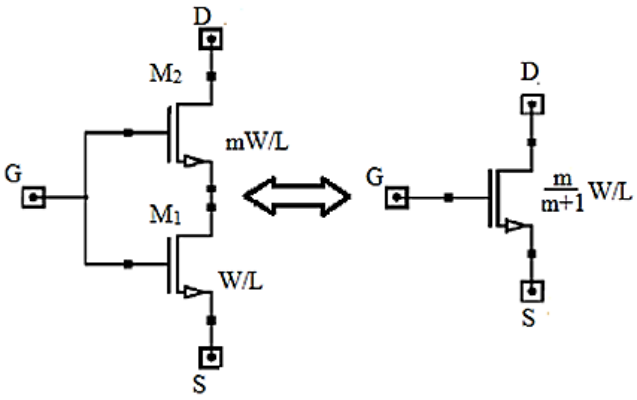

Fig. 2 Self Cascode Transistor

Fig. 2 shows that MOSFETs are in series, so currents in both transistors will be same. The two MOSFETs have same length but different widths thus the larger of the transistor will be in linear region and will have small drop across it, eventually in deep triode region, the transistor M_2 acts like a small source degeneration resistor for M_1. This makes the self-cascode arrangement suitable for low voltage applications. The effective β of new transistor is not changed much as new β is given by equation 1.

$$\beta_{eff} = \frac{\beta_1 \beta_2}{\beta_1 + \beta_2} \quad (1)$$

$$\text{if } \beta_2 = m.\beta_1 \quad (2)$$

$$\beta_{eff} = \frac{m}{m+1}\beta_1 \quad (3)$$

And if *m* is large, β is almost equal to β_1 where as the small signal output resistance of the new cascode transistor is given by equation 4. The equation suggests the resistance is increased by a factor of intrinsic gain of transistor M_2; this can be seen in $I_D V_D$ curves as shown in Fig. 3. The figure shows $I_D V_D$ curve for both self cascode transistor and a normal NMOS transistor. It can be seen that the slope of self cascode structure is smaller that indicates increase in output resistance.

$$r_0 = (gm_2 r_2).r_1 - r_1 - r_2 \quad (4)$$

$$r_0 \approx (gm_2 r_2).r_1 \quad (5)$$

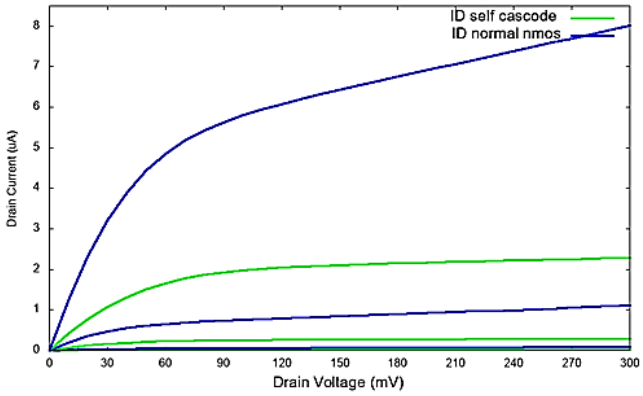

Fig. 3 $I_D V_D$ graph to demonstrate increase in output impedance of a self cascode transistor in subthreshold region. The curves are plotted for gate potential of 0.1, 0.2 and 0.3 volts

The overall gain of a self cascode inverter is given by equation 6.

$$A = gm_1.r_1 + gm_2.r_2 + gm_1.gm_2.r_2.r_1 \quad (6)$$

The small signal output resistance is multiplied by intrinsic gain of the wider transistor. Thus, the self cascode transistor is able to provide higher output resistance without sacrificing much performance. The increase in r_0 of transistor will improve the performance of the latch as mentioned earlier. The loop gain of a latch is product of gain of individual inverter of the latch as shown in Fig. 4.

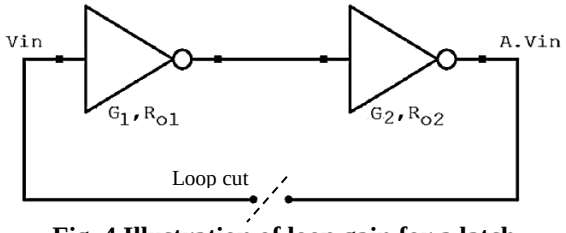

Fig. 4 Illustration of loop gain for a latch

The loop gain is given by equation 7

$$A = (G_1 R_{01}).(G_2 R_{02}) \quad (7)$$

Improvement in R_0 will improve the loop gain in square proportion.

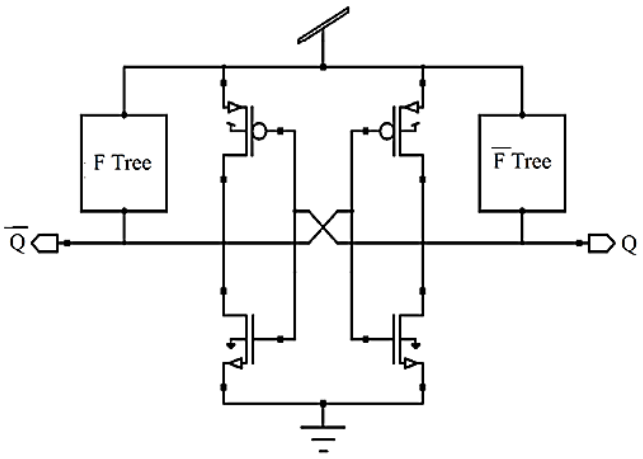

Fig. 5 PFAL circuit

Some standard adiabatic logic topologies like 2N2N2P, ECRL and PFAL [16] were simulated by replacing MOS transistors with self-cascode transistors in the latch. The PFAL topology was observed to provide better results. The PFAL adiabatic logic architecture contains a latch and two pull up network that realize a Boolean logic equation to be implemented as shown in Fig. 5.

3. PROPOSED LOGIC

A basic logic circuit as inverter using PFAL logic with fanout of four is designed and simulated using 70nm model file provided by Predictive Technologies Model (PTM) [14]. The circuit is as shown in Fig. 6.

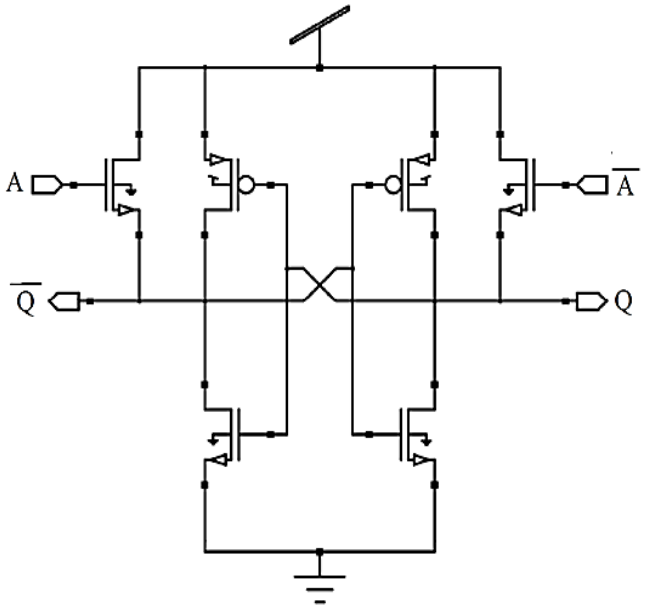

Fig. 6 PFAL inverter

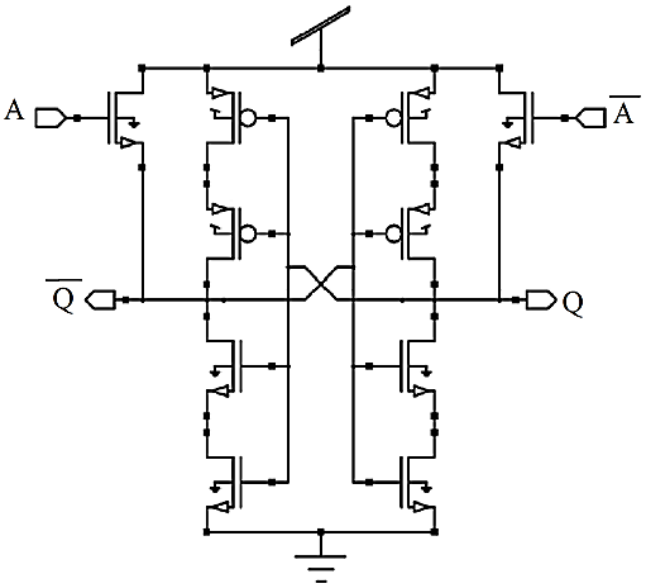

Fig. 7 Proposed Circuit

The latch transistors of the PFAL inverter circuit are replaced with self cascode transistors as shown in Fig. 7 to obtain SC-PFAL inverter as proposed circuit. To calculate the power consumption and propagation delay of the circuit, a test bench is developed with a triangular wave voltage source as supply voltage and a load of four unit load (inverter) is placed at output of design under test.

4. RESULTS AND DISCUSSION

The circuit is designed using 70nm PTM model file with threshold voltages V_{thP} = -326mV and V_{thN} = 310mV and simulated using T-Spice simulator. A 300mV triangular supply is used to power up the logic gate. To evaluate the performance of proposed architecture, basic logic gate is designed and simulated. The results are tabulated in table 1 and table 2. Simulated waveform of proposed inverter is shown in Fig. 8.

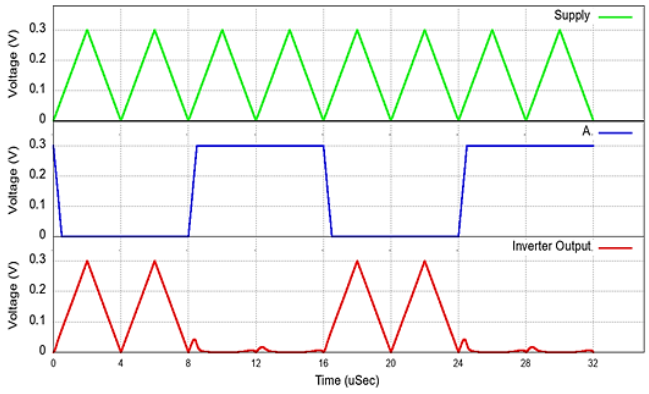

Fig. 8 Input output waveform of SC-PFAL inverter

It can be seen that the performance enhancement is better for SC-PFAL inverter than PFAL. The best enhancement in power reduction is observed to be obtained for inverter. Statistics shows that inverters are most used logic gates in a typical logic circuit.

Table 1. Basic inverter performance of PFAL for different clock frequencies

Frequency (MHz)	PFAL		
	Average Power Dissipation (W)	Propagation Delay (Sec)	PDP (J) (Dynamic)
0.5	2.77E-10	4.63E-07	1.28E-16
1	2.80E-10	2.32E-07	6.49E-17
1.5	2.83E-10	1.55E-07	4.40E-17
2	2.88E-10	1.17E-07	3.37E-17
2.5	2.93E-10	9.39E-08	2.75E-17
3	2.99E-10	7.85E-08	2.35E-17
3.5	3.06E-10	6.75E-08	2.06E-17
4	3.13E-10	5.95E-08	1.86E-17

Table 2. Basic inverter performance of SC-PFAL for different clock frequencies

Frequency (MHz)	SC-PFAL		
	Average Power Dissipation (W)	Propagation Delay (Sec)	PDP (J)
0.5	1.92E-10	4.64E-07	8.90E-17
1	2.01E-10	2.33E-07	4.70E-17
1.5	2.13E-10	1.57E-07	3.33E-17
2	2.26E-10	1.19E-07	2.68E-17
2.5	2.40E-10	9.57E-08	2.30E-17
3	2.56E-10	8.05E-08	2.06E-17
3.5	2.73E-10	6.95E-08	1.90E-17
4	2.91E-10	6.14E-08	1.79E-17

The power, delay and energy dissipation of SC-PFAL inverter is compared with PFAL inverter in plots a), b) and c) of Fig. 9 respectively. It is revealed that the SC-PFAL logic gives better results at lower frequencies. The SC-PFAL logic has shown better energy efficiency than PFAL adiabatic logic up to 4MHz. The plot of power dissipation versus operating frequency shows that power efficiency performance of proposed circuit is better at lower operating frequency.

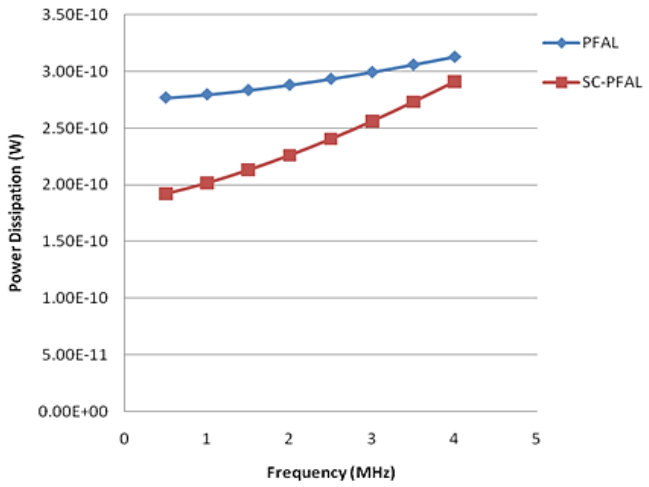

Fig. 9 (a) Comparison of power dissipation for inverter

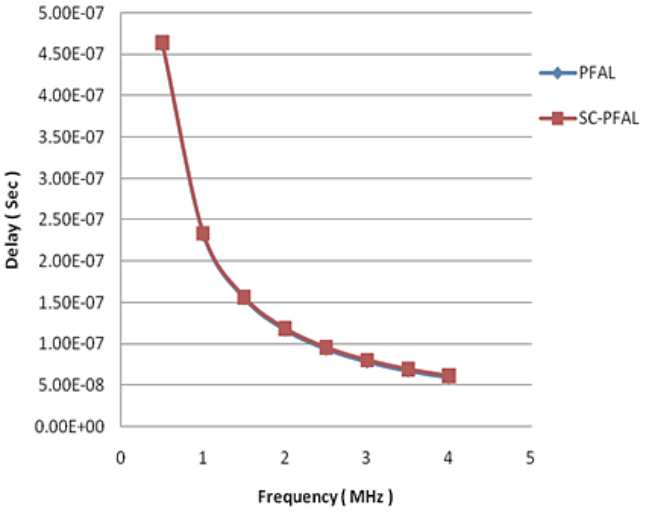

Fig. 9 (b) Comparison of propagation delay for inverter

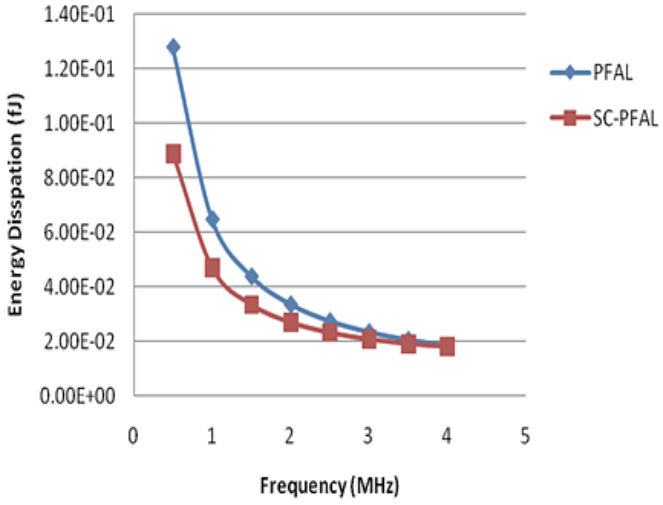

Fig. 9 (c) Comparison of energy dissipation for inverter

5. CONCLUSION

Proposed SC-PFAL circuit has better energy efficiency than PFAL circuit at lower operating frequencies in sub-threshold region. To reduce the power consumption, the concept of self cascoding is applied to the latch present in PFAL circuit. The effect of self cascoding was explored for PFAL and other adiabatic logic techniques also. It is revealed that PFAL logic is better suited for applying self cascode transistors. The simulation results show that power consumption of proposed SC-PFAL circuit is about 32% less than its original PFAL circuit at 0.5 MHz operating frequency. In summary, the SC-PFAL logic provides useful building blocks in design of energy recovery systems operating at very low power regime.

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Perovskite Halide Based Colorimetric Ammonia Sensor at Room Temperature

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Abstract:

Detection of the presence of ammonia at a low level is most desirable as the presence of the gas can occur in several areas like refrigeration, food processing and storage, fertilizers and ammonification by nitrogen cycle. An easy-to-use, low-cost, disposable colorimetric ammonia sensor based on perovskite halide was developed to detect presence of the toxic gas ammonia gas (NH3) on a cheap filter paper. This paper based sensor works at room temperature. The sensor was highly selective towards NH3 gas (as well as aqueous NH3) and is stable towards moisture. At low concentration of ammonia gas, the effect of color change of sensor was found to be reversible. The ability of the cost effective easy to make perovskite halide based colorimetric paper sensor to trace low level of NH3 at room temperature with high selectivity and high sensitivity without any added electronics, will have big impact in application and is of great practical relevance in areas of application where quick sensing is needed.

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Assessment of annual effective dose from equilibrium equivalent concentration of ^{222}Rn and ^{222}Rn in northern zone of Punjab (India)

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Abstract:

Radon (^{222}Rn) and Thoron (^{220}Rn) are major contributors to the ionizing radiation dose received by the mankind. High concentrations of ^{222}Rn and ^{220}Rn may elevate the risk of radiological exposure to general populace. In Indoor environment, most of the dose has been given by the ^{222}Rn and ^{220}Rn progeny. In the present manuscript, total equilibrium equivalent concentration of ^{222}Rn ($EERC_{A+U}$) and ^{220}Rn ($EETC_{A+U}$) has been calculated by using deposition based progeny sensors (DRPS/DTPS) in the dwellings of North region of Punjab (India). The separate attached and unattached EEC has also been discussed in the manuscript. The estimated ($EERC_{A+U}$) and ($EETC_{A+U}$) in the studied region fluctuate in the range from 11 Bq m^{-3} to 33 Bq m^{-3} and 0.8 Bq m^{-3} to 2.2 Bq m^{-3} respectively. The unattached fractions of EEC are directly responsible for the dose received by organs and target cells. An attempt has been made to estimate the unattached fraction and total radiological dose from ^{222}Rn and ^{220}Rn EEC. The total inhalation dose originated from $EERC_{A+U}$ and $EETC_{A+U}$ was lower than its recommended limit,

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Detecting Outer Edges in Retinal OCT Images of Diseased Eyes using Graph Cut Method with Weighted Edges

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Abstract:

Segmentation of biological and pathological layers in ophthalmic optical coherence tomography is very important for the examination and analysis of macular diseases. Identifying the deformation in any layer of retinal OCT could possibly track eye disease propagation. There are many methods available for manual segmentation of OCT scan images but manual segmentation has many challenges like chances of errors and inconsistency etc. Manual segmentation is a time taking process and diagnosis can vary from disease to disease. There are many researchers working with automated segmentation methods that overcome the limitation of manual segmentation of OCT retinal images but still overlapping of layers and noise present in OCT scan images makes it very challenging for separation of layers. The proposed work presents a method for segmenting ophthalmic layers in retinal Optical Coherence Tomography scanned images using pixel wise segmentation approach and real time classification of pixels in particular layer. With the help of prior knowledge of retinal structure, in this paper we experiment a promising method for segmentation of seven layers of retinal OCT scan image for multiple diseases. We validate our results with this method on 243 ophthalmic images.

Keywords:

Macular Edema; Drusen; Choroidal NeoVascularisation; Macular Degeneration; Optical Coherence Tomography (OCT); OCT layer segmentation