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HOLY MARY INSTITUTE OF TECHNOLOGY & SCIENCE

ICTASEMP-2021

15th - 16th July 2021 **Virtual Conference**

International Conference on

Technological Advancement in Science, Engineering, Management & Pharmaceutics

Organized By

Department of Electronics and Communication Engineering,
Holy Mary Institute of Technology & Science
in Association with
Institute For Engineering Research and Publication (IFERP)

International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Preface

The “International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics (ICTASEMP-2021) - Virtual Conference” is being organized by Department of Electronics and Communication Engineering, Holy Mary Institute of Technology & Science, Telengana in Association with IFERP-Institute For Engineering Research and Publications on the 15th-16th July, 2021.

Holy Mary Institute of Technology & Science (HITS) has a sprawling student –friendly campus with modern infrastructure and facilities which complements the sanctity and serenity of the major city of Telangana.

The “International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics” was a notable event which brings Academia, Researchers, Engineers, Industry experts and Students together.

The purpose of this conference is to discuss applications and development in area of “Technological Advancement in Science, Engineering, Management & Pharmaceutics” which were given International values by Institute for Engineering Research and Publication (IFERP).

The International Conference attracted over 150 submissions. Through rigorous peer reviews 83 high quality papers were recommended by the Committee. The Conference aptly focuses on the tools and techniques for the developments on current technology.

We are indebted to the efforts of all the reviewers who undoubtedly have raised the quality of the proceedings. We are earnestly thankful to all the authors who have contributed their research works to the conference. We thank our Management for their wholehearted support and encouragement. We thank our Principal for his continuous guidance. We are also thankful for the cooperative advice from our advisory Chairs and Co-Chairs. We thank all the members of our local organizing Committee, National and International Advisory Committees.

Acknowledgement

Er. R. B. Satpathy
Chief Executive Officer
Institute for Engineering Research and Publication (IFERP)

On behalf of Institute For Engineering Research and Publications (IFERP) and in association with Department of Electronics and Communication Engineering, Holy Mary Institute of Technology & Science (HITS), Telengana. I am delighted to welcome all the delegates and participants around the globe to Holy Mary Institute of Technology & Science for the "International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics (ICTASEMP -2021) - Virtual Conference" Which will take place from 15th-16th July, 2021.

It will be a great pleasure to join with Engineers, Research Scholars, academicians and students all around the globe. You are invited to be stimulated and enriched by the latest in engineering research and development while delving into presentations surrounding transformative advances provided by a variety of disciplines.

I congratulate the reviewing committee, coordinator (IFERP & HITS) and all the people involved for their efforts in organizing the event and successfully conducting the International Conference and wish all the delegates and participants.

Regards
Er. R. B. Satpathy

Message from Honorable Founder Chairman

Dr. Arimanda Vara Prasad Reddy

Founder Chairman, HMGI
Telangana, India

Message

I am pleased to welcome you to the International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics-2021 (ICTASEMP'21) to be held on 15th-16th July, 2021. Due to current pandemic situation, the conference will be organized in virtual mode only. This conference is from Holy Mary Institute of Technology & Science (Autonomous), Hyderabad in association with IFERP, Chennai.

The intent of this conference is not only to discuss lively and emerging issues of a particular domain but also dissemination of the awareness among other learned people. Over the years, dramatic improvements have been made in the field of Engineering, Pharmacy and Management Sciences. I hope ICTASEMP-2021 will become surely the most important International conference dedicated to bring out the Advancement in Science, Engineering, Management & Pharmaceutics.

In order to provide an outstanding technical level for the presentations at the conference, we have invited distinguished experts to participate in the Technical Programmes. We will have technical sessions, plenary sessions by keynote speakers during 2 days of conference including the awards presentation during the valedictory session on the last day of the conference.

I hope ICTASEMP-2021 will make you aware of state-of-the art systems and provide a platform to discuss various emerging technologies in Science, Engineering, Management & Pharmaceutics.

Message from Honorable Founder Secretary

Dr. Arimanda Vijaya Sarada Reddy

Founder Secretary, HMGI
Telangana, India

Message

It is a great pleasure and an honor to extend to you a warm invitation to attend the the International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics-2021 (ICTASEMP'21) to be held on 15th-16th July, 2021. at Holy Mary Institute of Technology & Science (Autonomous), Hyderabad in association with Institute For Engineering Research and Publication (IFERP), Chennai.

The ICTASEMP'21 Conference will provide a wonderful forum for you to refresh your knowledge base and explore the Advancement in Science, Engineering, Management & Pharmaceutics. The Conference will strive to offer plenty of networking opportunities, providing you with the opportunity to meet and interact with the scientists and researchers.

I feel this ICTASEMP'21 conference is important to reiterate the need to translate Engineering & Technology into knowledge to help overcome societal challenges.

I am looking forward to meet you during the virtual conference ICTASEMP-2021 and to share a most pleasant, interesting and fruitful conference.

Message from Chairman

Sri. Arimanda Siddhartha Reddy

Chairman, HMGI
Telangana, India

Message

The International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics - 2021 (ICTASEMP'21) to be held on 15th-16thJuly, 2021 at Holy Mary Institute of Technology & Science (Autonomous), aims to respond to the needs and aspirations of a rising global environmental issues with a theme of Advancement in Science, Engineering, Management & Pharmaceutics. ICTASEMP'21 provides an opportunity for the meeting of International Researchers, Engineers, Scientists, and specialists in the various research and development fields of Engineering and Technology.

This conference offers a premise for global experts to gather and interact intensively on the topics of Electronics and Communication, Computer Science and Information Technology along with all other Engineering streams and Pharmacy. I am privileged to say that this conference will definitely offer suitable solutions to the global issues.

I would like to express my appreciation to the organizing committee for their dedicated efforts to materialize the conference. I hope all the participants will have a fruitful and beneficial experience. Eventually I express my special thanks and appreciation to all.

Message from Director

Dr. P. Bhaskara Reddy

Director, HMGI
Telangana, India

Message

It is my great delight to welcome you to the International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics - 2021 (ICTASEMP'21) to be held on 15th-16thJuly, 2021 at Holy Mary Institute of Technology & Science (Autonomous), Hyderabad in association with Institute For Engineering Research and Publication (IFERP), Chennai.The idea to host the ICTASEMP'21 in HITS, Hyderabad is to bring together Researchers, Scientists, Engineers, Scholars and Students in the areas of Information Technology, Computer Science, Electronics and Communication Engineering and all other Engineering streams and Pharmacy including Management Sciences

The ICTASEMP'21 Conference will foster discussions and hopes to inspire participants from a wide array of themes to initiate Research and Development and collaborations within and across disciplines for the advancement of Technology.

The various thematic sessions will showcase important technological advances and highlight their significance and challenges in a world of fast changes. I welcome all of you to attend the plenary sessions and oral presentations and invite you to interact with the conference participants.

Message from Convener

Mr. Y. David Solomon Raju

Convener, ICTASEMP'21, HMGI
Telangana, India

Message

It is a great pleasure and an honor to extend to you a warm invitation to attend the International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics-2021 (ICTASEMP'21) to be held on 15th- 16th July, 2021 at Holy Mary Institute of Technology & Science (Autonomous), Hyderabad in association with Institute For Engineering Research and Publication (IFERP), Chennai

The theme of the conference is Advancement in Science, Engineering, Management & Pharmaceutics will underpin the need for participation in forums for collaborative Research and cooperation of individuals from a wide range of professional backgrounds.

The Advancement in Science, Engineering, Management & Pharmaceutics in the Conference will provide a wonderful forum for you to refresh your knowledge base and explore the innovations in Engineering and Technology. The Conference will strive to offer plenty of networking opportunities, providing you with the opportunity to meet and interact with the scientists and researchers, friends as well as sponsors and exhibitors.

I hope you will join us for a symphony of outstanding Conference, I am looking forward to meet you during the virtual conference ICTASEMP'21 and to share a most pleasant, interesting and fruitful conference.

Keynote Speaker

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Professor of Microelectronics, BITS-Pilani Goa
Ex-Director of North Eastern Regional Institute of Science & Technology (NERIST) – a Central University)

Prof. Shailendra N Kulkarni

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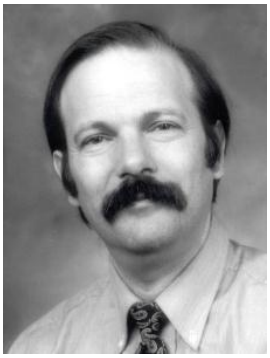

Prof. Moshe Vardi

Professor at Rice University
Bellaire, Texas, United States

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PAPERS

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15th-16th July, 2021 – Virtual Conference

Synthesis and Low Temperature Ferroelectric Studies of Polycrystalline $TbMnO_3$ Multiferroics

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Abstract—Multiferroics are the materials that simultaneously possess two or more primary ferroic (electric/magnetic/elastic/toroidic) properties. The possible applications of multiferroics are ac/dc sensors, microwave resonator-phase shifters, multi-state memories, solar cells, and thermal energy harvesting, and magnetocaloric materials. Among various types of single-phase multiferroics, Giant spin-driven ferroelectric polarization has been reported in single-crystal $TbMnO_3$ multiferroics under high pressure. A polycrystalline $TbMnO_3$ was synthesized through the sol-gel method and structural studies revealed the single-phase nature of the sample. Rietveld analysis has been used to analyze the structural results and to calculate the lattice parameters. Ferroelectric studies have been studied from the 4-50K temperature range and the results revealed that the specific results are well matching with ferroelectric transitions. These studies revealed the coupling between the ferromagnetic and ferroelectric orders.

Index Terms— Multiferroics, single-phase; Heat Capacity; Dielectric Constant

I. INTRODUCTION

Multiferroics term was first brought into usage by H. Schmid to describe materials that show more than one primary ferroic properties like ferromagnetism, ferroelectricity, magnetoelectricity in a single-phase[1]. The origin of magnetism is due to the presence of localized electrons in the partially filled d or f sub-shells in rare-earth ions. Nowadays this definition is expanded to fit antiferromagnetism and ferrimagnetism. Multiferroics materials are solid-state compounds, which exhibit two ordered states are magnetic and electric. These materials are very much interested in Research & Technological application due to their coupling between Ferro phases and the piezoelectric properties facilitate a direct control of Ferromagnetic and ferroelectric properties[2].

This Mechanism was used in such as actuators, switches, magnetic field sensors, and also electronic memory devices[3,4]. Typical multiferroic materials are transition metal oxides and also include rare earth manganite and ($RMnO_3$) such as $TbMnO_3$, $DyMnO_3$, and some bismuth-based compounds like $BaNiF_4$, $BiMnO_3$. Here $TbMnO_3$ is a single-phase perovskite-type manganite with a polycrystalline orthorhombic structure. Although there are many studies on magnetic, Heat capacity, magnetocaloric properties of $TbMnO_3$ from room temperature to low temperature, a very few have concentrated on low-temperature ferroelectrics properties of polycrystalline $TbMnO_3$. In this paper, the preparation of one such compound $TbMnO_3$ synthesized through the sol-gel method, and its ferroelectric behavior in low temperature has been studied and the results are discussed in the paper.

II. EXPERIMENTAL METHODS

2.1 Synthesis &Characterization

The polycrystalline $TbMnO_3$ sample has been prepared through the Sol-Gel method. The starting materials Tb_2O_3(Sigma Aldrich, 99.99%), freshly prepared $MnCO_3$ precursors were taken in stoichiometric ratio. The materials are dissolved in Nitric acid separately and then mixed in a glass beaker on a magnetic stirrer until it gets to a homogenous solution. Then citric acid has been added to the solution and mixed for 30 mins in the ratio of 1: 1. Further, PH has been adjusted to 7 with the help of Ammonia solution. Later this solution was heated on a magnetic stirrer with a hot plate until it was reduced to (1/3)rd of its original solution at 80 °C until the viscosity of the solution increases up to a point where the solution is no longer in a liquid state but is in a semi-solid gel state. After that Ethylene glycol ($CH_2(OH).CH_2(OH)$) was added to the final solution in the ratio of 1: 1.2, and continue to heat the solution until the water content evaporates completely at around 120-150°C. The gel form in the glass beaker was further heated until we get a black-colored powder. For experimental purposes, the black-colored powder was transported into a mortar and grind to get a fine powder. After obtaining fine powder from it was calcinated at 1000 °C for four hours to remove any residual organic impurities. Later the black-colored ash will be pressed into pellets with a diameter of 10 mm and thickness of 1.5 mm, with the help of a hydraulic press by applying pressure of 2 to 3 tons per square inch. Finally, the pellets were sintered at the temperature of 1300 °C for 5hrs.

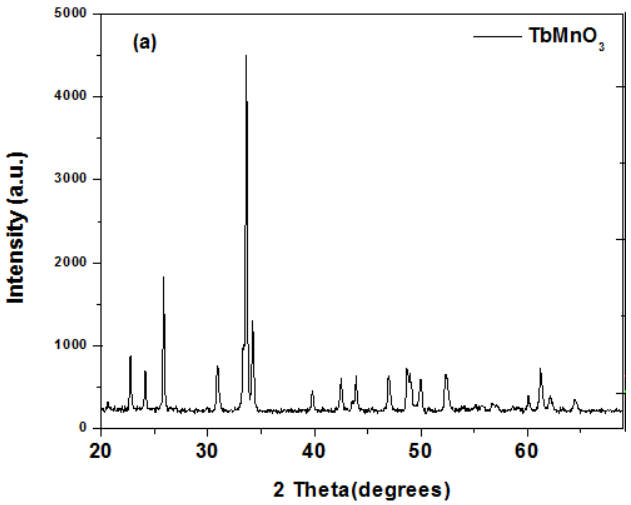
Table 1: XRD Analysis

S.No	XRD results	
1	a(A)	5.8
2	b(A)	7.4
3	c(A)	5.3
4	V(A)	227.5
5	R_p	8.25
6	R_{WP}	11.05
7	R_{EXP}	8.33
8	S (goodness of fit)	1.32

III. RESULTS AND ANALYSIS

The structural characterization of samples was carried out by the XRD(X-ray diffractometry), the diffraction patterns are mentioned in Figure 1. The XRD data were analyzed using the Rietveld refinement technique by assuming orthorhombic structure with ***the Pnma*** space group. The data of XRD of all the samples are shown in Fig 1(a). It is clear that samples are of a single phase with no detectable impurity and the sharp peaks seen in the XRD pattern; indicate that the studied sample to be purely crystalline.

The observed and calculated Rietveld refinement patterns of $TbMnO_3$ lattice parameter values are in the given Table (1). The lattice parameters a, b and c values as 5.8A°, 7.4 A°, 5.3 A° respectively, and the results have matched with the theoretical and experimental values, and also best of fit(GOF) was matched with the data in the literature. The values of residual factor R_p, R_{wp} are satisfactory range as per literature.



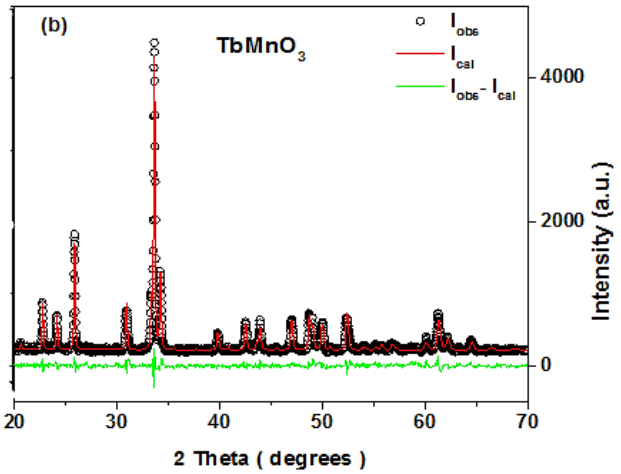


Figure 1: (a) XRD of $TbMnO_3$ sample. (b) Rietveld refinement pattern of $TbMnO_3$ samples.

3.1 Heat Capacity Studies

The heat capacity of a substance of 1 gm is defined as the amount of heat required to raise its temperature by 1° C . Heat capacity can be measured at either volume constant (C_v) or pressure(C_p). Heat capacity is important because this will give the information about the sample to how long the heating or cooling process will take at under a given heat supply.

By using semi adiabatic pulse method, the Heat capacity measurements were carried out. The given figure shows the graphical variation between the (C_P/T) with the temperature (T), to all the samples are at zero and with having magnetic fields. From the figure, the given sample exhibits approximately a sharp peak at 40 K and is attributed to the sinusoidal arrangement of Mn^{3+} ions. The other transition at about 26K is called lock-in-transition and is due to the change in the sinusoidal ordering of Mn^{3+} ions into spiral ordering which induces the breaking in the center of symmetry leads to the polarization. On further decreasing the temperature, another anomaly has been observed at below 10 K and it indicates the ordering of Tb^{3+} ion spins[5].

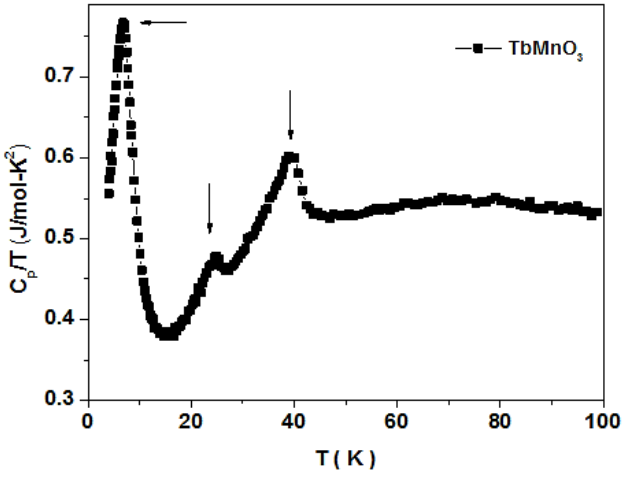


Figure 2: Variation of Cp/T with temperature

3.2 Low Temperature Dielectric Constant Studies

Figure-3 shows the dependence of the dielectric constant as a function of temperature at 1 kHz, 10 kHz, and 100 kHz frequencies. It has been observed that there is a slight change in dielectric constant values with the frequency. As the temperature decreases from 50K, dielectric constant values are found to increase and an anomaly has been observed at 30 K. It is matching with the anomaly in heat capacity studies. This is a paraelectric to ferroelectric transition at 30K[5]. It is known that ferroelectricity arises when there is a break in the center of symmetry. At this temperature, a change from the sinusoidal ordering of Mn^{3+} ions changes to spiral ordering which breaks the symmetry. The break-in center of symmetry leads to the polarization and dielectric constant.

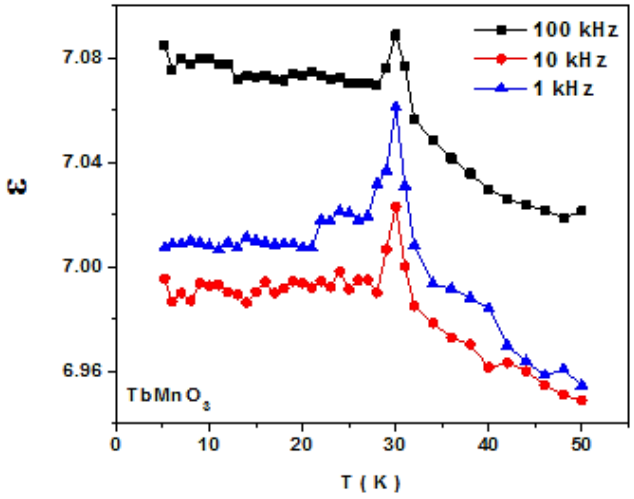


Figure 3: Variation of frequency with Temperature for different compounds.

IV. CONCLUSIONS

Polycrystalline $TbMnO_3$ has been prepared through the sol-gel method. Structural analysis has been carried out by using X-ray diffraction and observed that the samples crystallized in orthorhombic structure without any secondary phases. Heat capacity measurements revealed the multiple transitions in the material at 40K, 26K and below 10K are attributed to the ordering of Mn^{3+} and Tb^{3+} ions. Low-temperature dielectric constant studies revealed a transition at 30K which is ferroelectric transition. It is well matching with the heat capacity results.

V. ACKNOWLEDGEMENTS

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Autophagy: Readouts for Tracking the Progress of the Pathway

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Abstract—Autophagy is a highly regulated cellular pathway aiming to maintain and establish homeostatic state of cells. Autophagy is a form of programmed cell death pathway that keep an eye on non-functional proteins/organelles, intracellular pathogens, endoplasmic reticulum and oxidative stress some external stimuli like hypoxia, nutrient deprivation, specific drug molecules etc. This process starts by formation of a double membrane structure called autophagosome which ultimately delivers the target cargo to lysosomes for degradation. Autophagy has a debatable role in cancer progression as in some studies it is seen that it supports cancer progression while in others it shows cancer regression. This pathway is very crucial in regulating overall physiological state of cells Therefore it becomes very important to keep surveillance on this pathway. Tracing this pathway can lead to prediction of large spectrum of pathological conditions and also the efficacy of therapeutics. This review focuses on some indirect and direct methods that are applicable in lab setup to track this critical cellular pathway.

Index Terms— Autophagy, Cancer, Endoplasmic reticulum, Hypoxia, Lysosomes

I. INTRODUCTION

Autophagy is a conserved self degradative pathway which was first discovered and explored in yeast by Yoshinori Ohsumi in 2016. He was honoured with Noble Prize in the field of Medicine or Physiology but the term "Autophagy" was given by Christian de Duve way back earlier [1]. In the last two decades prodigious work has been done in the field of exploring autophagic pathway, identifying autophagy related genes (ATGs) and understanding all the protein complexes involved in the pathway. Typically three forms of autophagy are seen in the cell namely, macroautophagy, mitophagy (mitochondrial autophagy) and chaperone mediated autophagy (targets KFERQ motif in target protein). Apart from this xenophagy (autophagy mediated pathogen killing), aggrephagy (autophagy mediated lysis of aggregated proteins) are also seen. Interestingly autophagy also plays key role in some pathological conditions like neurodegenerative disorders [2], cardiovascular diseases [3] and autoimmune disorders [4]. This pathway grossly involves formation of double walled "autophagosome" which engulfs the target cargo and followed by fusion of outer membrane of autophagosome with that of lysosome resulting into a structure called "Autophagolysosome" therefore, causing its degradation via the lytic enzymes in lysosomes. Autophagic pathway is divided into 4 sub stages:

INITIATION:

In the first stage of starvation mediated autophagy mechanistic target of rapamycin complex 1 **(**Mtorc1) dissociates from unc-51-like autophagy-activating kinase 1 (ULK1/2) complex and ATG13 protein leading to their activation. ULK1/2, ATG13, ATG101 and FIP200 form the initiation complex for phagophore formation [5].

NUCLEATION:

The next step is nucleation of the initiation complex in which class III phosphatidylinositol 3-kinase (PtdIns3K) plays a central role. The key protein complexes in the step are VPS34, UV irradiation resistance-associated gene (UVRAG), BECLIN1. Together these complexes facilitate the nucleation step [5]. Some anti-apoptotic proteins like BCL-xL, BCL-2 and other proteins like Rubicon interacts with BECLIN1and suppress its expression [6] ultimately affecting immature autophagosome formation.

ELONGATION:

Atg12–Atg5-Atg16 protein complex is requisite for elongation of immature autophagosome in both yeast and mammals. Ubiquitin systems like microtubule-associated light-chain B (LC3B) in conjugation with lipidated phosphatidylethanolamine (PE) helps in membrane tethering and closing phagophore to form mature autophagosome. Combination of lipidated LC3B and Atg12–Atg5-Atg16 complex marks elongation and closing of autophagosome [5].

FUSION AND FEED DEGRADATION:

In the last step the autophagosome fuses with outer membrane of lysosomes resulting into autolysosome with the help of Rab GTPase and SNARE proteins [5].

METHODS FOR AUTOPHAGY READOUTS:

Autophagy is a zestful pathway and is more of an adaptive response to various types of stresses. As already discussed this process plays key role in various cellular processes including ageing, control of cell density, cellular homeostasis, maintenance of stemness in cancer cells etc. Therefore it becomes extremely important and needful to keep a track and monitor this process as failure at any step could lead to various pathologies (cancer, neurodegenerative disorders, and cardiovascular diseases).

Two ways of autophagic flux detection has been briefly discussed here:

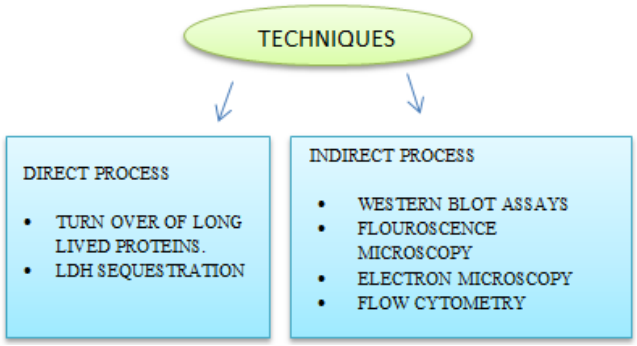

FIGURE 1- OUTLINE DEPICTING DIFFERENT WAYS OF ANALYSING AUTOPHAGIC FLUX.

INDIRECT METHODS:

A. WESTERN BLOT ASSAYS: One of the widely used indirect method of estimating autophagic flux, in this different autophagic substrates can be targeted and be analysed on a western blot or SDS PAGE. One approach is to use microtubule-associated protein 1 light chain 3 (MAP1-LC3) protein family, these are grouped as GABARAP and LC3 subfamilies. LC3 protein family has role to play in phagophore formation and closure as explained earlier in the text. LC3 proteins are found on outer and internal surface of autophagophore membrane. LC3 protein present on inner side of membrane gets delivered to lysosomes along with the cargo. Lipidated form of LC3 or LC3-II (Molecular weight14-16 KDa) and non lipidated LC3 or LC3-I (Molecular weight 16-18 KDa) this causes separation of protein via western blotting. Lysosomal inhibitor (like chloroquine, Bafilomycin) presence or absence in analysis of LC3-I/ LC3-II gives a hazy picture as increased LC3-II concentration may indicate dysfunctional autophagosome and lysosome fusion or dysfunctional induction of autophagy while decreased LC3-II concentration may indicate autophagy inhibition or increased autophagic flux. To check inhibition or stimulation of autophagy we can analyse LC3-II amount in existence and inexistence of lysosome blockers in same sample [7].

Second approach is estimation of SQSTM1/p62- is important autophagic substrate that helps in anchoring autophagic cargo proteins inside autophagosome by hooking onto their ubiquitin binding domain, moreover they convey the cargo to LC3-II via LC3 interacting region (LIR). Just like LC3-II estimation via western blotting SQSTM1/p62 can also be estimated in presence and absence of lysosomal blockers, increased levels of the complex indicate dysfunctional autophagic flux and decreased levels of this shows high levels of autophagic flux. A problem with this approach is some tissues and cells tend to have steady levels of SQSTM1/p62 even in presence of autophagy, because its expression is transcriptionally regulated and hence balanced by de novo synthesis. This makes abnormal western blot results but some studies afterwards showed that cycloheximide is a compound that blocks de novo pathway and further analysis can be done by radiolabelling pulse chase experiments and immuno-precipitation (of SQSTM1/p62) [7], [8].

B. FLOUROSCENCE MICROSCOPY: This indirect method allows qualitative and quantitative estimation of autophagy marker, substrates or proteins by immunofluorescence or live cell imaging [7]. Generally endogenous autophagy proteins or ectopically expressed proteins are utilised. These proteins can even be prepared by transfection ,stably transfected cell lines gives homogenous protein expression and low signal variability, therefore it is preferred in live cell microscopy and imaging [9]. FM (FLOUROSCENCE MICROSCOPY) Method can be performed by three approaches (i) Dyes- Some amphiphilic tracer dye, like Cyto-ID® can be used for tracking autophagic process by visualising microscopically in live cells and for cells difficult for transfection. Advantage being efficient, accurate and reliable and can be performed in difficult experimental setting, disadvantage being partial specificity [10].

C. ELECTRON MICROSCOPY: Electron microscopy directly allows autophagosomes, autophagolysosome, to be detected through eye, although it is easier said than done because it is very difficult to distinguish these ultra-cellular structures through naked eye morphologically. Adding to this tracking through h EM becomes difficult as there are some factors which govern its success like – well preserved cell morphology, cell type, use of lysosomal inhibitors, procedure for sample preparation, observational skills, cell volume [7]. An increase in autophagosome, autophagolysosome, amphisome indicate towards increased autophagic flux. Different variants of EM can be used as autophagy readouts like cryo-soft X-ray microscopy, transmission and immuno-Electron microscopy, electron tomography [11].

An increase in autophagosomal vesicle reflects increase in induction of autophagy but is not true in every sense sometimes it may indicate blockage of overall autophagic flux [12] or it may indicate dysfunctional autophagic process. Therefore direct methods seem to be more reliable.

D. FLOW CYTOMETRY: Method of imaging flow cytometry (combination of fluorescent microscopy and flow cytometry, unique in collecting their real and fluorescent images) and flow cytometry is helpful in cells that have poor adherence or are in suspensions. The advantage with using imaging flow cytometry is that signal location can be detected within the cell. GFP tagged LC3 (Microtubule-associated protein 1A/1B-light chain 3) could be used to monitor LC3 protein's movement into lysosomes where its degradation will cause decreased luminescence and will guide towards autophagic flux. Apart from this autophagic substrates

like p62,SQSTM1,NBR1 can also be tagged with green fluorescent protein and tracked for fluorescent quenching [13],[14]. One weak point of this is type of cell used, as it not very helpful in adherent cells but very effective for high content screens and monitoring of autophagy using fluorescent images [15].

DIRECT METHODS:

E. **TURN OVER OF LONG LIVED PROTEINS**: Long lived proteins are proteins that have high half life values and have an impact on age and other age related parameters. This method involves radiolabelling of elements like Carbon, Hydrogen, Sulphur in amino acids like leucine, leucine (radiolabel hydrogen), and methionine respectively. The radioactivity due to these labelled amino acids is measured by liquid scintillation counting during their degradation in autophagolysosome. [16]. This method is carried out in pulse-chase manner where radiolabelled compounds are added in the pulse phase and during the chase phase respective natural compound is added along with an autophagic inhibitor (Eg. 3 methyl adenine) [17]. MG132 (carbobenzoxy-Leu-Leu-leucinal) can be used to prevent proteasome degradation of these proteins.

Autophagy degraded lived proteins can also be estimated via non radio active compounds like L-azidohomoalanine (AHA), mode of action includes azide functional group of azidohomoalanine links with the alkyne functional group of dye used in a pulse chase experiment [18].The fluorescent signal intensity can be determined using techniques like flow cytometry or immuno fluorescent microscopy. This method takes an edge as there is no requirement of handling radioactive materials.

a) **LDH SEQUESTRATION**: It has been lately observed that autophagic sequestration assays could be explored as direct method to monitor flow of autophagic pathway, especially in bulk autophagy where non selective capture or sequestration of some cytosolic markers (not autophagic marker) into autophagic vesicles can be estimated directly [19]. A cytosolic marker should be soluble, abundant in quantity, should not interfere in autophagic process. One such marker is LDH (Lactate dehydrogenase) with advantages like a) ample amount that can be quantified by enzymatic assay b) non selective degradation in autosome-lysosome vesicles c) ubiquitously expressed in all cells [20]. Quantitative analysis by centrifugation of cytosolic LDH and sequestered LDH hints towards proceeding of autophagic flux and is more accurate than other methods. It is crucial to use lysosome blockers (Eg- leupeptine, rapamycin) to prevent sequestered LDH decay in lysosomes [21]. LDH amounts then can be estimated by enzymatic measurement assays (NADH) or by western bots [22]. This experiment has been validated in rat hepatocytes [23] and mammalian cell cultures. But it requires electro disruption (electroporation) in order to release cytosolic LDH and sequestered LDH can be collected through centrifugation [20].

ABBREVIATIONS USED:

ATG- Autophagy related genes

MTORC1- Mechanistic target of rapamycin complex 1

ULK1/2- unc-51-like autophagy-activating kinase 1

FIP200- focal adhesion kinase family interacting protein of 200 kD

PTDINS3K- Class III phosphatidylinositol 3-kinase

VPS34- Vacuolar protein sorting 34

UVRAG- UV irradiation resistance-associated gene

BCL-xL- B-cell lymphoma-extra large

PE- Phosphatidylethanolamine

LC3B- Microtubule-associated light-chain B

SNARE -Soluble N-ethylmaleimide-sensitive factor activating protein receptor

SQSTM1- Sequestosome-1 gene

AHA- L-azidohomoalanine

LDH- Lactate dehydrogenase

NADH- Nicotinamide adenine dinucleotide hydride

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Portable, Low Cost Ventilator

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Abstract—This paper is written to focus on the development of a non-invasive, user-adjustable mechanical ventilation for patients suffering from respiratory problems. The patients are fed with controlled breaths given by a feedback loop system i.e. a pressure transducer and a flow rate transducer. All the user input, are fed by the doctor, and are displayed on the monitor. The sensors will feedback the signals to the microcontroller, which will perform operations like converting the signal into pulse width modulation signal to check any error and synchronize the breathing cycle. The wide range of settings enable us to digitally control the ventilator according to the patient's needs. DC high pressure blower air pump, with electronic speed controller, is PID tuned and is replaceable with similar pumps after tuning. The ventilator uses replaceable sensors for dynamic modification of transfer functions. The result is the design and making of a portable low cost ventilator that can be used in ambulances, small hospitals and during disaster management to provide volume and pressure-controlled air for mechanical ventilation

I. INTRODUCTION

Ventilators irreplaceable lifesaving equipment, it is a closed loop system that aids in artificial breathing by regulating the quality and quantity of air being delivered to the human body at any given time. Mechanical Ventilators are required in seven major departments like medicine, pediatrics, pediatric surgery, surgery, orthopedics, chest medicine and TB, ENT and gynecology. A major impediment to their availability in small hospitals and clinics, especially of 3rd world countries, is their cost and the need for specially trained staff to operate and maintain such complex devices.

A. Negative Pressure Ventilation

In Negative-pressure ventilation (NPV) the air pressure supplied to the thorax during inspiration is subatmospheric pressure which causes thoracic expansion and a decrease in pleural and alveolar pressures, which results in pressure gradient causing the air to move into the alveoli from the airway opening. As soon as the pressure surrounding the thorax increases and becomes atmospheric or greater, elastic recoil of the respiratory system causes expiration to occur passively. The change in inspiratory

pleural and alveolar pressures, which changes the NPV, in, replicate those during spontaneous breathing. On the contrary, positive-pressure ventilation (PPV) causes an increase in intrathoracic pressures during inspiration. Due to upper airway obstruction and hypoxemia during sleep, Negative-Pressure Ventilation is used in only a few situations. As it does not require a tracheostomy it is a suitable and attractive option for patients with neuromuscular disorders, those with residual muscular function.

B. Positive Pressure Ventilation

In Positive-pressure ventilation, the airway pressure applied at the patient's airway through an endotracheal or tracheostomy tube is larger than the pressure at the airway of the lungs, which allows the air to flow into the lungs until the breath is terminated. As soon as the breath is terminated the airway pressure drops to zero and elastic recoil of the lungs pushes out the air within it making a passive exhalation.

Positive pressure ventilation can be delivered in two forms: Invasive Positive Pressure Ventilation (IPPV) which involves the delivery of positive pressure to the lungs through an endotracheal tube or tracheostomy and Non-Invasive Positive Pressure Ventilation (NIPPV), which is delivered through a special face mask with a tight seal (air travels through anatomical airways). A breath during positive pressure ventilation can be characterized by changes in pressure, volume, and flow during inspiration and expiration. Mathematical expression which expresses these principles is :

$$Paw = P1 + (Ee + Vt) + (flow + R)$$

Where P1=initial alveolar pressure, Paw = airway pressure, Vt = tidal volume, R = resistance to flow, Ee = inherent elastance of the pulmonary system.

II. DESIGN METHODOLOGY

Arduino Nano V3.0 microcontroller is the brain of this system, it interprets, sends, controls data which has been given via front panel settings knobs and all the parameters that are given to the system are displayed on LCD which acts like a user interface. Microcontroller processes this data and caliberates it with the real time values that are fed to it by two analog pressure transducers, placed after the custom made BLDC blower. This forms a closed loop system where data is simultaneously interpreted and controlled.

A. Input Methods And Parameters

High end Invasive Ventilators work on different parameters like: Respiratory Rate, Inhale to Exhale Ratio (I:E Ratio), Tidal Volume (Tv), Oxygen Concentration (O2), Flow Rate Sensitivity, Trigger, PEEP, but, since, non invasive ventilators are not made for emergency use rather just to support the breathing of stable patient, these all parameters

are not that needed and uses I:E Ratio, Respiratory Rate, Trigger and Sensitivity, modes- BiPAP and CPAP.

This ventilator uses above parameters, which are fed by the doctor using graphical user interface and knobs placed on the front panel as shown in Figure II.1. These parameters are then fetched to Arduino Nano which will process it using an algorithm.

B. *User Interface*

Once the doctor gives required parameters through the input methods to the ventilator, the microcontroller will make it user readable and fetch it to an LCD Display and the doctor can see the settings of the machine. This user interface makes it easy for the doctor to check whether the input parameters are the same which he had given with the help of input methods and it is reliable for anyone to monitor the patient. The user interface is shown in Fig. II.1

C*. Loop And Feedback*

The parameters given by the doctor are then processed by Arduino Nano with the help of an algorithm, which converts user readable data to machine readable data and controls the motor driver which changes the speed of the pressure blower to obtain the required set of outputs that matches the inputs given by the doctor. The pressure transducer converts physical air pressure, which falls on to it, to analog signals that are in proportion to the applied pressure and sends it to the microcontroller.

Before ground isolation is done, analog signals by the sensor to the microcontroller are converted to variable duty cycle Pulse Width Modulation signals through inbuilt programming. This is achieved by generating a saw-tooth signal of required frequency. Analog output from sensors act as reference signals which when fed to a comparator along with saw-tooth signal generates PWM signals. These signals vary in duty corresponding to varying analog voltage levels. After performing operations it will adjust the signals that it sends the motor driver to control the blower for the desired output.

D. *Pressure controlled Breathing Cycle*

The ventilator has two modes- BiPAP and CPAP, and it will perform accordingly as the mode set by the doctor. In BiPAP (Bi-Level Positive Airway Pressure) a high level of pressure is maintained during the inspiratory cycle and a low level during expiratory cycle, such that it matches the patient's needs. In CPAP, a constant pressure is maintained at any point of time, such that the lungs are kept open throughout the breathing cycle. The pressure never drops below PEEP (Positive End Expiratory Pressure), as set by the doctor ,such that no vacuum builds in lungs set by the doctor.

The mandatory breaths are pressure controlled breaths which cycles at preset breathing rate known as Breaths Per Minute, and it is adjustable according to the patients need.

E. *Pressure Control*

Speed controller for BLDC air pump is an Electronic Speed Controller which is controlled by Arduino Nano V3.0. This ESC has 2 MOSFETS which regulates the power to BLDC motor upon receiving signals from microcontroller.

This ESC LC low pass filter is used to remove ripple and unwanted noise. Typical inductor choice for this purpose is a ferrite drum and iron powder inductor. During ON state of the MOSFET, the inductor stores energy and releases it to the load. During OFF state, energy is freewheeled through the 2nd MOSFET.

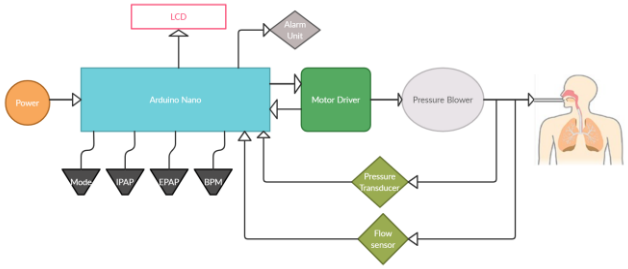

Fig. II.1

III. EXPERIMENTS AND RESULTS

A. *Blower Performance*

The blower is operated at 12V, 15V and 24V and we get the respective performance characterized by the flow(l/min) vs pressure graph(cmH2O). At 12V the output pressure of the blower is 17cmH2O,

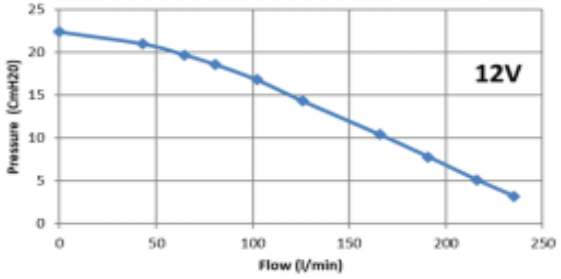

Fig. III.A.1

at 15V for zero flow it is 30cmH2O but at the flow rate of 100 l/min the pressure drops just to 25cmH2O.

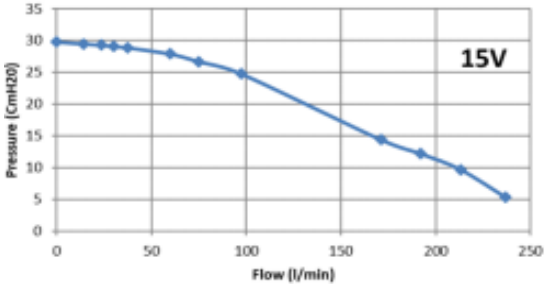

Fig. III.A.2

At 24V the output pressure is 66cmH2O.

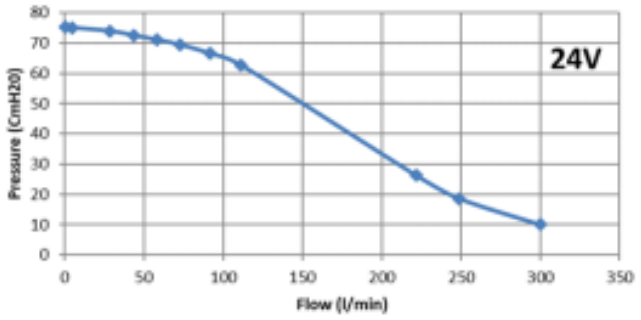

Fig. III.A.3

In Conclusion we can say that operation at 24V will give us desired output pressure required

***B**. Results*

To test, whether the ventilator performs mandatory inspirations or not, normal breathing rate of 12 bpm was set from the front panel and patient was asked to breathe with his glottis closed and start an end inspiratory cycle, the ventilator performed it's mandatory cycle from seconds 12 to 30, with probable fluctuations due to intended leak during the cycle.

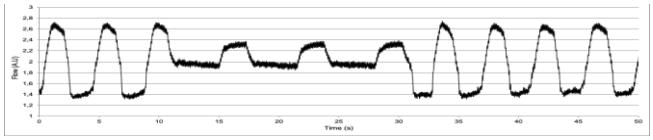

Fig.III.B.1 Flow rate readings

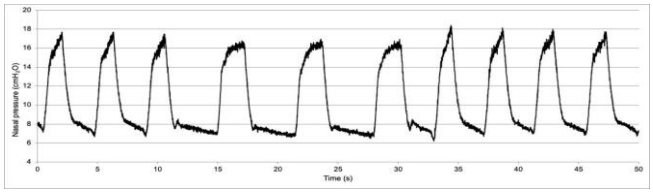

Fig. III.B.2 Pressure sensor readings

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MapReduce Parameter Optimization of Hadoop using Genetic Algorithm

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Abstract—In this era of massive knowledge, Hadoop, jointly of the foremost unremarkably used massive processing platforms, features a variety of parameters that are closely associated with resource utilization, particularly mainframe and memory. Calibration of these parameters through improvement may increase Hadoop's resource utilization. Manual calibration of those parameters is just about not possible thanks to the time price. Within the massive knowledge business, there's a requirement to mechanically set up parameters and thereby maximize resource usage. The previous automatic calibration strategies take an extended time to realize the optimum configuration, reducing the cluster's overall performance. With the help of a novel perceptive procedure, each genetic programming and a genetic rule are supported with a view to enhancing the performance of a Hadoop mapeduce work, we propose an assistant in nursing the best configuration finder. We have a tendency to use the algorithms on top of to search out the simplest values for parameter settings. Experiments were performed on four common applications, as well as WordCount, Terasort,Index and Grep, exploitation eight virtual machines in a very typical Hadoop cluster. Our projected methodology will increase MapReduce job potency by fifty three.63 p.c for a one GB dataset and by sixty seven.4 p.c for a five GB dataset, in keeping with the findings and by seventy three.68 p.c on a ten GB dataset additionally, for a terasort programme, MapReduce job potency will increase by fifty two.62 p.c for a one GB dataset, 61.2 p.c for a five GB dataset, and 55.17 p.c for a ten GB dataset. Mapreduce jobs boost the performance of grep applications by forty four.4 p.c for a one GB dataset, 56.25 p.c for a five GB dataset, and 49.44 p.c for a ten GB dataset.

Keywords—Big data processing; resource utilization optimization; parameter tuning; online configuration optimization

I. INTRODUCTION

The volume of data in different fields has exploded in recent decades. Data analysis in a number of fields allows heavy use of high-performance computing and distributed data processing technologies. Hadoop, Spark, Storm, and MARP are some of the most common distributed processing frameworks today. However, as the demand for data processing increases, job efficiency concerns in MapReduce have become increasingly more complex. Many variables also combine to affect performance issues at the same time. Wide configuration parameters, lack of efficient task scheduler, lack of efficient data locality, unbalanced loads, and unbalanced resource slot allotment are some of these factors. These factors create inefficiencies in Hadoop work. Wide configuration parameters are the primary issue in these factors, since the job scheduler, correct location of data, replica placement, and other optimizations all require appropriate configuration parameters [1], [6].

Tuning of Configuration Parameters is a challenging performance problem. In general, parameter tuning of Hadoop configuration is used to enhance the efficiency of a device or model by optimising the combination of different configuration parameters. MapReduce has more than 190 configuration parameters [2]. It includes, for example, the I/O operation, slot source allotment strategy, memory allocation, concurrency, and map and reduce settings, among other things, [8], [9].

MapReduce's most popular methods for optimising configuration parameters currently include combining configuration parameters as well as parameter optimization methods based on simulators, experiment concepts and machine learning[10], [11], [14], [16]. These methods consider into account all parameters during the parameter optimization process. Due to the combination of all setting parameters, the algorithm is highly complex and has a low efficiency. One reason for these problems is that current research does not realize that different MapReduce configuration parameters have differing degrees of significance. Despite the fact that MapReduce has over 190 configuration parameters, each of them has a variant effect towards the job completion time of MapReduce applications. Most of them have a direct effect on MapReduce execution time. The other MapReduce configuration parameters have no effect on the time it takes to run.

Hadoop MapReduce has a huge range of parameters, which makes it a problem to calibrate the parameters. The parameter tuning approach [1] based upon the Kmeans kernel clustering proposes to choose the corresponding parameters which can has the ability to impact the operaion execution time of the Hadoop workers instead of tuning all parameters. The variables chosen include mapred.child.java.opts, mapreduce.job.maps, mapreduce.job.reduces, mapreduce.map.output.compress, mapreduce.task.io.sort.mb and mapreduce.map.combine.minspill.

As a result, the paper introduces an optimization approach based on genetic algorithm to optimize the configuration parameter of MapReduce effectively. The following are the main contributions:

• Based on the execution of Hadoop job samples that are CPU or I/O intensive, genetic programming is used to create an objective fitness function. The constructed fitness function represents and mathematically describes the interrelationships among Hadoop parameters that are thought to affect execution time.

• In this analysis, a GA is used additionally to optimise Hadoop configuration parameters. It is used to look for the best or near-best Hadoop parameter settings using the fitness function provided by genetic programming.

The remaining contents are split into the subsequent elements. In section II, some connected work is conferred, and in section III, a collection of MapReduce parameters is conferred. Section IV discusses the way to use genetic programming to construct associate degree objective feature of MapReduce settings for Hadoop. Section V outlines the implementation of the GA for optimization of the MapReduce parameter, and in section VI, the projected work is evaluated employing a Hadoop cluster within the Microsoft Azure cloud. The outcome of experimens of Hadoop jobs at a very small group on a square measurement of Microsoft Azure are described in Section VII. After that, in section VIII, the paper involves a detailed.

II. RELATED WORK

In recent days configuration parameters of Hadoop are adjusted using simulator methods, network formed due to software, machine learning methods**.** H-Tune [6] is a machine learning optimization algorithm. H-main Tune is not meant to run the Hadoop application, but to predict a particular application output. Initially a profiler evaluates and captures the performance of Hadoop application data. Later, implements a predictor that provides a specific configuration for the performance of the Hadoop application. Also, double-stage fusion model training is used to find the best configuration for MapReduce applications. Furthermore, double-level fusion based model education is used to find the best MapReduce application configuration. However, gathering profiling data takes much too long, and creating a model for all MapReduce applications is extremely difficult.

A known optimization algorithm is the genetic algorithm [14]. MSET [9] is an algorithm for the optimization of genetically modified parameters. To reduce the time needed to obtain profiling data for Hadoop applications with specific configuration, a system is first implemented. The MT algorithm is also used to evaluate applications with different configurations in terms of execution time. Furthermore, the parameters space is searched using an MT-driven genetic Algorithm. However, only the five main parameters MR.map.java.opts, MR.reduce.java.opts, MR.map.memory.mb, MR.reduce.memory.mb, and MR.tasks.io.sort.mb are taken into account.

In order to find appropriate configuration parameters based on application time, DAC [10] also uses a genetic algorithm. Only a few configuration parameters can be dealt with by DAC. BestConfig [12] enables optimisation of settings using an algorithm of bound and search. However, only fixed applications are sufficient.

A simulator HSim is introduced to improve the situation of the machine (processor, buffer, disc, and network and I/O state). The Hadoop platform behaviour can be simulated accurately and system status dynamic transformation parameters reflected. In HSim, several validation benchmark programmes are initially developed for optimizing parameters. In addition, jobs which are constructed for the process of experiment are fed as input into HSim as data sources and the mechanism used for heartbeat is compared with the benchmarking software of the Hadoop cluster. Finally, the variable configuration efficiency can be decided in the comparison process. For easier simulation, a configuration variable was included to the experiments as input, thereby increasing the number of parameters in the application.

Babu et al. [19] propose a advanced optimization for multitenant work, with each job using in its own set of configurations on the Hadoop platform. This method's parameter optimization is explicitly applied by the Hadoop platform, reducing user workload. On the Hadoop network, however, there are different stages, and each stage's operation efficiency is different. As a consequence, judging the accuracy of a best example quickly has some limitations.

Bu et al.[15] use the RL approach to automatically optimise the MapReduce model setup parameters. A Markov Decision Process (MDP) is used to optimise application parameters. All parameter configurations in MDP have the definition of a state space, whereby n parameters represent a set of n-vector states and n actions as one of three types: increase, decrease or interaction. The smallest method is used to maximize the combination of parameters[20]. However, the combined parameters are not always as effective as needed.

AROMA [16] is implemented for automated allocation and setup changes to reduce costs. It employs machine learning methods for group employees and chooses the best setup for each group. AROMA is close to PPABS [17], which categorizes historic jobs based on work performance and resource use. Their main disadvantage is their inefficiency when the new job is dissimilar to any of the previous jobs or cold start problem in the cluster.

In order to accelerate the crossover of the configuration space, mrOnline [7] has modified the Hadoop source code, allowing each task to run in various configurations. But ineffective settings still have to work for a long time before you find the right settings. To evaluate the execution of big data workers, MRTuner [8] developed a Production-Transmission Consumption Model. However, as previously mentioned, the process of restoring the model after a work change is time-consuming.

As set out in [1], [13] and [16] [18], many parameters will increase the training time significantly, and there is also little efficiency in the optimization process. As a result, choosing a few key parameters that have a direct effect on job execution efficiency is a more effective approach for Hadoop MapReduce parameter tuning.

III. III. HADOOP PARAMETERS

Hadoop, being a java-based framework enables large data sets across computer clusters to be distributed for storage or processing. It can store large quantities of any kind of data because of its scalability and fault tolerance (structured, semistructured, and unstructured data). It also has more than 150 tunable variables that have a significant impact on Hadoop MapReduce's flexibility and some of them significantly affect the efficacy of Hadoop's work. The main device parameters for the efficiency of Hadoop work are listed in Table 1.

Below is a more comprehensive overview of the table 1's key parameter settings.

1) **mapReduce.task.io.sort.mb**: Each merge stream requires a certain amount of buffer memory when sorting data. This parameter specifies the size of each merge stream, which is set to 1MB by default.

2) mapReduce.task.io.sort.factor: The default value is set to 10,which specifies the number of merged streams used in the sorting process of the files.

3) mapred.compress.map.output: The output of the mapper needs to be sent to the reduces during the process of shuffling. If the output is sent withput compression is creates information traffic. Hence to speed up the hard disc's Input/output, the output results of the mappers should be compressed.

4) mapReduce.job.reduces: This parameter specifies the count of map tasks that are required in a Hadoop cluster. This parameter specifies the amount of map tasks. The value of this parameter is set to 1 by default. Furthermore, the efficiency of Hadoop jobs is affected by this parameter.

5) mapreduce.map.sort.spill.percent: This reflects the buffer threshold for map process and is usually 0.80.This means when the memory buffer size exceeds 80% input data is spilled to the hard disc.

6) mapReduce.tasktracker.reduce.tasks.maximum: The Task Tracker runs several maps and reduces tasks for each MapReduce job at each data node in the Hadoop cluster. This number indicates the task number to be reduced and the default value is 2. This parameter impacts the cluster effectiveness by using cluster processor and memory.

7) mapReduce.tasktracker.map.tasks.maximum: While parameter 6 specifies the number of reduction tasks, it specifies the number of simultaneous map tasks at each node. This variable defaults to 2. Any adjustment in this parameter's default settings can, by contrast, have a positive influence on MapReduce's total time.

8) mapReduce.reduce.shuffle.input.buffer.percent: The mapreduce job requires some capacity of storage memory from the total size of heap. The amount of percentage of mount is specified using this variable and defaults to 0.70.

TABLE 1. Default variable settings of Hadoop Framework

Parameters	Framework values
mapReduce.task.io.sort.mb	100
mapReduce.task.io.sort.factor	10
mapred.compress.map.output	False
mapReduce.job.reduces	1
mapreduce.map.sort.spill.percent	0.80
mapReduce.tasktracker.reduce.tasks.maximum	2
mReduce.tasktracker.map.tasks.maximum	2
mapReduce.reduce.shuffle.input.buffer.percent	0.70

IV. OPTIMAL PARAMETER SEARCHING WITH GENETIC PROGRAMMING

A fitness feature is developed based on Hadoop job's performance using genetic algorithm. This feature depicts the interrelations between Hadoop performance variables and describes them mathematically. To optimize the Hadoop performance variables GA is used for analysis. This GA is applied to the fitness feature generated by GA to find optimal or near optimal Hadoop variable settings. The configurations of the Hadoop job samples are altered for best performance settings.

Genesis (GP) is a method used for automatically resolving problems with a collection of genes and chromosomes. Two basic genetic operations used for the development of this are crossover and mutation. GP is used to build a MapReduce parameter objective function in this article. The Hadoop MapReduce is shown as (p1, p2 ...pn,) and a genetics algorithm is employed for eight parameters (GA). For an objective function first, GP should be used. As a result, between these parameter settings a mathematical expression or function must be defined. GP builds a parameter link between these variables by arithmetic operations (multiplication, addition,substraction, division).The value of correct fitness given to each variable during population phase needs to have the similarity between the fitness feature performance to that of the respective parameter. In GP, functions are known as arithmetic operations. The parameters (p1, p2... pn) are designated as terminals. On the basis of data type the mathematical equation of the MapReduce parameters is calculated. The number of parameters and the input data form should be equal in the mathematical equation. The fitness function completion time needs comparison and measurement in real time. The best fitted mathematical equation between the variables (p1... pn) is selected based on their approximate completion time very close to the real

value. The GA tree contains both terminals (p1, p2….pn) and functions (*, +, /,-).

Hadoop variables are combined to describe a Mapreduce job's completion time (p1,p2,….pn).The job completion time of the objective function should be nearly equal to the actual time of job completion of Hadoop job and almost similar to the target problem's completion time.

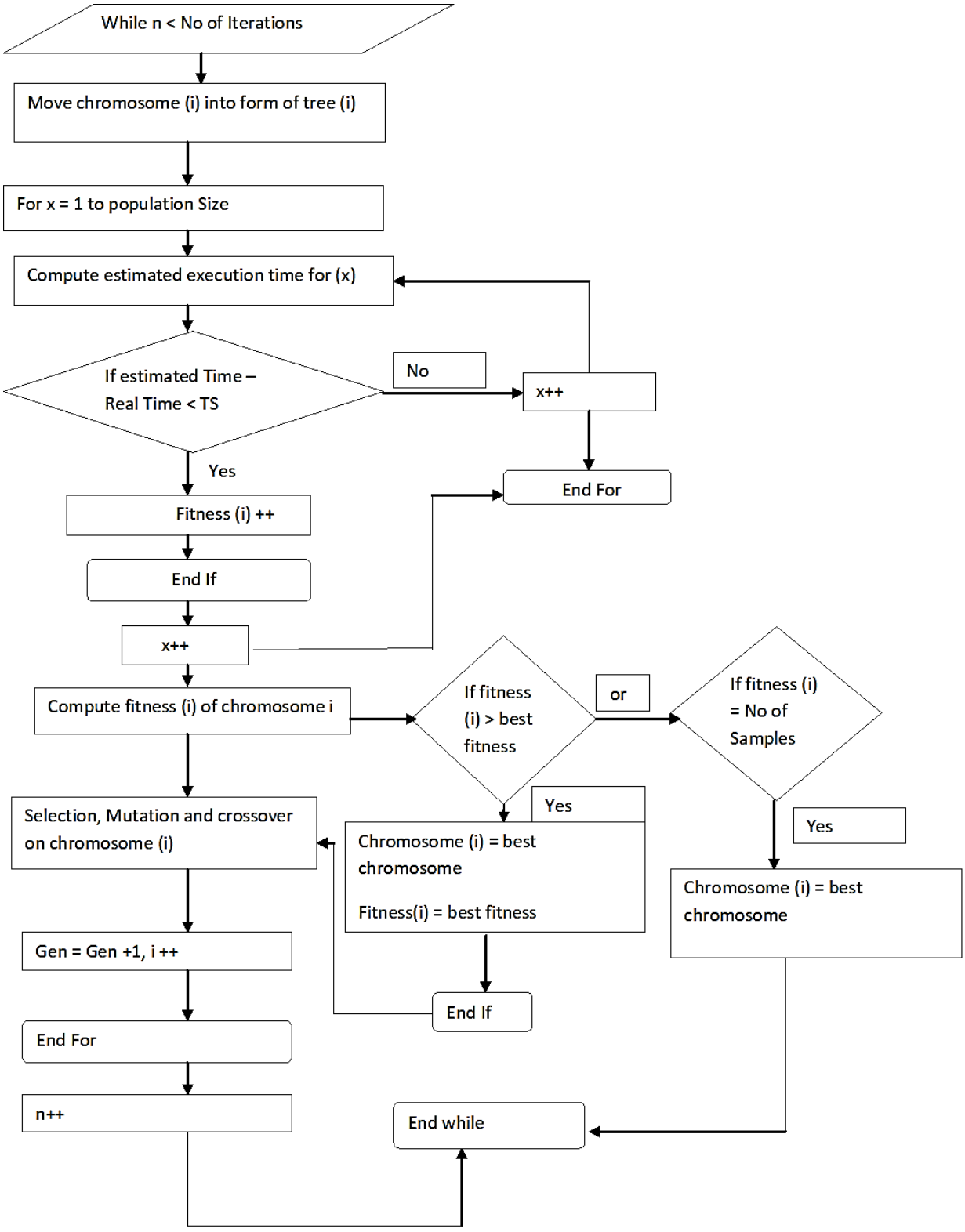


Figure 1 Flowchart1 - Genetic Programming

Flowchart 1 illustrates GP procedures. The common Hadoop applications like Word count, Index, Grep and TeraSort are taken as datasets and multiple experiments are carried out using different data sizes of these application datasets. As mentioned above GP is used for every possible expression between mapreduce variables by generating 600 of chromosomes initially in this analysis. The graphitic values in both linear chromosomes are calculated on the basis of the period of completion of the Hadoop job for each dataset of training. The real job execution time of the specific mapreduce job and the completion time of this f (p1, p2..Pn) is compared .Their difference is maintained to be not more than 40 seconds (also known as TS).The most fitness efficient chromosome is selected. The number of parameters considered in both the scenarios needs to be the same. This is continued until the specified number of iterations, once the best fitted value is reached. New chromosomes are created and existing ones are changed through mutation and crossover. The expression is detected after 30,000 iterations. The below equation represents the relationship between mapreduce variables and is used in the mentioned algorithm.

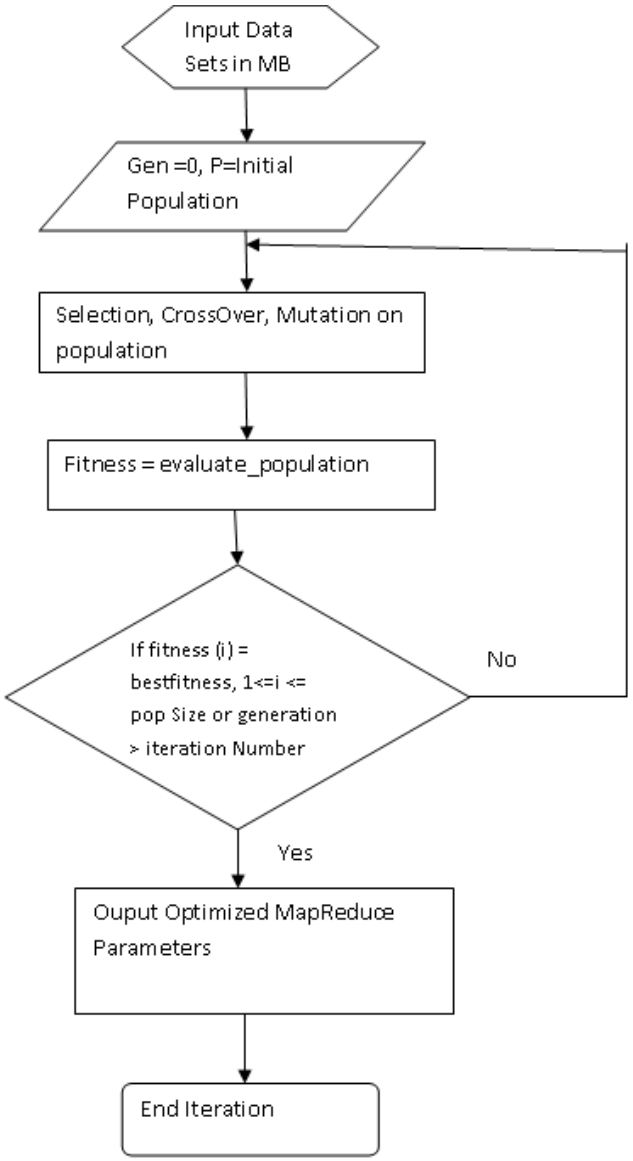
$$f(p1, p2. . . p8)=(p3+p7) * (p5/p2)+(p1 * p6) - (p4+p8) \quad (1)$$

V. V.CONFIGURATION TUNING BY GENETIC ALGORITHM

A genetic algorithm (GA) is novel intelligent technique that is part of the evolutionary algorithm (EA) family, initially proposed by John Holland to more effectively resolve complex problems. Many problems of optimization based on natural processes are addressed by GAs. They work on a synthetic chromosome collection that provides different solutions. The fitness value of every chromosome determines how good it is to solve the problem [18]. GAs start with the creation of a haphazard chromosome population. For the given problem multiple critical genetic operations like crossover, mutation are implemented to optimize the solution. The effective value of chromosomes is used to direct the selection process. The chromosome with the highest fitness has a chance to be selected and develop offspring to help the population grow [21]. The GA implementation procedure is defined in algorithm 2, in which GP-generated equation 1, selected the objective function to be optimized and written as follows:

$$f(p1, p2, .., pn) = (p3+p7) * (p5/p2)+(p1*p6) - (p4+p8)$$

Flowchart2 creates a random chromosome population and represents one of these chromosomes each MAPReduce parameter. Chromosome I = the number of parameters in p1, p2,...,pn. As mentioned above, eight parameters have to be defined in this work. The fitness value of every chromosome is measured using the objective function f following population production (p1, p2,.., pn).



Flowchart2 Genetic Algorithm

The chromosome with highest fitness is chosen and a new population is upgraded to generate genetic operators like selection, crossover and mutation The procedures shall continue to work until the most effective chromosome fitness values are obtained, representing optimized parameters of MapReduce or achieving the number of iterations. The population is 15 chromosomes in this algorithm and 200 iterations. Moreover, empirically, and as genetic operators the probability of crossover (Pc=0.1) and mutation (Pm=0.2) is measured. As a selection tool, the spinning of the wheel is used. Table 2 displays the arrived values for the eight job parameters.

TABLE 2. Hadoop mapreduce genetic algorithm recommended parameters

Hadoop Map reduce Parameters	Range	Parameters Name
P1	100-165	MapReduce.task.io.sort.mb
P2	10-160	MapReduce.task.io.sort.factor
P3	True	Mapred.compress.map.output
P4	1-16	MapReduce.job.reduces
P5	0.60-0.70	Mapreduce.map.sort.spill.percent
P6	2-4	MapReduce.tasktracker.map.tasks.maximum
P7	2-4	MapReduce.tasktracker.reduce.tasks.maximum
P8	0.70-0.71	MapReduce.reduce.shuffle.input.buffer.percent

VI. PERFORMANCE EVALUATION ENVIRONMENT

A Hadoop cluster of 5 virtual machines (VMs) was used to implement and test the proposed work. For the entire cluster, each VM was given 4 GB of memory including 4 CPU cores, and 250 GB of storage. Every node is constructed with Hadoop Cloudera (Hadoop 3.3.0), one master and the others as slaves. The replication factor of the data block is set to 3 for defective tolerances, and a 128 MB block size for HDFS. The specifications of the Hadoop cluster are set out in Table 3.

Table 3 Hadoop Network Setup

IntelCore (TM) i5 -8265U CPU	CPU	4 Cores for each VM
	Processor	1.60 Ghz
	Hard Disk	1 TB
	Memory	12GB
Operating System	Host Operating System	Microsoft windows Server 2010
	Guest Operating System	CentOS-6.8-x86_64

VII. EVALUATION RESULTS

The Grep, WordCount, Tera Sort and Index applications are executed as Hadoop test jobs to find the results of our proposed algorithm. There is an obvious difference between the tuned configurations and the default setting of the Hadoop MapReduce setting. Figure 3 demonstrates that increasing the io.sort.mb value reduces execution time in Hadoop MapReduce.

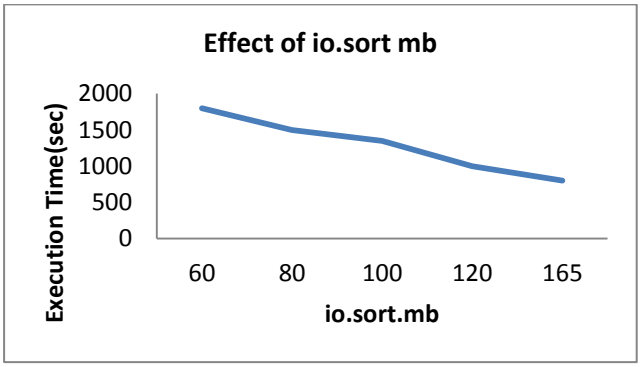


Figure 1 The influence of io.sort mb

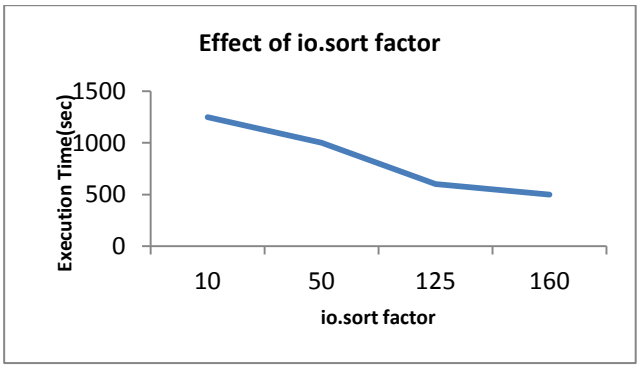


Figure 2 The influence of io.sort factor

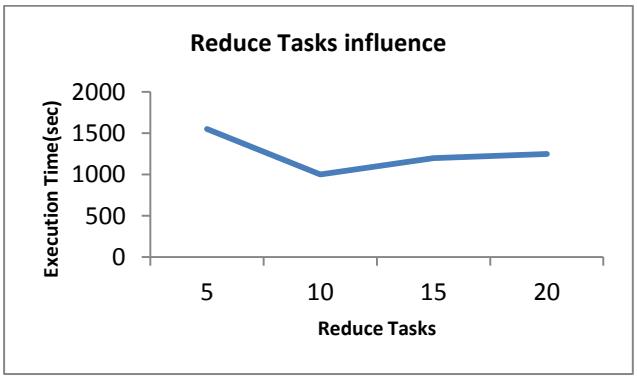


Figure 3 the influence of reduce tasks

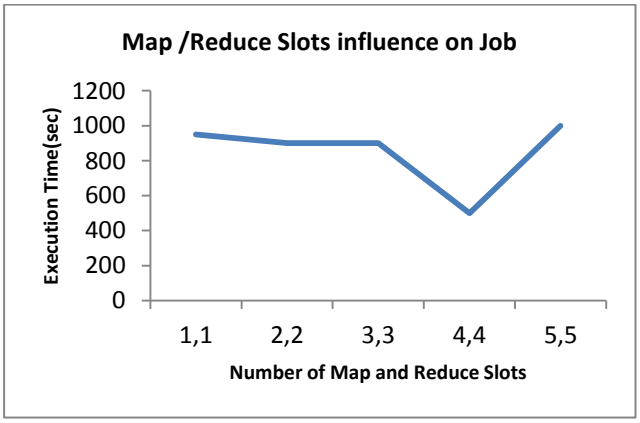


Figure 4 influence of Map/Reduce Slots

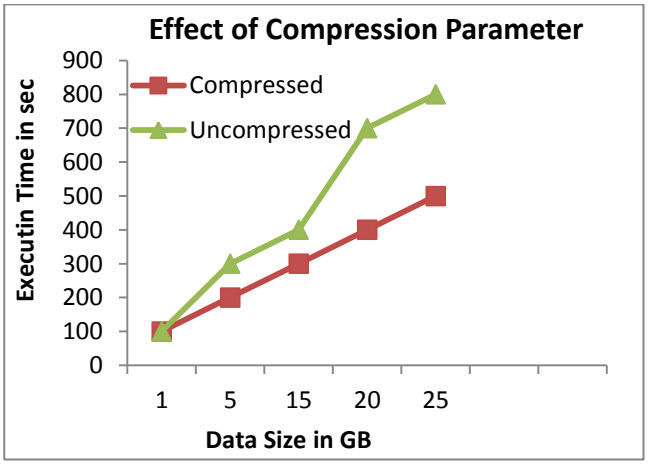


Figure 5 Effect of Compression Parameter

In addition, the io-sort-factor parameter specifies the number of data streams to combine during file sorting process. Figure 1 shows that the work execution time decreases as the value of this parameter increases. Figure 1 also indicates that the Hadoop MapReduce job execution time decreases when the reduce tasks is incremented from 5 to 10. Increased tasks reduction however increases the time required to execute due to overhead network and exploitation of CPU and memory computing resources. In addition, any additional increase in reduction tasks will eventually lead to increased traffic in the networks, resulting in an increase in Hadoop work time. Figure 4 shows how the number of maps and slots can help to use cluster resources better and thus reduce time overall. One slot has been set up per CPU core to optimize CPU use. Four cores were assigned to each cluster node, resulting in four slots in the cluster configuration. The CPU is used to delay the job processing time if more slots are added to the setup. For each dataset size on four virtual machines, Table4 shows the optimized Hadoop MapReduce parameter values. The performance of our system was demonstrated in different sizes, including 1 GigaByte, 5 GigaByte, and 10 GigaByte. The fine-tuned parameters were utilized for Word Count, Grep, Index and TeraSort applications. Based on tuned variables, this proposed method compares the execution time with the completion time for the apps based on TABLE 4 default. All applications have been running twice and our proposed method is found to improve the job performance in a network cluster, especially when the input data size is high. In contrast to the default method, Figure 6,7,8,9 indicates the job execution time of a specified jobs using the proposed method. Figure 6 show that the proposed solution increases the efficiency of the Hadoop Word Count Application by 63 percent for the 1 GB dataset as compared to the default settings. Furthermore, tests on a 5 GB dataset shows that this proposed method increases the efficiency of the Word Count Application by 69 percent. The above proposed method improved the TeraSort application efficiency by 52.73 percent over the default for 1GB, as shown in Figure 7. The performance of 5 GB was improved by 51.5 percent over the average, while the performance of 10 GB was improved by 55.17 percent over the default.

Table 4 Hadoop genetic algorithm parameter settings for 4 virtual machines

Name	Default	Optimized Values		
		1 GB	5 GB	10 GB
mapReduce.task.io.sort.mb	100	100	120	140
mapReduce.task.io.sort.factor	10	50	100	125
mapred.compress.map.output	false	True	True	True
mapReduce.job.reduces	1	16	10	10
mapreduce.map.sort.spill.percent	0.80	0.87	0.72	0.68
mapReduce.tasktracker.map.tasks.maximum	2	4	4	4
mapReduce.tasktracker.reduce.tasks.maximum	2	4	3	4

Figure 8 show that this proposed method has increased Grep application efficiency by 55.55 percent for 1GB as compared to the default framework. The performance of 5 GB was improved by 50.5 percent over the average, while the performance of 10 GB was improved by 47.19 percent over the default. Figure 9 show that this proposed method optimized the Index application efficiency by 40% as compared to the default framework for 1GB. The performance of 5 GB was improved by 51.67 percent over the average, while the performance of 10 GB was improved by 44.4 percent over the default.

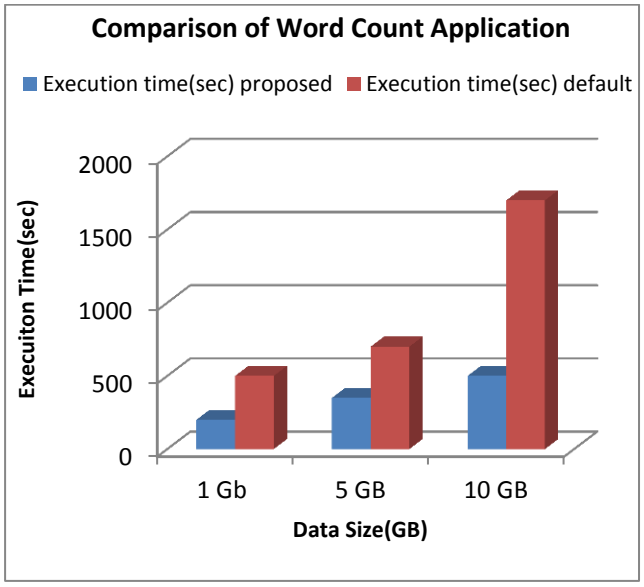


Figure 6 Performance of Word Count Application

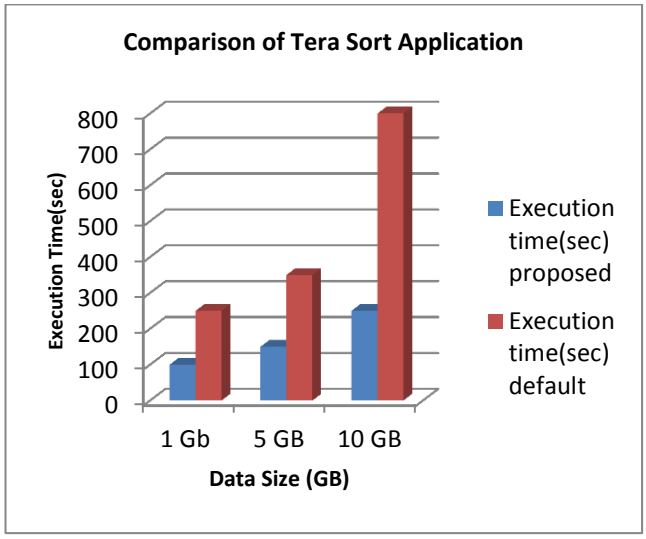


Figure 7 Performance of Tera Sort Application

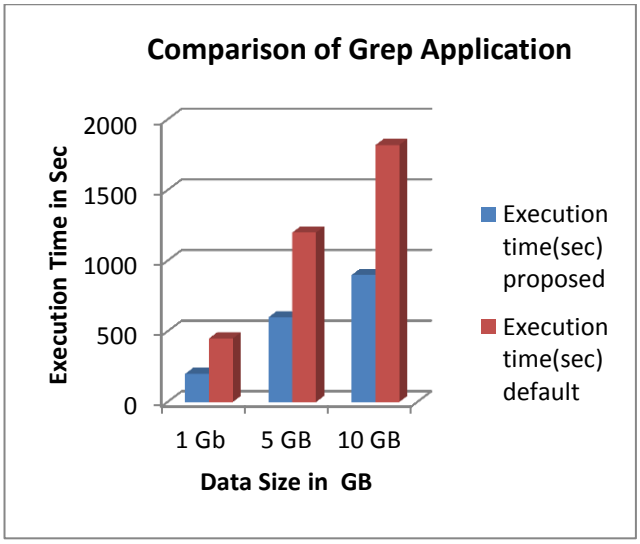


Figure 8 Performance of Grep Application

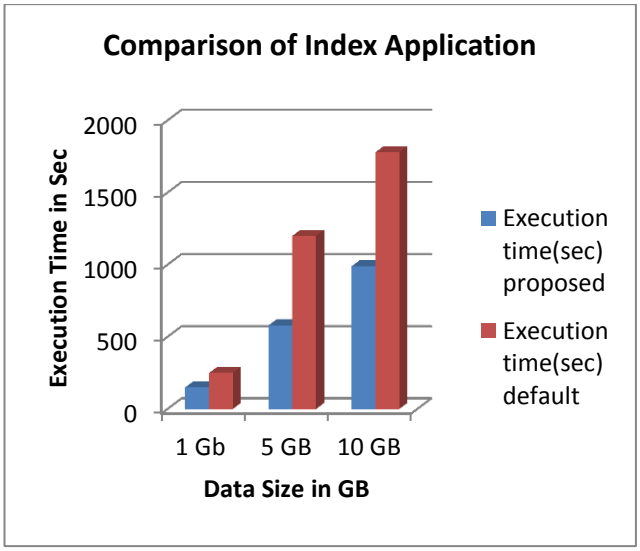


Figure 9 Performance of Index Application

VIII. CONCLUSION

In this proposed work, the configuration parameters of Hadoop MapReduce have been automatically adjusted using both genetic and génetic programming. Optimizing configuration parameter settings has enhanced the programming component of the Hadoop system. As a result of the upgrade, it takes less time to complete Hadoop MapReduce jobs. A number of applications, including Word Count, Grep, Tera Sort and Index, were executed to experiment the MapReduce job output of the Hadoop network. The experimental results proved that Hadoop jobs work better than a typical default variable setting network of data centres.

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Overuse of Steroid Drugs Methylprednisolone and Dexamethasone (Oral) Causes a Diabetic Patient to Become Infected With the Black Fungus in the Corona Virus

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Abstract—Background: Overuse of both methylprednisolone and dexamethasone drug on a corona patient can result in serious side effects and new infections may appear during their use. Infection with any pathogen, including viral, bacterial, fungal, protozoan, or helminthic infections at any site of the body, may be associated with the use of methylprednisolone or dexamethasolone in combination with other immunosuppressive agents that increase cellular immunity, humoral immunity, or Suppress neutrophils. The function they affect.

These infections can be mild, but can be serious and sometimes fatal. With increasing doses of methylprednisolone and dexamethasone, the rate of occurrence of infectious complications increases. When methylprednisolone and dexamethasone are used, there may be reduced resistance and inability to localize the infection.

Prolonged use of methylprednisolone and dexamethasone may produce posterior subcapsular glaucoma, glaucoma with potential damage to the optic nerves, and may accelerate the establishment of secondary ocular infections caused by fungi or viruses.

It has also been observed that more methylprednisolone and dexamethasone drug increases the level of glucose in the body, leading to normal corona patients who do not have any disease and diabetes after recovering from excessive consumption of methylprednisolone and dexamethasone drug.

Materials and Methods: A cross sectional study was conducted among 50 COVID doctors from the department's outpatient pool of COVID patients, distributing questionnaires to all subjects of different age groups. The questionnaire included information related to the name, age, gender and various factors that affect the doctor's choice of methylprednisolone and dexamethasone.

Result and Discussion: A total of 50 doctors and some medical stores from across India were included in the survey. Doctors prescribed more methylprednisolone and dexamethasone medicine than steroid medicines to corona patients. In our research, most side effects were observed for corona patients taking methylprednisolone and dexamethasone drug.

Conclusion: This research had shown that overdose of methylprednisolone and dexamethasone drug take diabetes patient he has serious eye effect and cause black fungus.

Keywords— Methylprednisolone, Dexamethasone, Side Effect, Drug Interaction, Diabetes Patients, Black Fungus, Eye Diseases

I. INTRODUCTION

Methylprednisolone (Depo-Medrol, Medrol, Solu-Medrol) is a synthetic glucocorticoid, primarily prescribed for its anti-inflammatory and immunosuppressive effects.[1],[2],[3] It is either used at low doses for chronic illnesses or used concomitantly at high doses during acute flares. Methylprednisolone and its derivatives can be administered orally or parenterally.[4]

Regardless of route of administration, methylprednisolone integrates systemically as exhibited by its effectiveness to quickly reduce inflammation during acute flares.[5] It is associated with many adverse reactions that require tapering off the drug as soon as the disease is under control.[6] Serious side effects include iatrogenic Cushing's syndrome, hypertension, osteoporosis, diabetes, infection, and skin atrophy.[6]

Chemically, methylprednisolone is a synthetic pregnane steroid hormone derived from hydrocortisone and prednisolone. It belongs to a class of synthetic glucocorticoids and more generally, corticosteroids. It acts as a mineralocorticoid and glucocorticoid receptor agonist. In comparison to other exogenous glucocorticoids, methylprednisolone has a higher affinity to glucocorticoid receptors than to mineralocorticoid receptors.

Glucocorticoid's name was derived after the discovery of their involvement in regulating carbohydrate metabolism.[6] The cellular functions of glucocorticoids, such as methylprednisolone, are now understood to regulate homeostasis, metabolism, development, cognition, and inflammation.[6] They play a critical role in adapting and responding to environmental, physical and emotional stress.[6]

Methylprednisolone was first synthesized and manufactured by The Upjohn Company (now Pfizer) and FDA approved in the United States on October 2, 1957.[7] In 2018, it was the 153rd most commonly prescribed medication in the United States, with more than 4 million prescriptions.[8][9] Methylprednisolone has been a prescribed therapy amidst the COVID-19 pandemic, but there is no evidence it is either safe or effective for this purpose.[10],[11]

Dexamethasone is a glucocorticoid medication[12] used to treat rheumatic problems, a number of skin diseases, severe allergies, asthma, chronic obstructive lung disease, croup, brain swelling, eye pain following eye surgery, and along with antibiotics in tuberculosis.[12]

In adrenocortical insufficiency, it may be used in combination with a mineralocorticoid medication such as fludrocortisone.[12] In preterm labor, it may be used to improve outcomes in the baby.[12] It may be given by mouth, as an injection into a muscle, as an injection into a vein, as a topical cream or ointment for the skin or as a topical ophthalmic solution to the eye.[12] The effects of dexamethasone are frequently seen within a day and last for about three days.[12]

The long-term use of dexamethasone may result in thrush, bone loss, cataracts, easy bruising, or muscle weakness.[12] It is in pregnancy category C in the United States, meaning that it should only be used when the benefits are predicted to be greater than the risks.[13] In Australia, the oral use is category A, meaning it has been frequently used in pregnancy and not been found to cause problems to the baby.[14] It should not be taken when breastfeeding.[12]

Dexamethasone has anti-inflammatory and immunosuppressant effects.[12]

Dexamethasone was first synthesized in 1957 by Philip Showalter Hench and was approved for medical use in 1961.[15],[16],[17] It is on the World Health Organization's List of Essential Medicines.[18] In 2017, it was the 321st most commonly prescribed medication in the United States, with more than one million prescriptions.[19]

AIM: To study the factors that influence doctor's choice of methylprednisolone and dexamethasone and to understand the most preferred options in selection with respect to the methylprednisolone and dexamethasone.

II. MATERIALS AND METHODS

A cross sectional study was conducted among 50 covid doctor from the outpatient pool of Department of covid patients were briefed about the study and informed consent was obtained from them and ethical committee approval was obtained from the University. Questionnaires were distributed to all subjects of various age groups. The questionnaire included information related to the covid patient's name, age, gender and various factors that influence a doctor's choice of methylprednisolone and dexamethasone.

Description

MEDROL Tablets contain methylprednisolone which is a glucocorticoid. Glucocorticoids are adrenocortical steroids, both naturally occurring and synthetic, which are readily absorbed from the gastrointestinal tract. Methylprednisolone occurs as a white to practically white, odorless, crystalline powder. It is sparingly soluble in alcohol, in dioxane, and in methanol, slightly soluble in acetone, and in chloroform, and very slightly soluble in ether. It is practically insoluble in water.

The chemical name for methylprednisolone is pregna - 1, 4 - diene - 3, 20-dione, 11, 17, 21-trihydroxy-6-methyl-, (6α, and 11β)-and the molecular weight is 374.48. The structural for-mula is represented below:

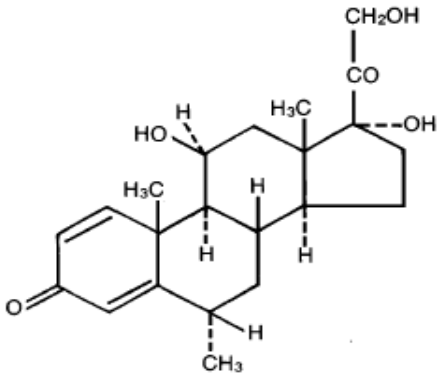

Figure No 1:- Chemical Structure of Methylprednisolone.

Each MEDROL (methylprednisolone) Tablet for oral administration contains 2 mg, 4 mg, 8 mg, 16 mg or 32 mg of methylprednisolone.

DEXAMETHASONE, a synthetic adrenocortical steroid, is a white to practically white, odorless, crystalline powder. It is stable in air. It is practically insoluble in water. The molecular formula is $C_{22}H_{29}FO_5$. The molecular weight is 392.47. It is designated chemically as 9-fluoro-11β, 17, 21-trihydroxy-16α-methylpregna-1, 4-diene, 3, 20-dione and the structural formula is:

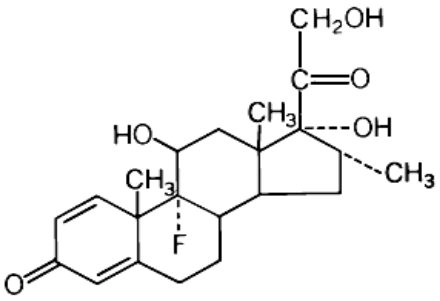

Figure No 2:- Chemical Structure of Dexamethasone.

Dexamethasone provides relief for inflamed areas of the body. It is used to treat a number of different conditions, such as inflammation (swelling), severe allergies, adrenal problems, arthritis, asthma, blood or bone marrow problems, kidney problems, skin conditions, and flare-ups of multiple sclerosis. Dexamethasone is a corticosteroid (cortisone-like medicine or steroid). It works on the immune system to help relieve swelling, redness, itching, and allergic reactions.

III. SIDE EFFECTS of METHYLPREDNISOLONE

✓ **Fluid and Electrolyte Disturbances**

Sodium retention, Congestive heart failure in susceptible patients, Hypertension, Fluid retention, Potassium loss, Hypokalemic alkalosis etc.

- ✓ **Musculoskeletal**
  Muscle weakness, Loss of muscle mass, Steroid myopathy, Osteoporosis, Tendon rupture, particularly of the Achilles tendon, Vertebral compression fractures, Aseptic necrosis of femoral and humeral heads, Pathologic fracture of long bones etc.
- ✓ **Gastrointestinal**
  Peptic ulcer with possible perforation and hemorrhage, Pancreatitis, Abdominal distention, Ulcerative esophagitis, Increases in alanine transaminase (ALT, SGPT), aspartate transaminase (AST, SGOT), and alkaline phosphatase have been observed following corticosteroid treatment. These changes are usually small, not associated with any clinical syndrome and are reversible upon discontinuation etc.
- ✓ **Dermatologic**
  Impaired wound healingPetechiae and ecchymoses, May suppress reactions to skin tests, Thin fragile skin, Facial erythema, Increased sweating etc.
- ✓ **Neurological**
  Increased intracranial pressure with papilledema (pseudo-tumor cerebri) usually after treatment, Convulsions, Vertigo, Headache etc.
- ✓ **Endocrine**
  Development of Cushingoid state, Suppression of growth in children, Secondary adrenocortical and pituitary unresponsiveness, particularly in times of stress, as in, trauma, surgery or illness, Menstrual irregularities, Decreased carbohydrate tolerance.
- ✓ Manifestations of latent diabetes mellitus Increased requirements of insulin or oral hypoglycemic agents in diabetics
- ✓ **Ophthalmic**
  Posterior subcapsular cataracts, Increased intraocular pressure, Glaucoma, Exophthalmos
- ✓ **Metabolic**
  Negative nitrogen balance due to protein catabolism

The following additional reactions have been reported following oral as well as parenteral therapy: Urticaria and other allergic, anaphylactic or hypersensitivity reactions.[22]

IV. SIDE EFFECTS OF DEXAMETHASONE

The following side effects have been reported with dexamethasone or other corticosteroids:

Allergic Reactions

Anaphylactoid reaction, anaphylaxis, angioedema.

Cardiovascular

Bracardia, cardiac arrest, cardiac arrhythmias, cardiac enlargement, circulatory collapse, congestive heart failure, fat embolism, hypertension, hypertrophic, cardiomyopathy in premature infants, myocardial rupture following recent myocardial infarction, edema, pulmonary edema, syncope, tachycardia, thromboembolism, thrombophlebitis, vasculitis etc

Dermatologic

Acne, allergic dermatitis, dry scaly skin, ecchymoses and petechiae, erythema, impaired wound healing, increased sweating, rash, striae, suppression of reactions to skin tests, thin fragile skin, thinning scalp hair, urticaria etc.

Endocrine

Decrease carbohydrate and glucose tolerance, development of cushingoid state, hyperglycemia, glycosuria, hirsutism, hypertrichosis, increased requirements for insulin or oral hypoglycemic agents in diabetes, manifestations of latent diabetes mellitus, menstrual irregularities, secondary adrenocortical and pituitary unresponsiveness (particularly in times of stress, as in trauma, surgery, or illness), suppression of growth in pediatric patients.

Fluid and Electrolyte Disturbances

Congestive heart failure in susceptible patient's fluid retention, hypokalemic alkalosis, potassium loss, sodium retention etc.

Gastrointestinal

Abdominal distention, elevation in serum liver enzyme levels (usually reversible upon discontinuation), hepatomegaly, increased appetite, nausea, pancreatitis, peptic ulcer with possible perforation and hemorrhage, perforation of the small and large intestine (particularly in patients with inflammatory bowel disease), ulcerative esophagitis.

Metabolic

Negative nitrogen balance due to protein catabolism.

Musculoskeletal

Aseptic necrosis of femoral and humeral heads, loss of muscle mass, muscle weakness, osteoporosis, and pathologic fracture of long bones, steroid myopathy, tenson rupture, and vertebral compression fractures.

Neurological/Psychiatric

Convulsions, depression, emotional instability, euphoria, headache, increased intracranial pressure with papilledema (pseudotumor cerebri) usually following discontinuation of treatment, insomnia, mood swings, neuritis, neuropathy, paresthesia, personality changes, psychic disorders, vertigo etc.

Ophthalmic

Exophthalmos, glaucoma, increased intraocular pressure, posterior subcapsular cataracts.[23]

DRUGS INTERACTION

DECADRON may interact with aminoglutethimide, potassium-depleting agents (e.g., amphotericin B, diuretics), macrolide antibiotics, anticholinesterases, oral anticoagulants, antidiabetics, antitubercular drugs, cholestyramine, cyclosporine, dexamethasone suppression tests (DST), digitalis glycosides, ephedrine, estrogens and oral contraceptives, barbiturates, phenytoin, carbamazepine, rifampin, ketoconazole, aspirin or other nonsteroidal anti-inflammatory drugs (NSAIDs), phenytoin, skin tests, thalidomide, and live or inactivated vaccines. Tell your doctor all medications and supplements you use and all vaccines you recently received. Decadron should be used during pregnancy or during breastfeeding only if the potential benefit justifies the potential risk to the fetus or infant. Infants may suffer adrenal suppression if their mothers use this drug during pregnancy. In special instances (for example, leukemia and nephrotic syndrome), Decadron has been used in pediatric patients. Such use should be done in most patients in conjunction with a pediatric specialist.

MEDROL may interact with aspirin (taken on a daily basis or at high doses), diuretics (water pills), blood thinner, cyclosporine, insulin or oral diabetes medications, ketoconazole, rifampin, seizure medications, or "live" vaccines. Tell your doctor all medications and supplements you use and all vaccines you recently received.[24]

Corticosteroids may mask some signs of infection, and new infections may appear during their use. Infections with any pathogen including viral, bacterial, fungal, protozoan or helminthic infections, in any location of the body, may be associated with the use of corticosteroids alone or in combination with other immunosuppressive agents that affect cellular immunity, humoral immunity, or neutrophil function.[25]

These infections may be mild, but can be severe and at times fatal. With increasing doses of corticosteroids, the rate of occurrence of infectious complications increases.[26] there may be decreased resistance and inability to localize infection when corticosteroids are used.

Prolonged use of corticosteroids may produce posterior subcapsular cataracts, glaucoma with possible damage to the optic nerves, and may enhance the establishment of secondary ocular infections due to fungi or viruses.

V. BLACK FUNGUS INFECTION (MUCORMYCOSIS)

- ✓ Black fungus, also known as Mucormycosis, is a rare but dangerous infection. Black fungus is caused by getting into contact with fungus spores in the environment. It can also form in the skin after the fungus enters through a cut, scrape, burn, or another type of skin trauma.
- ✓ Fungi live in the environment, particularly in soil and decaying organic matter such as leaves, compost piles, rotten wood, and so on. This fungal infection is caused by a type of mould known as 'mucromycetes'. It should be noted that this rare fungal infection affects persons who have health issues or who use drugs that weaken the body's ability to fight the infections. [27]

Black Fungus Causes:

- ✓ Mucormycetes are a type of mould that causes fungal infections. These moulds can be found everywhere in the environment, including soil, air, and food. They enter the body via the nose, mouth, or eyes and can have an impact on the brain if it is not treated on time. According to medical experts, the main cause of black fungus (mucormycosis) is steroid overuse during COVID treatment.
- ✓ Black fungus (mucormycosis) primarily affects people who have health problems or who take medications that reduce the body's ability to fight germs and illness. The person's immunity is low after covid treatment, which makes them vulnerable to black fungus infection. People with diabetes and COVID-19 patients are at greater risk of developing an infection. [27]

Black Fungus Risks:

- ✓ People who fall into the following categories are more likely to develop black fungus:
- ✓ Uncontrolled diabetes, diabetic ketoacidosis, and diabetics taking steroids or tocilizumab.
- ✓ Patients taking immunosuppressant's or receiving anticancer treatment, as well as those suffering from a chronic debilitating illness
- ✓ Patients taking high doses of steroids or tocilizumab for an extended period
- ✓ Cases of COVID-19 Severity
- ✓ Patients on oxygen who required nasal prongs, a mask, or a ventilator support
- ✓ Patients who get COVID treatment within six weeks are more likely to develop black fungus.[27]

VI. RESULT AND DISCUSSION

A total of 50 doctors and some medical stores from across India were included in the survey. Doctors prescribed more methylprednisolone and dexamethasone drug medicine than steroid medicines to corona patients.

In our research, most side effects were observed for corona patients taking methylprednisolone and dexamethasone drug.

Due to over-prescription of doctors, we came to know from other studies that diabetics who were cured of taking methylprednisolone and dexamethasone medicine when

they had corona, got a disease called black fungus after some time. And more deaths from black fungus disease were seen in diabetic patients.

We also found in our survey that Methylprednisolone drug is prescribed more by the doctor in corona patients. Compared to methylprednisolone, doctor prescribed dexamethasone drug is less given in corona patients.

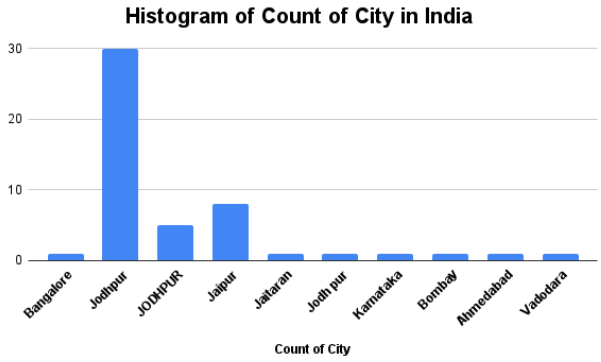

Figure 3:- Names of The Cities We Placed In Our Survey.

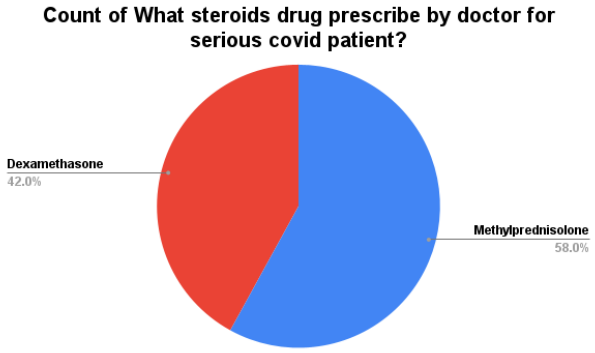

Figure 4:- Survey of Which Steroid Drug Is More Prescribed By the Doctor In Covid-19 Patients

VII. CONCLUSION

This research had shown that overdose of methylprednisolone and dexamethasone drug take diabetes patient he has serious eye effect and cause black fungus.

It has been found from research that three things have been detected by giving high amount of steroid drugs to corona patients.

1) Patients who have been cured of corona, who did not have any disease before corona, after recovering from corona in their body, after going home, they have diabetes.
2) Those corona patients who already have diabetes, after being cured by giving more steroid medicine, they got a complaint of black fungus disease.
3) These two things have shown that more steroids are being given to corona patients than giving more side effects because giving more steroids reduces immunity in the body, due to which the black fungus present in the environment is easily found in patients with low immunity. It goes away and the infection increases in the patient's eyes, if the patient does not take treatment on time, then his life is also lost.

However very less work has been on this drug & there is further more scope of scientific investigation.

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Power and Area Efficient VLSI Architecture for Fault Tolerant Method using Magnitude Comparator

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Abstract— Issues caused by perseverance in secure-resistive fundamental memories, leads to the research of the proposed paper, this paper is designed for enduring stuck-at faults in secure-resistive fundamental memories. This methodology uses a number of memory regions with stuck-at faults to store the data appropriately, as well as the random features of the Advanced Encryption Standard-encoded data (AES) as a rotational shift activity. This design results show that the energy consumption is fundamentally lower than that of existing approaches due to its simple hardware implementation. In contrast with the three errors tolerating methods the implementation of the proposed design is done using the main memory system that is based on Phase-Change Memory. Advantage of this technique is that it can use other error correction methods such as ECC and ECP.

Keywords— ECC Error correction code, ECP Error correction pointer

I. INTRODUCTION

Cloud servers have become more computationally intensive, necessitating increasing core counts and memory density. For every two years the core Processors double, whereas for every three years, the capacity of DRAM DIMMs doubles. As a result, there is a significant discrepancy between the number of cores and the density of memory. Conventional Dynamic RAM chips require over 40% of the energy used by servers. In addition, scaling DRAM to achieve increased density of memory has several drawbacks, such as increased current leakage, worse reliability of memory cells, and more complicated production methods. To address scaling and power consumption issues, new memory technologies have been invented, which are divided into nonvolatile DRAM-based (resistive-based)and volatile (DRAM-based).Low-power DDR DRAM architectures, such as LPDDR3, LPDDR4, have low latency and tiered latency. DRAM is a type of memory that is used Volatile DRAM-based memory such as RL-DRAM and TL-DRAM are examples. The fabrication process expenses are higher though their latency and power consumption is low. Spin-transfer torque RAM (STT-RAM), phase-change memory (PCM), resistive RAM (ReRAM), and 3DXpoint are examples of nonvolatile memories with a long latency, high dynamic strength, and short durability despite their low leakage power and outstanding scalability. The cell endurances of these RAM's are of the order of 10^8, 4 10^{12}, and 10^{11} write operations, respectively.

While PCM has a poor durability, in computing systems it has a better possibility of becoming the next generation of main memory due to its greater scalability qualities and decreased usage of energy attribute. The improvement of the PCM's endurance is well discussed in this article. In this article, we'll talk about how to improve the PCM's endurance. Any method for ensuring the efficiency of the main memory must be both energy and area appropriate.

By changing the state of the chalcogenide components, PCMs may store "0" and "1" values. When a high temperature is applied to chalcogenide above 600°C, it transforms into a liquid. It freezes into a glassy amorphous state form with significant electrical resistance after cooling. The chalcogenide must be heated to a temperature above its crystallization point to produce a low resistance condition, Formation of a hard defect in a cell's material as a result of continuous heating and cooling reduces the cell's lifetime.

Stuck on faults, stuck at logical a hard fault is denoted by the letters "1" or "0."Another form of defect that is soft errors is more common in DRAM-based memory. They're called transient faults since they're caused by colliding alpha particles.

Methods for addressing both hard and soft memory faults fall into three groups. The BCH code, which is based on the Hamming codes categorized in first group that are single and double error detection (SEC-DED). The amount of mistakes increases the amount of computations necessary for data encoding/decoding in ECC-based techniques, putting significant overheads on the system. The error correction pointer (ECP) methodology is used in the second category where redundant cells are utilized to replace faulty cells and is used to identify the location of the errors among the memory cells. This method, which is ideal for hard errors, and these have a significant area on high for keeping the pointers but can be used with other techniques that are fault-tolerant with small overhead. Clustering and re-grouping are used in methods like SAFER and RDIS to reduce ECP area overhead and to tolerate harsh faults. Third category falls where, data modification procedures (e.g., inverting data) are used to tolerate hard defects by using the "0" and "1" places.

To clarify these techniques, consider the two sorts of failures that cause the endurance problem caused by stuck-at faults:ST-R stands for Stuck at Right, and ST-W is for

Stuck at Wrong. The Stuck-at Right is represented by the symbol "ST-R", and Stuck-at Wrong is represented by the symbol"ST-W" and these symbols denote the value of the information to be put to the memory cell is equivalent to or not exactly the fault value. According to previous studies, by altering the data in memory blocks ST-R can be obtained with increase in number. A recently published solution for hiding severe fault faults in secure memory created fresh encrypted data by re-encrypting the input data. Another way for tolerating ST-W hard failures in SLC PCM memory is symbol-shifting, which inverts the recorded values.

As previously stated, Phase-change memory is seen as an alternative to Dynamic RAM. Secure data storage, on the contrary, is a problem on cloud servers. Many ways to increasing security at each memory hierarchy level has been introduced in recent years. The nonvolatile nature of PCM memories allows an attacker to gain unauthorized access to personal data even after the machine has been turned off. The data retention time of DRAM memories might be several seconds after the memory is turned off.PCM cells data retention time could be of many years after the machine has been turned off, providing a security risk for these memories. Data encryption is a well-known approach for preventing unwanted access to memory system data. The Advanced Encryption Standard (AES) defines encryption and decryption algorithms for encrypting (decrypting) data blocks before they are written to storage or read from memory. The main element of the AES algorithm is the avalanche effect, which produces a 50% toggling of the output bits when a bit in the input is flipped. This impact (using the AES algorithm on PCM) significantly reduces the PCM lifetime due to the encrypted memory has a high bit flip rate. To overcome this problem, techniques such as selective encryption have been devised. If the PCM cell's written value matches the cell's stuck-at-fault value for a read operation, the error correction unit does not need to fix this cell's error.

We show how to handle memory failures that are stuck-at in a simple and energy-efficient approach when data is encrypted and saved in the PCM main memory. In PCM, the distribution of stuck-at faults is random hence this helps in boosting "ST-R" in each cell by producing random values. As a result, we propose a shift operation-based method for meeting stuck-at faults by creating random values. The method proposed is called Rand Shift which belongs to a third type of hard-fault-mitigation strategy.

Fig. 1. Stuck-at Wrong and Stuck-at Right ideas are represented

A. Main Memory Security

Encrypting the information (data) saved in the memory cells of personal PCs and cloud servers to prevent the sensitive information from leaking is possible with the AES algorithm. The close upon algorithm used for data encryption in insecure memory is AES algorithm. This algorithm outperforms the previous symmetric encryption techniques when it comes to speed and power. The inputs to the AES can be 128-bit, 192-bit, and 256-bits. Based on the input bit length AES encrypts with 10, 12, and 14 rounds, respectively where each round includes high-energy tasks such as AddRoundKey, Substitute, Shift Rows, and MixColumn.The one-time pad (OTP) is a way for speeding up the encryption process while also increasing the security of the data being encrypted. The details of this technique's hardware implementation are presented to the left of Fig. architecture rand shift (OTP).The write operation is performed on the cache line, which is first XORed with the AES module's generated OTP before being placed in memory. The memory line is also XORed with the OTP before being sent to the final level cache for the read operation (LLC).This method, which is based on temporal and geographical variations, employs the line address and the cache counter to give a robust encryption scheme.

B. Phase change memory Main Memory Error Correction

The hard fault rate, which includes stuck-at faults, is at least ten times higher than the soft error rate, according to a study on PCM main memory. Many wear-leveling approaches had been suggested to delay the incidence of PCM memory cell defects. ECC is one of the most fundamental single-bit error correcting methods in memory. This type of Error correction is often employed in DRAM memory to fix parity calculation-based soft mistakes. While this is an excellent method for single-bit error correction, it isn't excellent for multi bit error correction in non-working PCM cells.ECP has been proposed for multi bit error correction applications. A pointer to ECP and one bit for its right value are present at each memory block's fault location. In a 512-bit block of memory with six faults, ECP results in an 11.9 percent area on high. To solve multi bit error correction, the SAFER approach recommended dividing the memory block into several groups, each having a single fault. As a result, it repaired each fault by the data inversion in order to raise the stuck-at right. To alleviate the hard fault, a symbol-shifting technique was developed for SLC single-level PCMs and MLC multilayer PCMs. To enhance the rate of "ST-R" values, this article shifts data in each MLC and inverts data in SLCs. RDIS locates a set of data bits that can be inverted that results in the greatest number of stuck-at Wrong "ST-W" situations. Following the discovery of this set, this set includes both "ST-W" and "NF" bits and is inverted for optimum hard fault coverage. The counter advance mechanism was developed in and resulted in an increase in the main memory of a secure PCM of the stuck-at Right "ST-R" level. The randomization function of AES encryption was employed

in this article to produce values for data blocks that were akin to stuck-at faults. It, re-encrypted AES using various counters to generate data in which part of the Bits ought to be stuck-at bits. When the number of stuck-at Wrong "ST-W" are zeros or the iteration number surpasses a predetermined with the maximum number of iterations, the data generation is ended.AES encryption is recalculated using the counter development process and with another counter worth with the memory block granularity level is The line level uses 512 bits, while the word level uses 128, 64, and 32 bits. As a result, despite the fact that this procedure is straightforward to implement, it wastes a significant amount of energy due to the large number of AES re-computations.

A simple and energy efficient Randshift approach is proposed in this article since the AES encryption is only recalculated once for each bit of information write to the PCM main memory.RandShift's fault coverage is nearly identical to that of the counter-offensive approach, but with substantial energy savings.

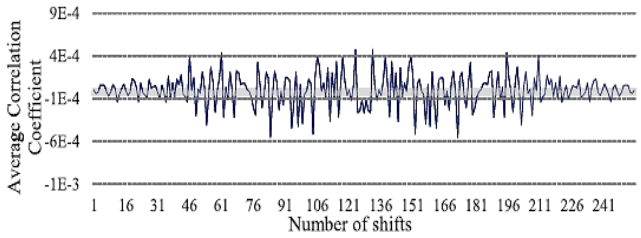

Fig. 2. The 50K 128-bit encrypted data's correlation coefficient.

II. LITERATURE SURVEY

The literature review focuses on AES, specifically how to apply it with low power consumption, good security, higher performance, and increased efficiency. The possibility of implementation in a VLSI context is also thoroughly investigated and examined. **Analysis of Faults in the AES-CBC Algorithm Space Applications Using Hamming Code Computer security was given by the National Institute of Standards and Technology in 2001.**The modes of operation for two specific block cypher algorithms have already been proven in two FIPS papers. With the Triple DES algorithm (TDEA) as the underlying block cipher, the mode's block cipher algorithm consists of two functions that are inverses of each other for each given key; four of these modes are equal to the ECB, CBC, CFB, and OFB modes.

Francois-Xavier Standard, Gael Rouvroy, Jean-Jacques Quisquater, and Jean-Didier Legat in 2004 described Rijndael Encryption on Reconfigurable Hardware: An Effic ient Implementation.It covered a variety of techniques for implementing, design of Advanced Encryption Standard for FPGA implementation. Several ways for implementing block ciphers can result in good designs. In order to create an efficient methodology, inherent limits of FPGAs were taken into account. For the substitute box, the authors developed algorithmic optimizations, as a well as effective combination of the main addition is the diffusion layer, within these structures. 25 Farhadian.A and Aref. M.R. (2009) developed an effective approach for simplifying and estimating s-boxes using power functions. The S-box configuration structure this investigation is vigorously dependent on figure calculations, power capacities over limited fields, and explicit reversal capacities. To grave break down such S-boxes, another orderly proficient strategy is given. This strategy is generally fundamental and doesn't need any heuristic endeavors; it tends to be utilized as a fast standard for finding basic approximations. Approximations for refined encryption principles (AES) like S-boxes, like AES, Camellia, and Shark, can be produced utilizing this novel strategy. At long last, a basic straight guess for the AES S-box is appeared as a utilization of this strategy.

III. RANDSHIFTMETHOD

As previously indicated few of the cell shave worn down and are permanently stuck at a "1" or "0" value due to the PCM's limited write endurance. The idea of fault coverage is illustrated in Fig. 1 by a memory word based on "ST-R" and "ST-W," where 4-bit places contain stuck-at faults, i.e. bit locations 0, 4, 10, and 13.Storing "0xB3A8" this term in memory as word, for example, results in ST-W at the 4th and 13th bits. In this situation, a 1-bit roundabout shift to the correct changes the worth to "0x59D4," results in stuck-at Right ST-R in the 4th and 13th bits but no additional ST-W.As previously established, any two AES encrypted data can be correlated and is nearly nil, as a result, the AES encryption's output can be considered an arbitrary integer. The normal relationship coefficient of AES-128 encryption for 50K 128-bit encrypted memory data in the "astar" test from CPU2006 is introduced in the presentation Fig. 2 [22].As seen in Figure 2, the displayed average is really close to zero which means that the output data in each iteration of the AES encryption algorithm is different has a low relationship. The AES's output value's unpredictability characteristic could be used as a way to accommodate stuck-at errors in PCM cells. However, due to the existence of spatial/temporal correlations among the data blocks, manipulation methods such as circular shifting or inversing may not be suitable for resolving the problem of stuck-at faults in the case of raw data that has not been encrypted.

The number of "ST-W" is 0 if the encrypted data does not entirely match the stuck-at faults, the encrypted data can be regenerated using the approach described in. As previously stated, this methodology is a power-hungry approach due to the likelihood of having to perform a significant number of regenerations. Each time the writing data and the stuck-at-fault values don't match foe which AES-128 adds twelve rounds of substitution, shift-Rows, and mix-Column to the mix. The number of "ST-R" in the case of a memory block with a small number of stuck-at fault bits are improved although the data reorganization strategy, in addition to the creation of new encrypted data, may not completely maintain the data's randomness. The former method is

obviously much faster and more energy efficient. Because the RandShift strategy is applied to encrypted data whose bits have a high degree of randomness, the disturbance in. The probability of the stuck-at fault coverage's of the suggested RandShift method and the one proposed in [12], which is referred to as ReGen in the rest of this study, should be compared to evaluate the efficacy of the two approaches. The ReGen technique [12] has no reliance in between the two previous and subsequent generation of data because of the randomized aspect of AES encryption. The RandShift method's data interdependence between the shifted bits makes it impossible to construct a formula with a close form to compute the fault coverage probability. As a result, we employed a simulation methodology to determine the suggested method's fault coverage probability. For the block length of 128 bits, in each row of PCM memory, there are one to six stuck-at faults. For varying iteration counts, Fig. 1 demonstrates the likelihood of matching with stuck-at faults for the RandShift and ReGen algorithms. This simulation utilizes memory data from the astar and Leslie3d benchmarks. As previously stated, the RandShift technique performs a circular shift to the right with each iteration, but the ReGen technique uses AES encryption and generates a new counter value to generate distinct encrypted data. One million encrypted data were used as stimuli to compute the RandShift and ReGen coverage probabilities. For the assumed distribution in this article, there are no more than six faults in 128 bits of data. The parameter Diff in Figure 3 is the average absolute difference between the two scenarios RandShift and ReGen.Diff is low (0.45%) for the provided number of faults and recurrences, showing that the proposed methodology is capable of tolerating about the same number of stuck-at faults. Figure 4 shows the pseudo code for the RandShift technique to allowing stuck-at faults to be tolerated. The memory controller encrypts data block lines 1 and 2 when the LLC makes a data write request. By storing and reading the pattern of all 1s and 0s in memory, the Row Verifier checks the value and location of the stuck-at faults [6]. 3rd line. After that, the RandShift function iterates until all stuck-at faults are concealed lines 4–13 or the number of iterations. Finally, if all faults are found to be identical, the data write operation will begin. A data write failure exception signal is generated if this is not the case sent (lines 14–19) to notify the processor, for example, of the write failure.

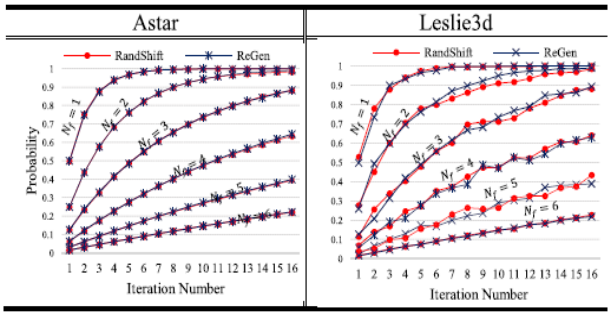

Fig. 3. Coverage probability of faults

```
1-  DB = Write request   -- (write-back 512 -bits  Data Block (DB) from
    LLC)
2-  DB = AES Encryption (DB)  -- (Encrypts DB with AES)
3-  {Fault Positions & Fault Values} = Row Verifier
4-  For i = 0 to NSh then   -- (NSh: The maximum number of shift
    operations)
5-  |   If (BD (Fault Position) == Fault Values (Fault Position)) then
6-  |   |       ShiftEnable = 0;
7-  |   |       Write Covering = 1;
8-  |   |       Break;
9-  |   Else
10- |   |       BarrelShiftCount++;
11- |   |       ShiftEnable = 1;
12- |   Endif;
13- End For;
14- If ( Write Covering == "1" ) then
15- |   Write is Done;
16- |   BarrelShiftCount = 0;
17- Else
18- |   Write is Failed;
19- End if;
```

Fig. 4. RandShift pseudo code.

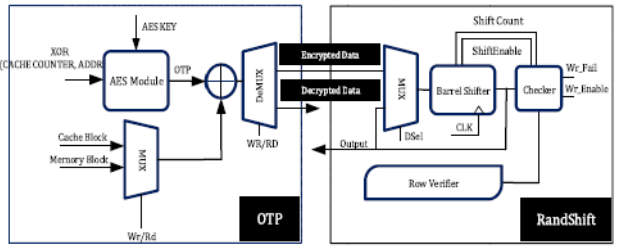

Fig. 5. Full architecture of RandShift.

A) RandShift Hardware Implementation

Implementation of hardware of the proposed RandShift architecture is shown in figure 3. The design includes three units Encrypt unit, Decrypt unit and the Shifter unit. At first the data is encrypted in the Encrypt/Decrypt unit using the OTP and is delivered to shifter unit. The Checker unit receives the position and value of the faults from the Row Verifier unit. The Checker unit verifies that the data bit values shifted and the fault values supplied by the Row Verifier are a same. The Shifter unit, which is a simple barrel shifter, is implemented by multiplexers. At the row or word level, the RandShift technique can be used. In this article, the data in a row of 512 bits is shifted entirely at the row level, whereas each word in a row of 64 or 128 bits is shifted separately at the word level.

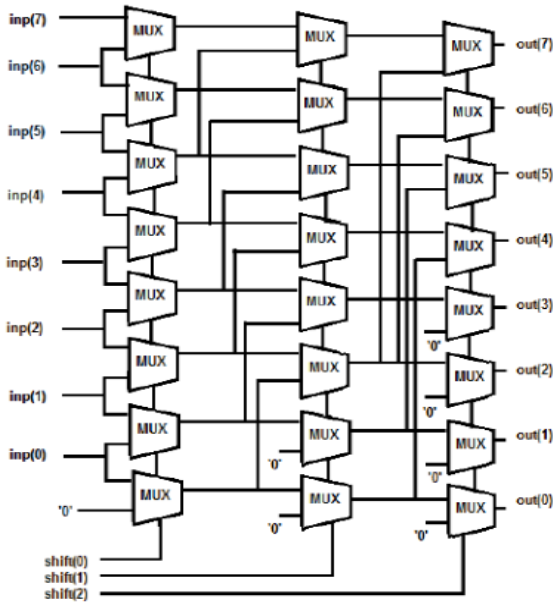

Fig. 6. Barrel Shifter design

Both general-purpose and embedded digital signal processors use barrel shifters to speed up data processing. It is basically a combinational circuit composed of multiplexers in which the signal travels through a fixed number of logic gates. A barrel shifter is a digital circuit that can change the number of bits in a data word in a single clock cycle. It may be very well executed as a progression of multiplexers, in which case the output of one multiplexer is associated with the contribution of the following multiplexer in a shift distance-subordinate way. A cascade of parallel 2:1 multiplexers is commonly used to create a barrel shifter. Consider an 8-bit barrel shifter with the following inputs: A,B,C,D,E,F,G,H. No bits are lost when the barrel shifter cycles the order of bits ABCDEFGH as HABCDEFG, GHABCDEF, and so on. A barrel shifter is essentially a shift register that rotates in bits. The bits that were moved out of the LSB end of the register are shifted back into the MSB end. For an n-bit word, the number of multiplexers required is n*log2 (n). The following are four common word sizes and the number of multiplexers required. As seen in Fig. 4, three layers, each containing eight 2:1 MUX, are required for an 8-bit barrel shifter. If input to barrel shifter is considered as j Input(j) with 8 bits the output is also j with the jth bit and shift(k) is the select input. The values of j and k are between 0 and 2.As the (i-1)th bit, the shift input is connected to the MUX's selection lines in the ith I = 1,2,3) layer. If (i-1)th bit is high, the layer offers a shift of 2i-1 bit positions. The initial two phases of the shift contribution of "100" pass contributions with no shift, while the third layer moves contribution by 4-bit positions. An 8-bit barrel shifter may move a word by 0-7 bit positions by integrating shifts in all three levels, with 0 being the simplest case. A barrel shifter, unlike a shift register, can perform a n bit position shift operation in a single cycle due to its combinational logic structure. These shifters are as of now being used in floating point add and subtract activities, which require suitable mantissa arrangement of the operands [1, 2]. This exploration investigates the thought of utilizing barrel shifters in multiplication when shifting is frequently fundamental.

B) Magnitude Comparator

Advanced Binary or digital comparators are comprised of ordinary AND, NOR, and NOT gates that think about computerized signals at their input terminals and give a yield dependent on the condition of those information sources. For instance, we should have the option to think about double numbers and choose whether the worth of input A is higher than, lower than, or equivalent to the worth of information B, in addition to other things. A Magnitude Comparator is an advanced comparator with three output terminals, one for every one of input, A is equivalent to B, A greater than B, and A less than B. The magnitude comparator can similarly be used to signal equality, but it includes two additional outputs: one for when word A is more than word B and another for when word A is smaller than word B.As a result, magnitude comparators are used to make decisions in logic circuits. Any logical problem can be reduced to a pair of compared values and one or more (often many) yes/no decisions. Figure 7 depicts a basic 1-bit magnitude comparator. Gate 1 generates the function A>B, gate 3 generates AB, and gate 2 is an XNOR gate that generates an equality output. Any number of bits can be added to this simple magnitude comparator circuit, but the more bits the circuit must compare, the more complicated it becomes. There are magnitude comparators built into integrated circuits that can be used to compare multi-bit words.

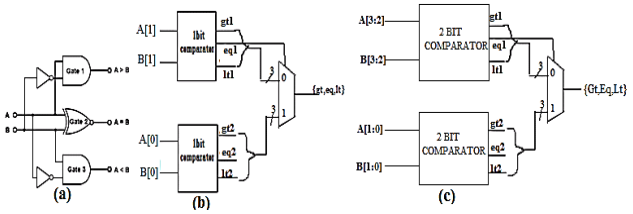

Fig7:(a) 1-Bit Magnitude Comparator,(b) 2-Bit Magnitude Comparator,(c) 4-Bit Magnitude Comparator

IV. RESULTS

RTL SCHEMATIC: The RTL schematic, also known as the register transfer level, denotes the architecture's blue print and is used to compare the designed architecture to the ideal architecture that we are working on. The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e, verilog, vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing. The figure represented below shows the RTL schematic diagram of the designed architecture.

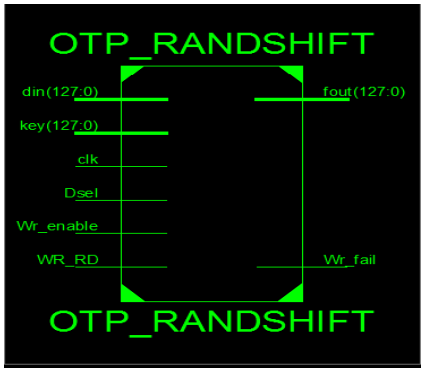

Fig 8:RTL Schematic of OTP Rand shift using magnitude comparator

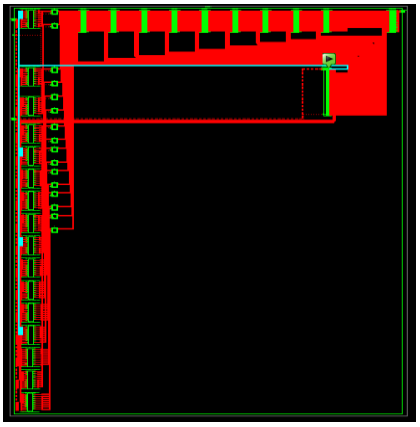

Fig9:View technology schematic of OTP Rand shift using magnitude comparator

TECHNOLOGY SCHEMATIC:-The architecture is represented in the LUT format by the technology schematic; the LUT is an area parameter that is used in VLSI to estimate the architecture design. The LUT is a square unit, and the FPGA's LUTs mirror the code's memory allocation.

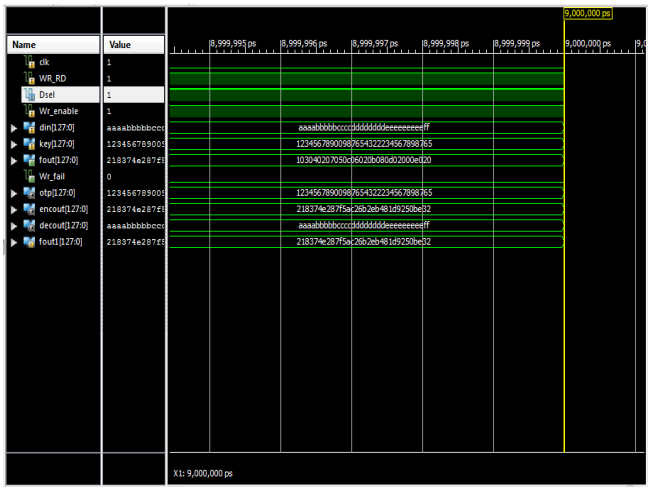

Fig10: Simulation Wave form of OTP Rand shift using magnitude comparator

SIMULATION:-

The simulation is the method that is used to verify the system's functionality, whereas the schematic is used to verify the connections and blocks. Switching from implantation to simulation on the tool's home screen opens the simulation window, and the simulation window limits the output to wave forms. It has the flexibility of provisos in this case.

Parameter	OTP Rand Shift By Digital Comparator	OTP Rand Shift By Magnitude Comparator
No of LUTs	21586	21519

Table1:LUT comparison table

PARAMETERS:-

The parameters are acquired by using the tool XILINX 14.5 and the HDL language is verilog language in this case. The parameters considered in this research for comparison area, delay, and power as in VLSI, these factors can be used to compare one architecture to another.

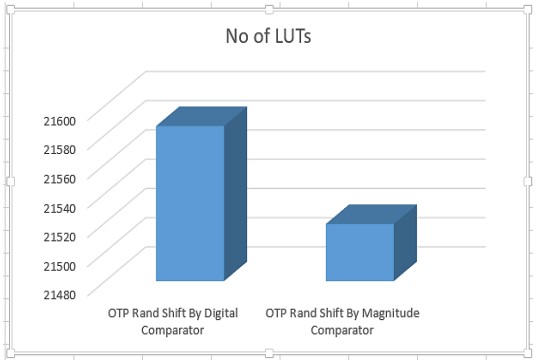

Fig 11: LUT comparison bar graph

V. CONCLUSION AND FUTURESCOPE

In this research, we present a method for tolerating severe failures in nonvolatile memory cells that combines with rotational shift operation; AES encryption has a randomization function. The RandShift approach benefited from its low energy consumption and easy hardware implementation. As the state-of-the-art methodology, it reduced the need to use ECC and ECP are powerful error correcting algorithms when almost the same fault coverage is observed. In this paper Proposed OTP rand shift using magnitude comparator it gave better improvement in area utilization and number of LUTs are consider as a area of design and the design was synthesized and simulated in Xilinx14.5ISE.In future this paper will be used in communication medium and cryptographic algorithms.

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15th-16th July, 2021 – Virtual Conference

A Novel VLSI Architecture of Truncation- And Rounding-Based Scalable Approximate Multiplier for High Speed Applications

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Abstract— Many effective structures are employed in the traditional designs so that the maximum speed can be included. Many of the structures will have multiplier as the basic blocks, these will run with low speed because of its huge structure. In practical, not all applications need accurate results as in digital signal processing and image processing etc. So approximate multipliers are employed. By considering these two points are scalable multiplier approximation, called as truncation- and also scalable rounding-based multiplier approximation (TOSAM) is represented. The suggested plan, multiply is done by change, addition, and lesser multiplication width fixed operation resultant in huge improved in the speed compared to those of the straight multiplier. For improving the entire accuracy, operands input of the multiplication slice are round to the nearby odd values. Why Because, the operand inputs are truncated, which is based on the leading 1-bit positions, the precision has become the weakly depends only on the size of the operand inputs and the multiplier will become scalable.

Keywords— configurable accuracy, Multiplier approximation, Speed is high, speculative inexact adder

I. INTRODUCTION

An important role play's by multiplier in today's DSP, and other applications. The DSP stands for Digital

Signal Processing .Digital signal processing is the brain of the system. Digital signal is nothing but processing of signals by means of a digital computer.

Here signal is nothing but the information is carried out by electromagnetic wave. Electromagnetic waves are used in wireless communication system. Here communication is nothing but the exchange of information between persons or systems with a proper medium, medium plays a major role in communication system. Very large scale integration is used for the purpose of reducing the size, and for low power consumption. We are having different types of technologies, like vlsi, they are, lsi , vlsi, ulsi.

The LSI stands for large scale integration, and ULSI stands for ultra large-scale integration. Depends upon the number of transistors used, the technology name will consider according to that. And these all are coming under in IC technology, IC stands for integrated circuit or integrated chip.

One of the complex design constraints in designing digital systems is power consumption. Digital systems will use digital values. The digital values are 0's and 1's.Approximate computing (AC) is one of the approaches which may be used for reducing energy usage and or increases the fast. Meanwhile the computing results are not correct, Approximate computing (AC) in error-resilient uses can be exploited. Image processing and audio machine learning, data mining.. Image processing is nothing but processing of images by means of digital. Further most specifically, in many applications like signal processing, the cause of arithmetic processes is a big portion of the energy consumption (e.g., up to almost seventy five percent of the full energy consumption is of FFT architecture).

The key contributions of the system are

1) Scalable approximate multiplier's new scheme.

For better improvement of the accuracy of the operation of multiplication It will discoveries the leading position 1 bit & truncation exploits and also rounding actions.

2) Finding a tradeoff b/w exactness, interval, and verve consumption truncation exploration and parameters h rounding.

3) For 2 operations that is, signed and unsigned operations presented. Implementation of h/w for truncation- and scalable rounding based estimated multiplier (TOSAM).

4) For the multiplier proposed for processing images and also for differentiation purpose applications design parameters are investigated.

II. II. LITERATURE SURVEY

For designing estimation multipliers the study efforts are reviewed. In this (segment method) DSM structure [1], operand inputs truncated by bits m. It is based on the place 1 bit wherever a multiplication fixed-width was executed by the truncated values. This is the way of truncation made and the produced o/p continuously less than the particular one, making the mean relative error (MRE) is -ve. Because of the fact that for the estimated arithmetic elements with the Gaussian distribution error was undesired, for having a higher S/N ratio whenever allocating with DSP'S uses [15].

III. PROPOSED APPROXIMATION FOR MULTIPLIER

A) TOSAM

Representation of +ve number integer (N)

$$N = \sum_{i=0}^{k} 2^i x_i \qquad (1)$$

In the above k indicates the leading position 1 bit and xi denotes the i th N bit. The factoring 2k from (1)

$$N = 2^k \left(\sum_{i=0}^{k} 2^{i-k} x_i \right) = 2^k \times X \qquad (2)$$

$$A \times B = 2^{k_A + k_B} \times X_A \times X_B. \qquad (3)$$

The widths of XA and XB are the equal as B and A creating the calculation of the precise value of XA × XB time and power consuming.

$$Y = X - 1. \qquad (4)$$

$$S = 2^h \qquad (5)$$

$$Y_{\mathrm{APX}} = \frac{2m-1}{2S} \quad \text{if } \frac{m-1}{S} \le Y < \frac{m}{S}, \quad m = 1, 2, \ldots, S. \qquad (6)$$

For better analysis purpose the estimated amounts of Y for the case in the above equation S is same to 4, is depicted in Fig. 1 Let us consider one example, whenever S = 4 (h =2), if two more noteworthy bits of Y are 0, it denotes as 0 ≤ Y < 1/4.

$$A \times B = 2^{k_A + k_B} \times (1 + Y_A + Y_B + Y_A \times Y_B). \qquad (7)$$

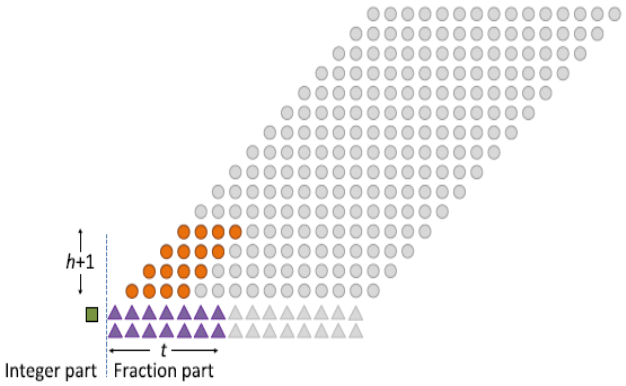

Fig. 1. Dot diagram of term.

1+(YA)t +(YB)t +(YA)APX×(YB)APX

APX from the above

t = 7 and h = 3.

Now, the approximation of (7) can be expressed by

$$A \times B \approx 2^{k_A + k_B} \times (1 + Y_A + Y_B + (Y_A)_{\mathrm{APX}} \times (Y_B)_{\mathrm{APX}}). \qquad (8)$$

For improving that only speed of calculation, here we truncate YA & YB to t bits, where in the last of this paper, we represent by (YA) t and (YB)t . Hence, we change (8) as

$$A \times B \approx (A \times B)_{\mathrm{APX}} = 2^{k_A + k_B} \times \begin{pmatrix} 1 + (Y_A)_t + (Y_B)_t + \\ (Y_A)_{\mathrm{APX}} \times (Y_B)_{\mathrm{APX}} \end{pmatrix} \qquad (9)$$

where the width of (YA)APX ((YB)APX) is h +1 bits.

Figure 2. Is a numeric example of 16-bit TOSAM(3, 7) with A = 11761 andB = 2482. The approximate result [(A × B)APX] is equal to 28 901 376 while the precise result [(A × B)Exact] is same to 29 190 802.

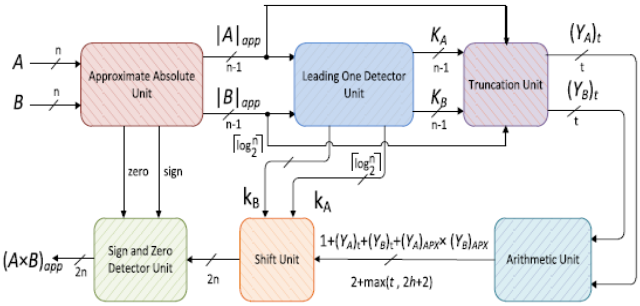

Fig. 2.Proposed approximate signed multiplier block diagram.

B) H/W IMPLEMENTATION

Fig. 3. shows the suggested signed estimated multiplier is depicted. In this unit, the bits of if the input is negative then the input are inverted and if the input is positive they are not reformed.

To the Leading-One Detector Unit |A|app and |B|app are injected and the places of their leading 1 bits are found using

$$K[i] = \left(\bigwedge_{j=i+1}^{n-2} \overline{I[j]} \right) \wedge I[i] \text{ for } 0 \le i \le n-2 \qquad (10)$$

In the above I can be either |A|app or |B|app. Revealing the position of the input leading one bit. Only one bit of the signal K is "1". kA and kB signals needed for (7) can be generated by using the KA and KB signals in a lookup table,

Fig. 4. Shows the schematic of the Leading-One Detector Unit for 8-bit input operands is depicted in let us consider one example, the |A|app = (011001)2, in this case KA = (010000)2 and kA = (100)2 = 4. Signals |A|app, |B|app, KA, and KB are applied to the Truncation Unit to produce (YA)t and also (YB)t .

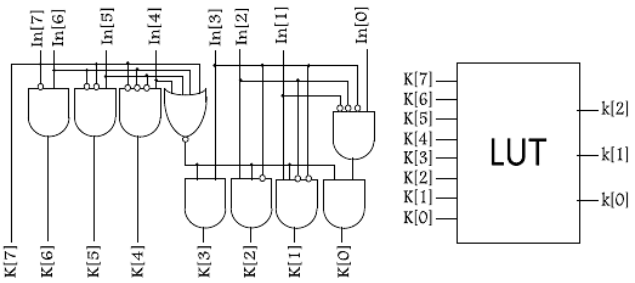

Fig.3. Schematic of the Leading-One Detector Unit for 8-bit input operands.

In this case, the i th bit of the output can be generated using

$$(Y)_t[i] = \bigvee_{j=0}^{n-2} (K[j] \wedge I[j+i-t]) \text{ for } i < t. \qquad (11)$$

4. Proposed Inexact Speculative Adder

For reducing area of multiplier in arithmetic unit inexact carry speculative adder was used instead of conventional carry skip adder. ALUs and DSPs broadly uses adders. These are the most complicated arithmetic circuits in digital electronics.

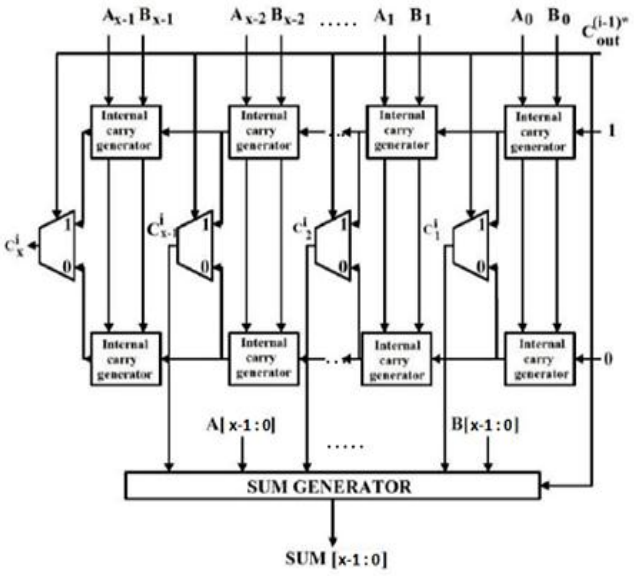

Fig 4: proposed inexact speculative adder

IV. RESULTS

RTL SCHEMATIC: - The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e verilog ,vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

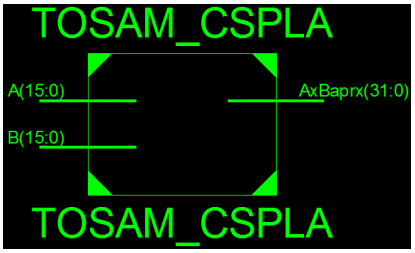

Fig 5: RTL schematic of proposed TOSAM

SCHEMATIC TECHNOLOGY

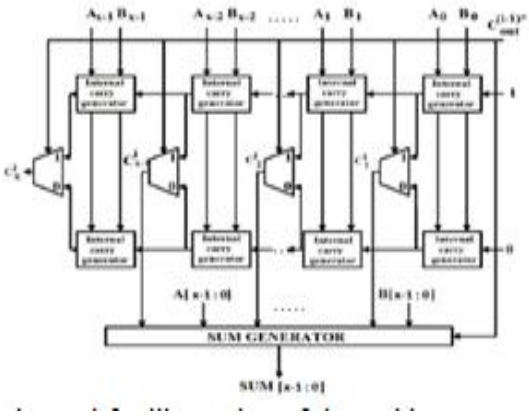

Fig 6: Schematic diagram of TOSAM

It is used for illustration of the architecture in the LUT format ,where the LUT is consider as the parameter of area that is used in VLSI for approximation the architecture design and the LUT is consider as an square unit the memory allocation of the code is represented in there LUT s in FPGA, where FPGA stands for field programmable gate arrays.

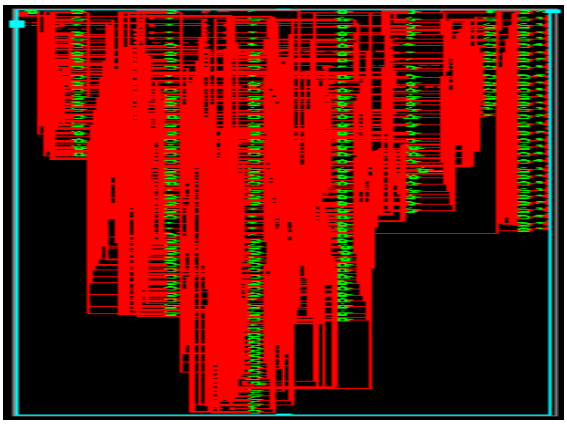

Fig7: view technology schematic of proposed TOSAM

SIMULATION:-

In the simulation process, on which, it is considered as the last confirmation in respect to its working where it is the schematic is the verification of the connections and blocks. As shifting from implantation and on the home screen of the apparatus the simulation window is launched, the simulation window confines the output in the form of the wave forms. Here it has the flexibility for providing the changed radix number systems.

Fig8.:Simulated waveforms of proposed TOSAM

PARAMETERS:-

Let us consider in VLSI (Very Large Scale Integration) the constraints preserved are region ,delay and power ,on these considerations one can judge the one architecture to the other. Here the consideration of delay is considered the parameters are obtained by using the tool XILINX 14.5 and the HDL language is verilog language.

Parameter	TOSAM_CSKA	TOSAM_CSPLA
No of LUTs	225	198

Table1: parameter comparison table

GRAPH:-

The graph is the pictorial representation of the represented data, which makes one to easily estimate the comparison. This graph is representing the comparison between two architectures delay and the scale is nano seconds.

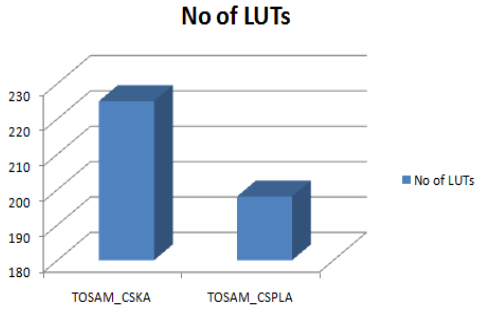

Fig9 : Delay comparison and lut comparision bar graph of TOSAM

V. CONCLUSION

The proposed design is developed and simulated using XILINX14.5 ISE, with verilog HDL language and the parameters are observed in vertex6 low power. This project presents high speed truncated and based rounding scalable approximate 16 x 16 multiplier design which is useful at floating point values. To achieve high speed, we using TOSAM algorithm.

A technique for computation which will incomes a possibly inaccurate outcome rather than a certain accurate outcome, and it can be used for applications wherever an estimated result is absolutely enough for its purpose the approximate computing. In the future these kinds of multipliers used in most of designs when accuracy is not a mandatory for example processing of image filters, cryptographic and etc.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

15th-16th July, 2021 – Virtual Conference

Synthesis and Elastic properties of Transition element doped $La_{0.67}Ba_{0.33}MnO_3$

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Abstract— Materials with the compositional formula $La_{0.67}Ba_{0.33}MnO_3$ and 5% Zn doped $La_{0.67}Ba_{0.33}MnO_3$ have been prepared by the conventional solid-state method. Structural analysis has been carried out by X-Ray diffraction (XRD) method. Rietveld analysis has been used to analyze the XRD data. The bulk densities (ρ) of the samples were measured using the immersion method and the X-ray densities (ρ_0) were calculated from lattice parameters. Later, the ultrasonic longitudinal (V_l) and shear (V_s) wave velocities were measured using 1MHz quartz transducers with the help of a pulse transmission technique. Using the ultrasonic velocity values, Young's and rigidity moduli along with Poisson's ratio and Debye temperatures were calculated. As the materials are porous, zero porous elastic moduli have been computed using Hasselmann and Fulrath model.

I. INTRODUCTION

Colossal magnetoresistance(CMR) is the sizeable drop in resistance observed in the proximity of Curie the temperature of materials, mainly transition metal oxides when they are subjected to a large applied magnetic field. The magnetoresistance of standard materials permits changes in resistance of up to 5%, but materials featuring CMR may demonstrate resistance changes by significant orders of magnitude[1] .These materials, known as manganites have the chemical formula $A_{1-x}B_xMnO_3$, where A and B are rare and alkaline earth ions, respectively. They exhibit not only CMR but also a variety of AFM, FM, orbital, and charge-ordered phases depending on temperature and doping. The CMR effect occurs when a magnetic field is applied near the Curie temperature Tc, which separates the high temperature paramagnetic (PM) phase from the low temperature ferromagnetic (FM) phase. Perovskite Mn oxides of type $La_{1-x}Ba_xMnO_3$ have attracted much attention because of a negative magnetoresistance effect observed near roomtemperature[2,3]. The sample $La_{0.67}Ba_{0.33}MnO_3$ crystallizes in perovskite Hexagonal crystal structure with *R-3c* space group4. The compounds $La_{1-x}Ba_xMnO_3$ show metallic conduction below the Curie temperature T_C. Near T_C, the applied dc magnetic field tends to align the local spin and suppresses the resistance greatly[4]. A large amount of experimental and theoretical work has been done to improve the magnetoresistance properties of these manganese oxides[4,5,6]. Transition element doped CMR materials also well studied in the literature7. However, up till now most research works about $La_{1-x}Ba_xMnO_3$ have been concentrated on the magnetic, electrical and dc resistance dependence on the magnetic field. Et Al Sotirova[8], studied the effect of Zinc doping on the structure, transport, and magnetic properties of $La_{0.7}Sr_{0.3}Mn_{1-x}Zn_xO_3$ manganites and they found that there is a decrease in the insulator to the metal transition temperature, with increasing the zinc concentration on the Mn site, while the resistivity values were found to increase with the increase in the zinc doping level for $0<x<0.1$. In addition to the electrical and magnetic properties of CMR materials, a study of the elastic behaviour is also important to study the inter atomic and inter-ionic forces in them. Moreover, anon-destructive technique like ultrasonic velocity measurements is a very sensitive tool not only for studying the defects of microscopic processes in solids but also successful in monitoring systems undergoing magnetic and structural phase transitions. Therefore, in the present investigation, elastic properties of $La_{0.67}Ba_{0.33}MnO_3$ (LBMO) and Zn doped LBMO have been studied and the results are presented here.

II. EXPERIMENTAL

The polycrystalline $La_{0.67}Ba_{0.33}MnO_3$ and $La_{0.67}Ba_{0.33}Mn_{0.95}Zn_{0.05}O_3$ CMR manganites were prepared by solid state reaction method using C_3H_6O (acetone) as grinding medium. Mixed powders of La_2O_3, MnO_2 and $BaCO_3$ taken in the stoichiometric ratio were ground for 4 hours in an agate mortar and then calcined at 750°C for 3 hours. Subsequently, the calcined samples were ground for 2 hours to get the homogeneity. The powders were compacted into disc-shaped pellet form with a hydraulic press and the pellets were sintered at 1250 °C for 6 hours. Powder X-ray diffraction (XRD) technique was used to characterize the structure of the samples, using a Bruker D8 advanced Diffractometer equipped with Cu-Kα radiation (λ=1.54068 Å) source. The XRD data were analyzed using the Rietveld refinement technique and Fullprof software. The bulk densities (ρ) of the samples were also measured using the Immersion method[9]. Ultimately, the elastic moduli were calculated by a pulse transmission method called Ultrasonic Velocity Test. A pulse generator set up

along with a built-in amplifier, RPR-4000 (RITEC INC., USA) was used. X- and Y-cut (1MHz) quartz transducers were used for the generation and detection of ultrasonic longitudinal and shear wave pulses respectively. The overall accuracy of these measurements is about 2 m/sec in velocity values and about 0.5% in elastic moduli.

III. RESULTS AND DISCUSSIONS

3.1 Structural characterization:

The samples were characterized structurally by XRD studies and the results are shown in figure1(a). From the graph it is determined that the peaks are sharp, indicating that the samples were crystalline. It can be said that increase in Zn doping could improve the crystallization of the sample[10]. The absence of impurity peaks in XRD results indicates that they are a single phase. The samples are crystallized in a hexagonal structure with *R-3c* space group. The crystalline size of the samples was calculated using Scherrer's formula and all the samples were found to have crystallite size in the range of 70-100 nm. The unit cell volume increases with an increase in Zn concentration, since the ionic radius of Zn^{2+} is larger than that of Mn^{3+}, so it can be said that Zn substitution can make the volume larger[10]. Rietveld refinement technique using Fullprof software was used to investigate whether doping of transition metals caused any structural changes among the compounds. For calculating lattice parameters, it was assumed that all the samples are of Hexagonal structure with *R*-3*c* space group. The Pseudo-Voigt function was used to fit the peak profiles in X, Y Sigma format. The background model used was 6 coefficient polynomial functions with the origin of the polynomial at 40. Refinement was carried out for 10 cycles with reflections ordering at each cycle. The refined structure of the pure LBMO samples is shown in Figure 1(b). The lattice parameters of the samples obtained from refinement were tabulated in Table.1 and the values are in good agreement with the literature[11]. It can also be observed that the samples residual factors such as R_P, R_{WP}, R_{exp} and goodness of fit values confirm that the refinements are acceptable and the compositions are up to the stoichiometry. It can be seen from the table 1 that the lattice parameters are found to increase slightly with the doping of Zn and it is due to the large ionic radius of Zn^{2+} than that of Mn^{3+}.

3.2 Density Studies:

Bulk densities of the samples have been determined with the help of the immersion method using xylene as buoyant. For performing it, initially, the weight of the sample in the air was measured and taken as *D*. The weight *I* was measured after suspending the sample in Xylene. It was then placed in a vacuum chamber and a vacuum pump was used to remove any pores in the Xylene immersed sample. The new weight was measured and taken as *S*. Using these parameters the density of the sample was calculated using the relation, $\rho = D \times \rho_{xylene} / (S\text{-}I)$. The bulk densities were calculated, given in Table.2 and were found to be 5666 Kg/m^3 for a pure sample and 5670 Kg/m^3 for Zn doped sample. The X-ray densities also calculated by using the formula ZM/VN where Z is the number of atoms in the unit cell (here Z=6), M is the molecular weight of the compound; V is the volume of if the unit cell and N is Avogadro number. The calculated X-ray densities are given in Table 2. The porosities of the samples were calculated from the formula

$$P = [1 - \frac{\rho_{bulk}}{\rho_{X-ray}}] \times 100.$$

The obtained values are given in Table 2. It can be seen from the table that the porosity of the samples is 16-17%. The advantage of having porosity is relieving of the internal stresses which results in getting less constrained samples. This may be due to the fact that the stresses were generated during the sintering. Therefore, it is clear that porosity plays an important role as far as the mechanical properties are concerned.

3.3 Ultrasonic velocity studies:

The ultrasonic longitudinal (V_l) and shear wave velocities (V_s) of all the samples of the present investigation were measured using pulse transmission technique and with the help of X- cut and Y- cut quartz transducers and the velocity values are presented in Table 3. With the help of longitudinal and shear wave velocities, Poisson's ratio (σ) values of all the samples were calculated using equation(1) and are given in Table 4.

$$\sigma = \frac{V_l^2 - 2V_s^2}{2(V_l^2 - V_s^2)} \quad (1)$$

The Poisson's ratio values measured were found to be in the range 0.134-0.140. Finally, the elastic constants, Young's modulus (E) and rigidity modulus (G) were also calculated using the well- known equations[12] given below.

Rigidity modulus: $G = \rho V_s^2$

Bulk modulus: $B = \frac{2G(1+\sigma)}{3(1-2\sigma)}$

Young's modulus: $E = (1 + \sigma)2G$

The obtained values are given in Table 4 and are in good agreement with the literature[5].

3.4 Porosity correction:

The elastic moduli depend on the porosity of the samples; the experimental elasticity values do not have any significance unless they are corrected to zero porosity. As the samples of the present investigation are porous, it is essential to make porosity corrections to the elastic moduli values. For this purpose, Hasselman and Fulrath model has been adopted. In this model, it was assumed that the samples prepared by ceramic process (sintered) contain mainly spherical type of pores, the Young's and shear wave moduli may be given by:

$$E_0 = \frac{E}{1-\alpha_E P}\ ; where\ \alpha_E = \frac{3(9+5\sigma)(1-\sigma)}{2(7-5\sigma)} \quad (2)$$

$$G_0 = \frac{G}{1-\alpha_G P}\ ; where\ \alpha_G = \frac{15(1-\sigma)}{(7-5\sigma)} \quad (3)$$

where E_O and G_O are the Young's and rigidity moduli of non-porous matrix respectively, while E and G are the experimental values of Young's and rigidity moduli respectively, and P is porosity of the material. By using equations 2 and 3, porosity corrections have been made for the experimental elastic moduli and are the zero porous values are given in Table.4.

3.5Acoustic Debye temperature (θ_D) and mean sound velocity (V_m) :

The Debye temperature, Θ_D is the temperature of a crystal's highest normal mode of vibration i.e , the highest temperature that can be reached due to a single normal vibration. It characterizes numerous properties of solids such as thermal expansion, thermal conductivity, specific heat, and lattice enthalpy .Therefore, Debye temperatures of all the samples were calculated using Anderson's relation[13].

$$\text{Debye temperature: } \theta_D = \frac{h}{k}\left[\frac{3N_A}{4\pi V_A}\right]^{\frac{1}{3}}.V_m \qquad (4)$$

where h and k are Planck's and Boltzmann's constants respectively, N_A is the Avogadro's number and V_A is the mean atomic volume given by $(M/\rho)/q$, where M is the molecular weight and q is the number of atoms in the formula unit and V_m is the mean sound velocity, which is calculated using the formula.

$$\text{Mean sound velocity: } V_m = \left[\frac{3(V_l^3.V_s^3)}{(V_s^3+2V_l^3)}\right]^{\frac{1}{3}} \qquad (5)$$

The Debye temperature (θ_D) of all the samples calculated using equation (4) is given in Table.4. From the table, it is clear that θ_D values are found to be decreasing with the decrease of the ionic radius of Zn. From equation 4, it is clear that the Debye temperature depends on mean atomic weight (M), density (ρ), and its average sound velocity (V_m).In general, the elastic behavior of oxide materials can be interpreted in terms of binding forces between various ions. According to Wooster[14], the elastic moduli of a material system can increase or decrease continuously with increasing dopant concentration, depending upon the effect of dopant ion on the binding forces. In the present investigation, with the doping of Zn, the elastic properties were found to decrease and it may be due to the binding forces between various ions of these materials might be decreasing. Further studies are needed to understand the complete behaviour of the samples of the present investigation.

IV. CONCLUSIONS:

Single phase LBMO and Zn doped LBMO have been prepared through the sol-gel method and the lattice parameters found to increase slightly with Zn doping. Bulk and X-ray densities were calculated and there was no much change with the doping of Zn. But there was a drastic decrement in the elastic constants with the Zn doping. It may be attributed to the decrease in binding forces between the various ions.

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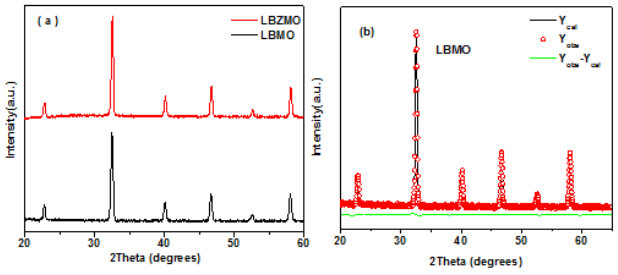

Figure 1. (a) X-Ray diffraction patterns of LBMO and Zn doped LBMO. (b) Rietveld refinement profile of LBMO.

Table 1. Crystallographic data

Sample	a=b (Å)	c (Å)	R_P	R_{WP}	R_{EXP}	S (goodness of fit)
LBMO	5.51	13.44	38.2	16.3	13.66	1.42
LBMZO	5.52	13.46	39.4	17.0	13.32	1.63

Table 2. Crystalline Size (Using Scherrer Formula) and Porosity Data

Sample	β (FWHM)	2θ	D(Crystallite size) (Å)	Bulk density (Kg/m^3)	X-Ray Density (Kg/m^3)	Porosity %
LBMO	0.352	32.50	4.10	5666	6800	16.67
LBMZO	0.322	32.55	4.47	5670	6830	17.00

Table 3. Ultrasonic velocities & attenuation values (at 1MHZ)

Sample	V_l (m/sec)	V_s (m/sec)
LBMO	3125	1910
LBMZO	2190	1346

Table 4. Experimental elastic data corrected to zero porosity along with Poisson's ratio

Sample	E (G Pa) 1 MHz	G (G Pa) 1 MHz	σ 1 MHz	E_0 (G Pa) 1 MHz	G_0 (G Pa) 1 MHz	θ_D 1 MHz
LBMO	49.68	20.67	0.20	74.53	31	259.3
LBMZO	24.58	10.27	0.19	37.22	15.5	175.1

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A Cascaded Deep Network Architecture for Multi Modal Biometric Recognition

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Abstract— It is very often to see that the results obtained from a uni-modal biometric system have negative results when the input subject is deteriorated or damaged. To provide more accurate and high security with biometrics, researchers have integrated the unique feature of more than one biometric system resulting in multi modal system. Face and Iris recognition systems yield higher precision and observed to be robust against tampering because of the unique features that are extracted for classification. In recent times, deep learning has gained a lot of importance in computer vision application especially for image classification with high accuracy and similarity index. Multiple layers of convolution operation are performed on the spatial elements of image, extracting the finer details pertaining to it. This makes the deep network more suitable for solving classification problem. This paper presents a cascaded customized deep network architecture that aims to merge the classification scores of multiple biometrics to attain more robust recognition system that is invariant to illumination. The proposed approach is tested and evaluated with two standard datasets and metrical analysis is compared against state of art methods.

Index Terms—Deep Networks, Multi- Modal biometric system, Classification, Score based fusion.

I. INTRODUCTION

An individual can be recognized based on the unique attributes that were extracted from any physical property of the person, these attributes are termed as patterns that are the key elements of any biometric recognition system [1]. These biometric systems provide reliable and sustainable solution for identifying an individual, due to this these systems are adopted in many of access controls in many of high security private and government organizations. The anatomical characters include face, finger, Palm, Iris and skin which are treated as physiological traits that were employed in most of the biometric systems.

In general, any biometric recognition system refers to single information which is termed as Unimodal systems which are cost effective, simpler, however some of these unimodal systems are non-reliable and sometimes the output of these systems are wrong when the inputs are deteriorated. In order, to overcome these shortcomings of the traditional unimodal systems novel multi-modal systems are introduced which are dependent on multiple input data [2]. These multi-modal systems have multiple merits like (i) Low error rate (ii) Availability (iii) Higher degree of freedom (iv) robust against attacks [3].

To merge the decision from multiple modalities a score base fusion approach has to be employed for attaining final classification result. This fusion process plays a vital role in deciding the overall performance of the multi-modality system. This integration process can be performed at different levels like at sensor level [4], feature-level [5][6], score level [7] and decision level [8]. The fusion at sensor level is not preferable as it may cause more redundancy, feature level fusion is sufficient to identify an individual more accurately however its practical implementation is too tricky since the sources from multiple inputs may be non-compatible [9]. In the recent times, the rank based fusion process has attained high interest due to easiness of integration that concentrates in identifying the individual. Due to the limited source of information, the decision based fusion process it too rigid. But the score level fusion process finds more attractive due to the simplicity and the outcomes of the fusion process is accurate. This process doesn't include complex redundant data with optimum information needed for attaining high recognition. This paper presents, an effective way of integrating score based fusion process for multi- modal biometric system. The scores were attained from two different customized deep networks that were designed for classifying different biometric modalities. The paper is organized as follows, section I presents the introduction, need and importance of multi-modal systems. Section 2, presents the related work pertaining the present context of implementation. Section 3 presents, proposed approach of score based fusion process with experimental results that were presented in section 4 and conclusion remarks in section 5.

II. RELATED WORK

This section presents a brief literature on related works that were conducted by several researchers earlier and that related to preset context of work. In [10] authors have discussed about a combinational fusion approach that are relied on dynamic features and scores that are obtained from the classifiers of face and Iris modal systems. These features are combined together in an algorithmic fashion where an optimal threshold is used as a thumb rule for integration. It was presented that this approach attains higher accuracy and likely to be robust against noise attack.

In other work presented by Huo and others [11] where a Gabor filter bank features were employed to fuse the multi modal systems. In this work, the features were extracted using Gabor filters with varying angle and scale factors for Face and Iris Images and later histogram statistics were used to convert them into orientation features that are low dimensional and possess the attribute of high differentiability. PCA (Principle Component Analysis) and SVM (Support Vector Machines) were employed to reduce the dimensionality and classify the features at faster rates.

Texture based multi modal system was proposed by Basma et.al [12], in their work Log Gabor filters were employed to extract the features and combines Spectral regression with kernel based discriminant system. These features are extracted for Face and Iris modal systems and attained an average classification accuracy of 90.75 percent. A new deep learning based approach was proposed by Veeru et.al [13], in this work the authors have included Forward error codes to minimize the false positives and converted a Pseudo feature space of features that were extracted with CNN (Convolutional Neural Network) are integrated using joint representation layer. Finally, the sorted features are selected who dimensionality is reduced, this later creates a binary template which is obtained with distance transform for error correcting codes. In this work the authors have employed Reed Solomon Codes for FEC and pass the generated template through an appropriate decoder which is closest code word which is later forwarded to final template.

Barni et.al [14], have presented a secure and effective multi modal system that aimed to increase the efficiency of the multi modal system by operating them with encrypted codes. Xu et.al [15] have proposed a 3-modality based biometric system with deep learning mechanism. In this work the authors have developed a customized CNN structure for each uni-modal system and later they have integrated them in algorithmic fashion. The work presented in this paper is adapted from the works of Xu. With this multi-modality architecture, the authors have attained an average classification accuracy of 98.5 percent however the approach is tricky and consumes lot of time. So in this work, these two factors are concentrated where the present works aims to design and develop a new architecture and integration process which is simple, faster and yields higher classification rate. Few more networks were presented in [16] [17] that aims to fuse Face, speech and Iris modalities.

III. FACE-IRIS MULTI-MODAL SYSTEM

In this work two modalities like Face and Iris are considered for implementing the proposed score based fusion process. These modalities are very often used in many access control and authentications systems (Eg: Adhaar –Indian Unique Identification System). These modalities are chosen because of the reliability, uniqueness and robust against tampering.

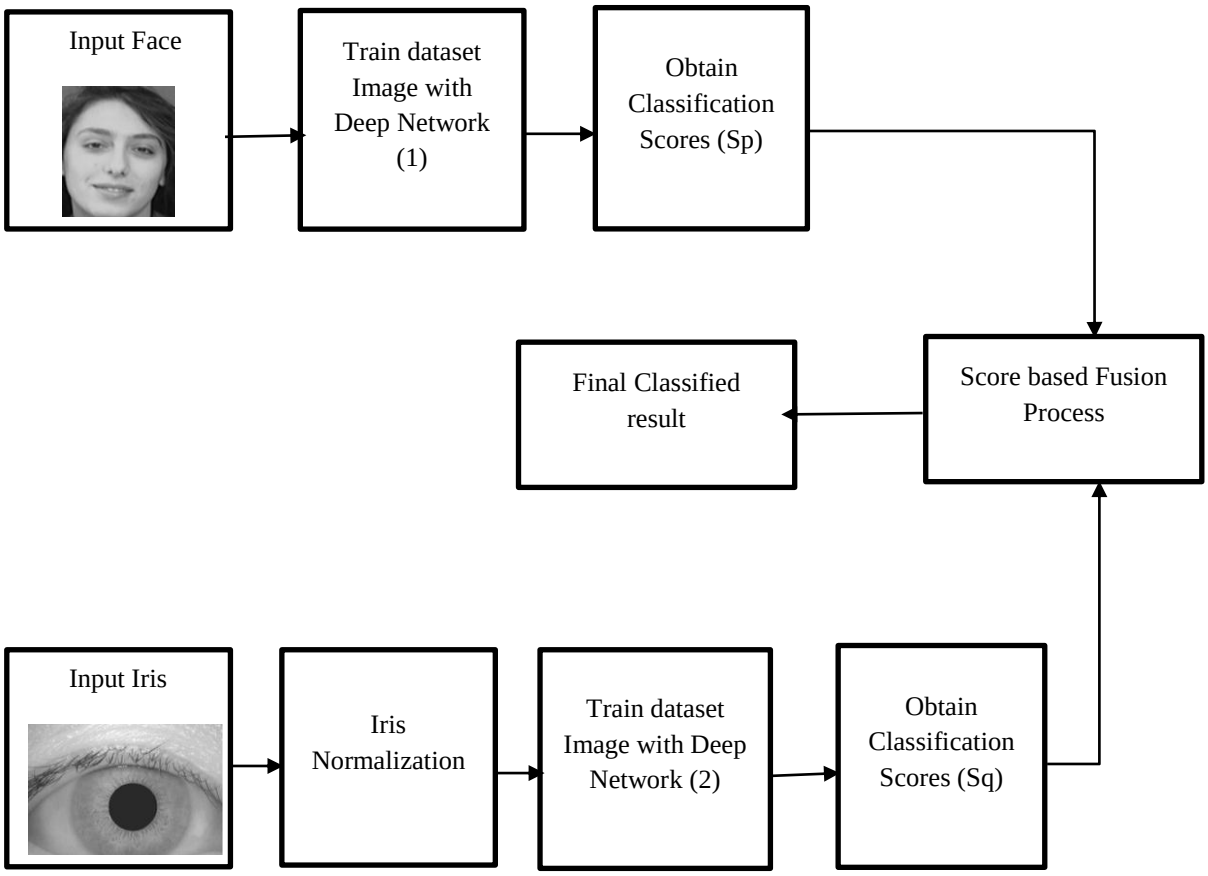


Figure 1: Proposed Score based fusion process block diagram

The proposed approach block diagram is depicted below in figure 1. The proposed approach takes the inputs from two acquisition blocks each for one individual modality. The face images were considered from ORL face data set where each sample is of dimensions 112x92 gray scale images that are translated and have two categories like "with gasses" and "without glasses".

To increase the number of samples, first the images are rotated and scaled with constants such that for each single image we obtain 12 samples. In similar fashion the Iris images were taken from CASIA V1.0 dataset which are gray scale images with 256x256 dimensions. Same as in the case of face images, the Iris images are also rotated and scaled so that we obtain more number of samples for training the Deep network.

Unlike Face images, the Iris images are pre-processed to extract the Iris localized region from the total Eye image. In order to accomplish this activity, we have processed the images with Daughman's rubber sheet model for localizing and extracting the Iris regions [19]. In the present work an integro-differential operator is employed to partition the eye regions.

Thus, obtained segmented portions of Eye images that contain only Iris regions are processed to deep network for training. In parallel to this, face images are processed for other network. So, in total there will be two networks which are custom designed for two modalities The specifications of the networks are given in table 1 and table 2

Table 1: Network specifications for Face Network

Input Image size	112x92x1
2D-Convolutional Layer	5x5x1-920
Max pooling	2x2 with stride factor 2
Fully Connected	7
Softmax Output	Cross Entropy

Table 2: Network specifications for Iris Network

Input Image size	256x256
2D Convolutional Layer	7x7x1-920
Max pooling	2x2 with stride factor 2
Fully Connected	7
Softmax Output	Cross Entropy

The proposed network can be represented pictorially as shown is figure 2. In this network, it consists of 2-convolutional layers each of size 5x5 with 20 filters with stride factor of 1. Max pooling is employed at pooling stage with stride factor of 2. At the end, a fully connected layer of size 7 is employed that aims to classify the subjects with cross entropy classification. Finally, the feature vector is passed to neuron in fully connected layer that produces a k-dimensional vector s = (s1, s2, .., sk) representing class scores towards 'k' subjects.

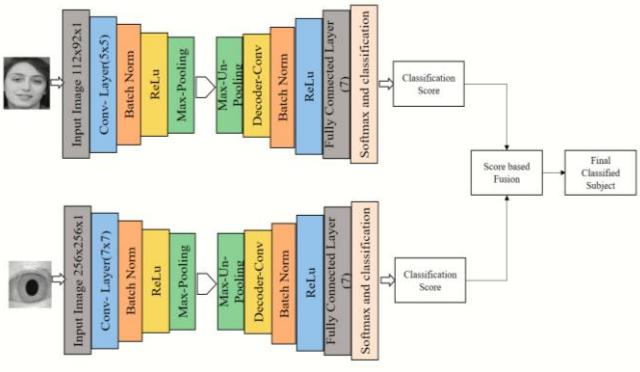


Figure 2: Proposed approach of the network architecture

The proposed score based fusion process is applied to the outcomes of both the networks. It was observed that in many of the cases the scores obtained from individual classifiers are not homogeneous and follow different distribution that may not fall into the same interval [20]-[22]. Let us consider the scores obtained from face network are termed as F(p) and from Iris network as I(q) for the p^{th} and q^{th} subject. The rank of all confidence of all individual scores are calclulated with the following euqation

$$A(k)_{p,q} = \frac{|s_{p,q}(k) - \delta(q)|}{\delta(q)} \quad (1)$$

In the above equation (1),'k' is number of modalities in this analysis k=2 (Iris, Face), the parameters correspond to p^{th} subject of the q^{th} sample and 'S' corresponds to individual classifier raw score. In brief, if there are 7 subjects each of 12 samples then total number of scores are 84. In the above equation the regularization parameter 'δ' termed as mean-to-overlap extrema-based anchor. The aim of this parameter is to focus on the overlap scores and its neighbours in both the modalities which is given as

$$\delta(q) = \{\max\big(F(p)\big) - mean(F(p)\} + \{mean\big(I(q)\big) - \min\big(I(q)\big)\} \quad (2)$$

Where "F" stands for face score and "I" stands for Iris score.

From the above equation (1) the normalized factor is calculated

$$N(k) = 1 - \frac{A(k)}{\sum_{k=1}^{m} A(k)} \quad (3)$$

The fusion score (F) is obtained sum product rule as given in equation (4)

$$F = \sum_{k=1}^{m} N(k) * s_{p,q}(k)/m \quad (4)$$

In the above equation 'm' is temporary variable where m=2. Clear numerical analysis in given in the next section.

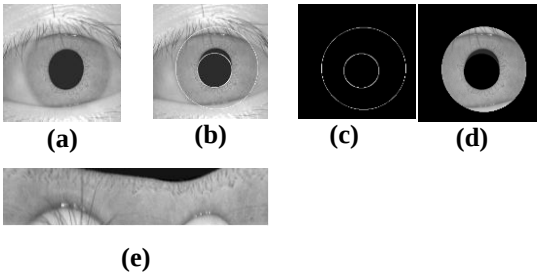
IV. EXPERIMENTAL RESULTS

The experiments of this work were conducted in ORL Face dataset [23], CASIA Iris Dataset (V1.0) [24]. Total 40 out of which 7 subjects were presented with 3 rotation and 3

scaling transformations which are considered for training the network. The Face image is of resolution 112x92 and Iris image dimensions are set to 256x256 gray scale 8-bit.

(a1) (b1) (c1)

Figure 3: a1 Original Image b1 Rotated Image c1: Scaled Images; the images are augmented and used for training the network



(a) (b) (c) (d) (e)

Figure 4: (a) Original Image (b) Iris Marked using Daughman algorithm (c) Marking or region (d) Extracted Region (e) Normalized Image

For the experimental analysis a confusion matrix was constructed based on the scores of the network.

Table 3: Confusion Matrix of scores ($s_{p,q}$) for k=1 (Face)

Target (col)/ Predicted score (row)	P1	P2	P3	P4	P5	P6	P7
P1	1	0	0	0	3.49e-13	0	0
P2	4.06e-13	1	0	0	0	3.58e-14	0
P3	0	0	1	2.28e-14	1.22e-21	0	1.46e-12
P4	6.06e-24	0	0	1	4.15e-19	1.69e-13	2.37e-20
P5	1.84e-16	0	7.39e-14	2.9e-24	1	0	2.46e-24
P6	0	2.31e-13	0	3.09e-14	0	1	8.8e-24
P7	0	0	0	0	0	2.10e-14	1

Table 4: Confusion Matrix of scores ($s_{p,q}$) for k=2 (Iris)

Target (col)/ Predicted score (row)	P1	P2	P3	P4	P5	P6	P7
P1	1	1.41e-16	3.7e-32	2.8e-2	5.3e-19	0	9.8e-35
P2	2.32e-28	1	6.51e-24	0	0	0	9.9e-25
P3	0	0	1	0	1.71e-23	0	0
P4	4.09e-13	0	3.93e-30	1	8.3e-27	0	9.42e-12
P5	1.01e-32	0	9.18e-36	0	1	0	0
P6	6.81e-25	6.91e-41	4.12e-17	48e-34	0	1	9.21e-30
P7	0.0027	1.21e-14	1.48e-8	0.0012	2.46e-5	1.047e-8	0.996

From the above two tables calculate the alpha value. In our experiments alp values are $\alpha = \{1.004, 1,11,1,1,1,.98,1\}$

Table 5: Confusion Matrix of Fusion scores with Proposed Weighted Normalization

Person/W	P1	P2	P3	P4	P5	P6	P7
P1	0.9997	0	0	0.0129	0	0	0
P2	0	1	0	0	0	0	0
P3	0	0	1	0	0	0	0
P4	0	0	0	1	0	0	0
P5	0	0	0	0	1	0	0
P6	0	0	0	0	0	1	0
P7	0	0	0	0	0	0	1

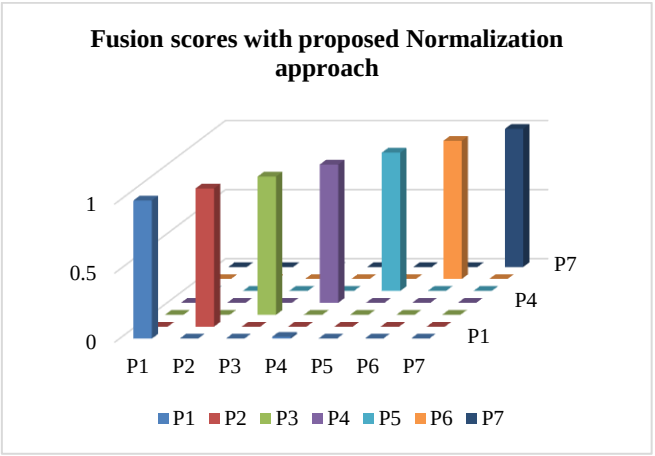


Figure 5: Graphical representation of the proposed weighted Normalization Matrix

The proposed face biometric recognition is compared against face recognition of Huo's method [11] and found that it yields ~98% accuracy which is about 1~1.5% low than the proposed approach.

Table 6: Performance of recognition rates for unimodal and proposed multi modal methods under different geometric transformation

Method/Transformation	Face –Unimodal		Iris-Unimodal		Multi Modal	
	Trained	Untrained	Trained	Untrained	Trained	Untrained
Normal	1	0.9762	1	0.97	1	0.97
Scaled (70%)	0.897	0.7142	1	0.92	0.945	0.89
Flipped	1	0.8810	0.9821	0.89	0.985	0.9
Average	0.965	0.857	**0.99**	0.92	0.976	**0.92**

Table 7: Performance of correct recognition rates for proposed and Huo's multi modal

Method/Transformation	Multi Modal [11]		Multi Modal (proposed)	
	Trained	Untrained	Trained	Untrained
CRR	0.983	0.91	1	0.97

Table 8: Performance of correct recognition rates (CRR) for proposed and Huo's multi modal under different geometric attacks

Method/Transformation	Multi Modal [11]	Multi Modal (Proposed)
Under Illumination scaled to 80%	96.6%	98.5%
Under Gaussian noise of density 10	88.4%	90.2%
Under JPEG compression with quality factor of 30	89.8%	99.05%

Table 9: Performance of CRR of proposed approach and unimodal recognition systems

	Unimodal Modal – Face-ORL	Unimodal-Iris CASIA V 1.0	Multimodal
CRR	99.05%	99.10%	99.25%

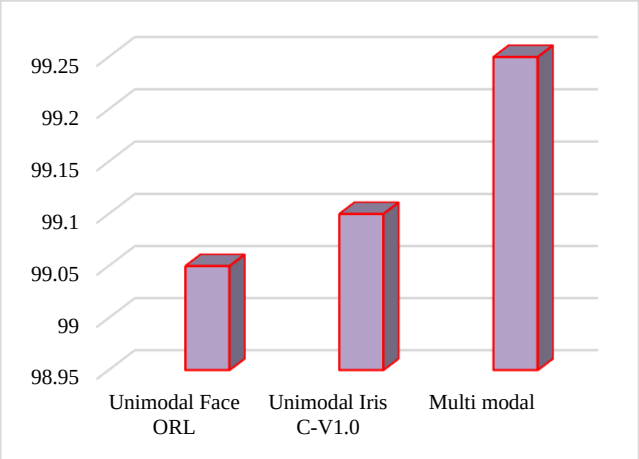


Figure 6: CRR performance comparison for proposed and Unimodal methods

From the results it can be observed that the proposed multi modal weighted normalization approach value ranges between [0-1] that makes all the calculations simpler and which obtains an average efficiency rate of 97.6% under different transformation. In this analysis the data is augmented with rotation and scaling and have not considered the effects like noise, blur and crop. For some Iris image it was observed that the model is mismatching with the imposters, however this is limitation is got through with the proposed weighted normalization.

V. CONCLUSIONS

A score based multi modal fusion approach with deep networks is proposed in this paper. This work has considered two bio metrics like face and Iris recognition system for which two individual deep networks were designed and are fused together with sum product rule. In unimodal systems for some inputs a low score was attained leading to mis-match or imposter recognition however this got through with the proposed weighted normalization with which the scores are absolute and attained high accuracy.

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A Novel GDI Latch for Sense Amplifier-Based Flip-Flops

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Abstract— In this paper discusses the improvement of a new GDI latch based designing sense amplifier flip-flops (SAFF). One of the most essential characteristics to consider while designing is power consumption, delay, and area. A GDI-based latch architecture is used in the new flip-flop, which reduces power consumption and increases power-delay efficiency (PDP). Tanner EDA tool was used to do the simulation, which used 45nm technology. Simulation results demonstrate that by constructing the latch stage of a SAFF with a Gate Diffusion Input (GDI) method, improved power consumption and delay may be obtained.

Index Terms— Gate Diffusion Logic (GDI), SAFF

I. INTRODUCTION

Flipflops are the most basic elements used in registers, counters and Finite state machines.The performance of these applications such as registers, counters and Finite state machine depends on the performance of flip-flop. As the technology scales down, the supply voltage also scaled.Hence the role of sense amplifier based flip-flops is crucial in these applications.

Flipflops[5] are the basic storage element, containing single bits of data. If latency, Power consumption and area of the flipflop are higher, the application's power consumption will be higher. If the flipflop latency, area and Power consumption of the application are decreased. The application uses less power, has a shorter latency, and takes less space. As a result, developing a delay, area, and power efficient flipflop is essential.

Flipflop is a basic single bit storage element which stores binary information logic 1 or logic 0. The most commonly used flipflop is D flipflop which is also called as Data flipflop or Delay flipflop. The block diagram for Dflipflop is seen below.

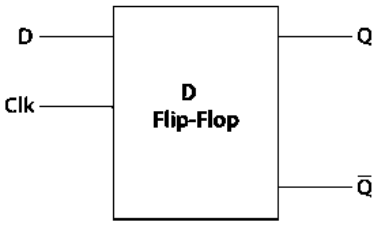

Fig.1 D Flipflop Block Diagram

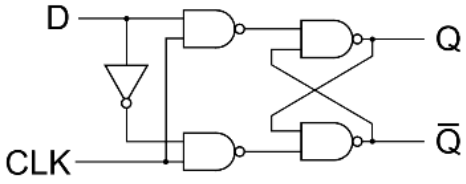

Fig.2 conventional gate level architecture of D Flipflop

Table:1 Truth table of D flipflop

CLK	D	Q	Qb
0	0	Q	Qb
0	1	Q	Qb
1	0	0	1
1	1	1	0

From the above truth table, it can be observed that when the clk signal is high only, the data present in D input will be transferred to Q output.

Because flipflop performance affects application performance, sense amplifier-based flipflops are utilised to increase flipflop performance in terms of power and latency.

A high-speed flip-flop is one that has a sensor-amplifier-based configuration time that is close to 0 or -Ve.

The SAFF consists of slave latch and sense amplifier. The SA level output may be sustained and data gathered immediately after the edge of clk during the positive half cycle of clk.

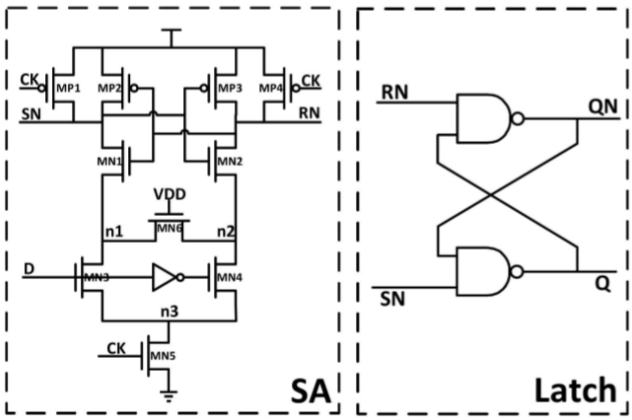

Fig.3 Conventional SAFF

Traditionally CMOS logic design is used for designing the digital circuits. CMOS logic uses both PMOS and NMOS logic.The basic architecture of CMOS logic shown below.

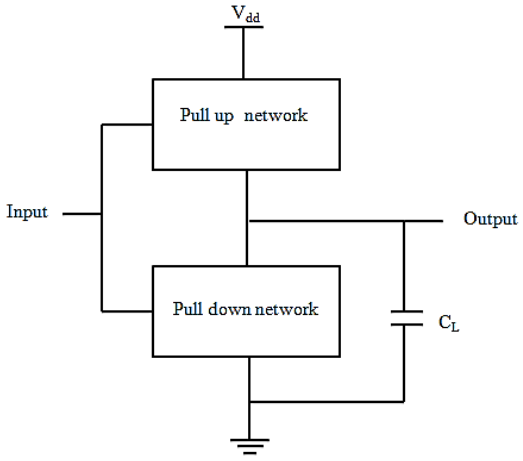

Fig.4(a) Basic CMOS circuit structure

CMOS logic's drive capacity is high. But more electricity is dispersed and more area is needed. In order to solve this issue, several logic models are employed to minimise power consumption, such as transistor logic and gate logic. However, the count of transistors and power are not decreased efficiently. GDI logic is known to be the best effective approach to be used since even the most complicated Boolean algebra can even be implemented using less transistor count. The basic GDI gate is shown below.

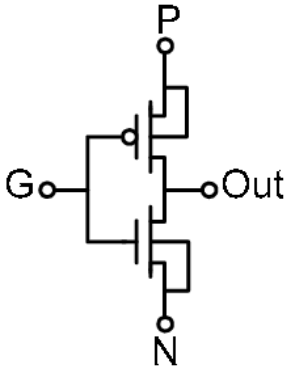

Fig.4(b) A simple GDI gate.

Considering an example of and gate. It is observed from the below figures that the transistor count required for implementing AND gate using GDI logic is 2. The transistor count of AND gate implemented using CMOS logic is 6. From this example, it may be clear that the GDI transistor count is significantly lower than the CMOS Logic count. As the number of transistors is less, the dissipation of power is less. Hence in GDI logic both power dissipation and area are reduced.

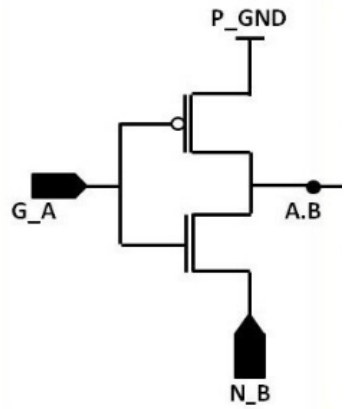

Fig.5 GDI And gate

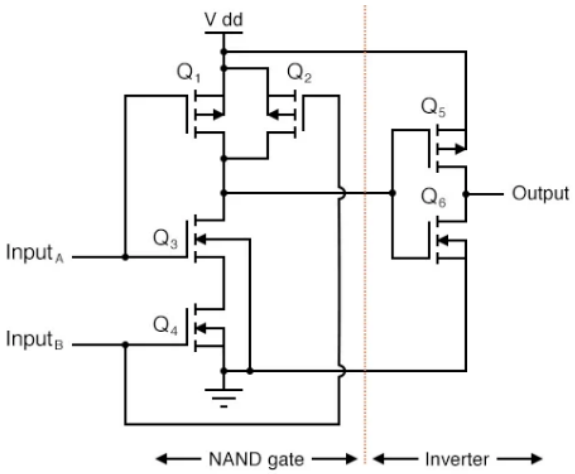

Fig.6 CMOS and gate.

II. RELATED WORKS

Sense amplifier based flipflops are designed to improve the performance at low operating voltages.

Sense amplifier based flipflophs stages. Amplifier stage and latch stage. Previously, the latch used for the latch is Conventional D Latch which is major cause for the delay since the two outputs are dependent on each other. To overcome this, nikolic proposed a novel latch in such a way that the outputs Q and Q bar doesn't depend on each using some complex logic and a pair of not gates. The circuit diagram of nikolic sense amplifier[9] based Flipflop is shown below.

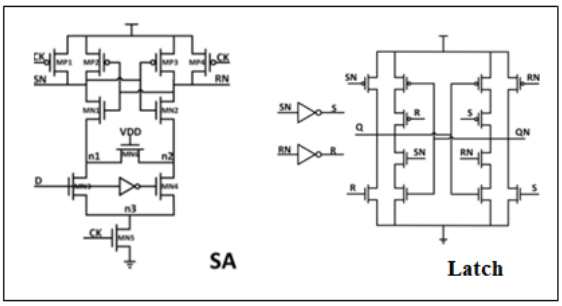

Fig.7 Circuit diagram of Nikolic Flipflop.

Although the dependence of the outputs is eliminated, because of complex logic and usage of pair of not gates, the delay is not as effectively reduced.

To overcome this, Kim [10], proposed a new latch which posses two pairs of not gates and N-C^2MOS circuits. The circuit diagram of Kim's latch is shown below.

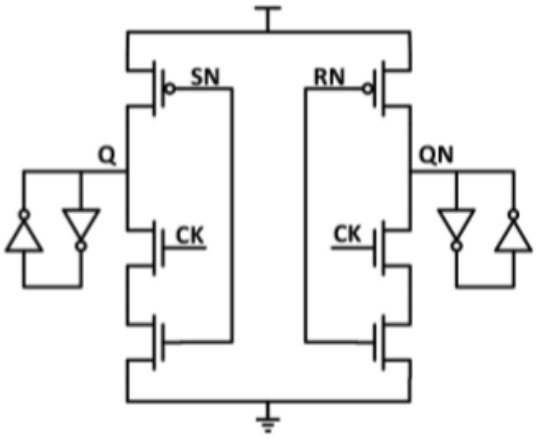

Fig.8 Circuit diagram of Kim's latch.

The power consumption in the Kim's is huge because the two inverters are continuously switching which results in more dynamic power consumption.

A Single ended latch is proposed by Lin to overcome the power consumption that occurs in Kim. The circuit diagram of Lin's latch [11] is shown below.

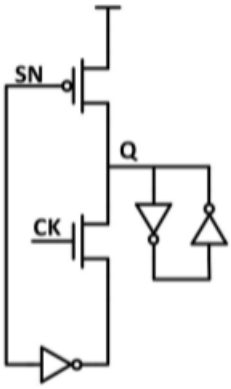

Fig.9 Circuit diagram of Lin's Latch

Although power consumption is reduced, glitches are formed. To overcome this drawback, the strollo proposed a novel latch. The suggested latch's circuit schematic is given below.

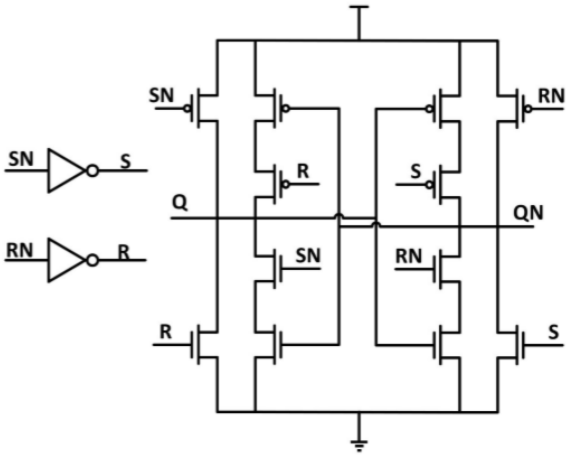

Fig.10 Circuit diagram of strollo's Latch

Till now the latch circuits have been modified. Jeong has now modified the sensing amplifier circuit to decrease the Power consumption. Below is circuit schematic for jeong sensing amplifier-based Flipflop.

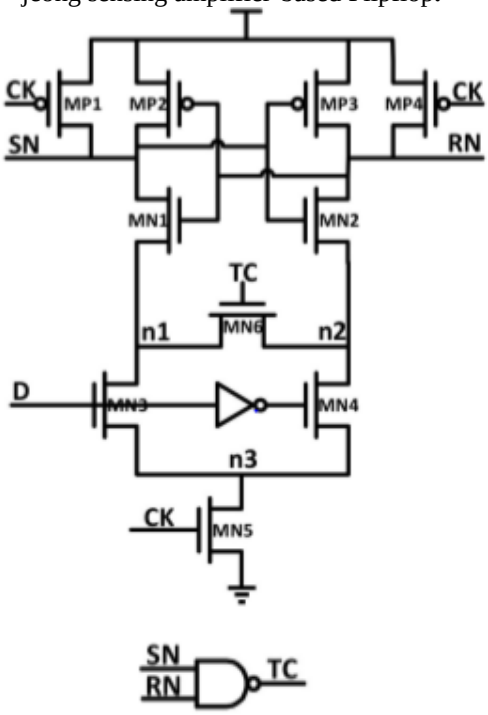

Fig.11 Circuit diagram of Jeong SAFF

In this Jeongsense amplifier[14] circuit, the extra logic that is added to reduce power consumption but this causes increase in delay which is the major drawback.

So to overcome the problem of power consumption without impacting delay, the MTCMOS logic is used. In this, the transistor that is between the nodes n1 and n2 is a HVT transistor and the remaining transistors are standard vt transistors. The circuit diagram of MTCMOS based sense amplifier based flipflop is shown below.

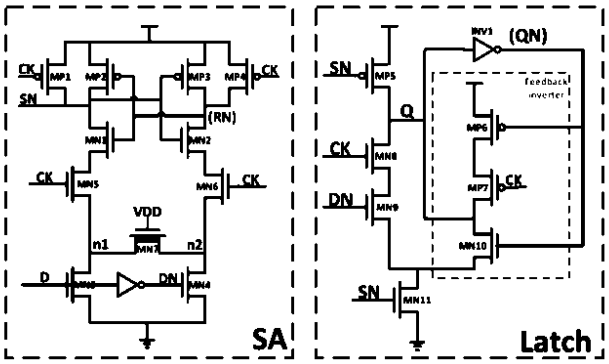

Fig.12 Circuit diagram of MTCMOS sense amplifier based Flipflop

III. IMPLEMENTATION

Power consumption, area and delay are one of the important parameters while designing anydigital circuit. The GDI method is used to design the latch stage of an MTCMOS-based sensor amplifier Flipflop to improve its performance in terms of Area, Power, and Delay.

The GDI technique[1] is gaining the attention of researchers today since it increases performance in terms of power, delay, and area. When compared with other techniques such as transmission gates and CMOS ,the GDI reduces the Delay, Area and Power along with maintain low complexity. It can be seen from the below that various Boolean algebra and logic gates using minimum number of gates compared with the other logics such as CMOS, Transmission gates etc..

Due to rapid technology advancement in mobile and data communications and high interest for the usage of electronic appliances such as Laptop, computers, phones the power consumption and area are mostly crucial while designing the circuits for these applications..

Hence it is necessary to reduce the consumption of flipflop since its application is effected by its performance. If the area of the chip is reduced, more features may be added to the chip. Hence designing the basic flipflop with minimum power consumption and area is needed. The GDI method decreases not only power but also delay and area. From below table it can observed that, the logic gates and various Boolean expression are realized using minimum of gates using GDI technique, when compared to CMOS and transmission gate logic and pass transistor logics.

Table:2 various logic gates and Boolean algebra using GDI[13].

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
0	1	A	$\bar{}$	NOT

For example, from the above table consider MUX implementation.

Fig. 14 GDI technique using 2: 1 mux.

The above figure shows the implementation of the 2 to 1 multiplexer using GDI technique where S is the Select line and A and C are the input operands. The transistor count required for the implementing 2 to 1MUX using GDI logic is only2.

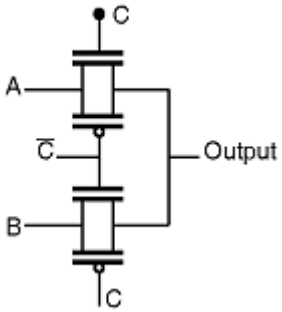

Fig.15 2: 1 mux using Transmission gates.

The 2 to 1 MUX is implemented using transmission gates is shown in the above figure. Here C is the select line, A and B are the input operands. The No.of transistors required for implementing the 2 to 1 multiplexer using transmission gates is 6.

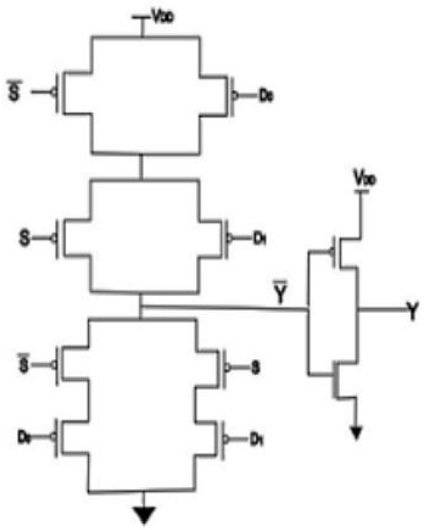

Fig.16 CMOS Logic Using 2:1 mux.

The 2 to 1 MUX is implemented using static CMOS Logic gates is shown in the above figure. Here S is the select line, D0 and D1 are the input operands .The no. of transistors required for implementing the 2 to 1 multiplexer using transmission gates is 12.

The 2 to 1 MUX is implemented using static CMOS Logic gates is shown in the above figure. Here S is the select line, I0 and I1 are the input operands. The no. of transistors required for implementing the 2 to 1 multiplexer using transmission gates is 4.

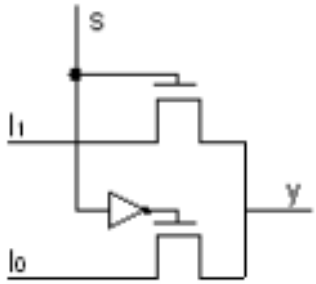

Fig.17 2:1 mux using pass transistor Logic.

In comparison to other logics, the transistor count of a 2 to 1 multiplexer constructed using the GDI technique[13] is the smallest, as seen in the above Figures. It can also be observed that GDI consumes less power since it uses minimal number of transistors.

Since Mostly, the flipflops are used in power hungry applications like CPU. Hence in our proposed method, the latch stage is designed using GDI technique. By using this technique, the proposed Flip flop consumes less power, area and delay. The schematic of sense amplifier based Flipflop is shown below.

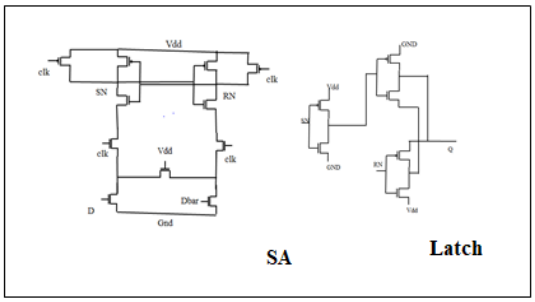

Fig.18Block diagram of sense amplifier based Flipflop using GDI latch

This sense amplifier based flipflop works in two phases.

1. Phase of pre-charge

2. Phase of evaluation

The internal nodes SN and RN will be charged during the phase of pre-charge (clk=0). In the Phase of evaluation (clk=1) actual flipflop operation occurs.Whenclk=0 both pmos transistors with clk as input at the gate are on, the charge from vdd is transferred to SN and RN nodes.

When clk=1, the charge stored in SN and RN nodes is discharged through based on the inputs. Since for NMOS-_7 and NMOS_8 gates clk is given as input, both are ON.Now based on D and Dbar input, either SN or RN is discharged.

Now consider D=1 since D=1, SN will be discharged and RN will not get discharged (since Dbar =0).Since RN=1 N11 is on whose source is connected to vdd. Since it is on, the vdd present in the source will appear at the drain. Now this is given as input to N10 Source. The gate of N10 is connected to SN inverted output which is logic high. Since it is logic high N10 gate is on and the vdd present in the source is appeared at Q.

Now consider D=0 since D=0, SN will not be discharged and RN will get discharged (since Dbar =1).Since SN=1, SN Inverted output will be zero. hence P6 gate will be on and its source is connected to ground. Since the gate is on, the logic low value present in the source will be transferred to Q.

As seen in Fig. 18, the proposed circuit has a less transistor count than previous SAFF designs. The proposed SAFF is not only area but also power and delay efficient. When this proposed SAFF is used in various applications such as registers, counters, the power, delay and area of the application is also reduced which is the major concern in VLSI circuits.

IV. RESULTS AND DISCUSSIONS

The schematic diagram and waveform of sense amplifier based flipflop is shown below. Simulations are performed using Tanner EDA tool using 45nm technology.

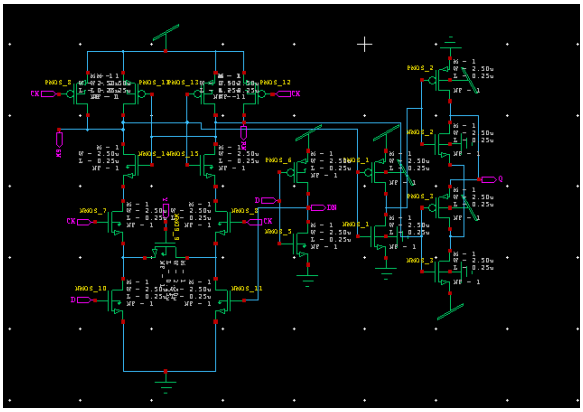

Fig. 19 schematic diagram of proposed SAFF using GDI based latch.

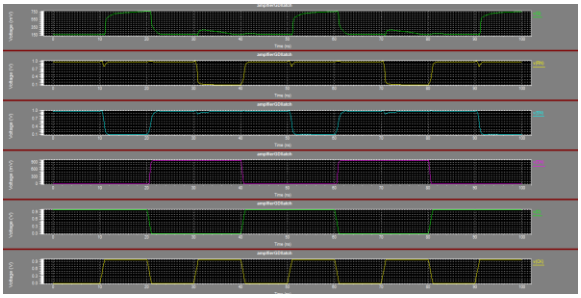

Fig 20Waveform of proposed SAFF using GDI based latch.

Table 3: Comparison table for Power, Delay and Area

	Power	Delay	Area
Existing SAFF	46uw	10.2ns	22
Proposed SAFF	28uw	0.4ns	19

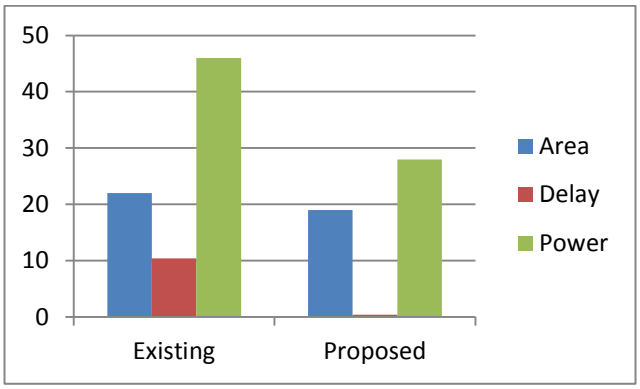

Fig.21 Comparison of area between existing and proposed method

V. CONCLUSION

The design of a novel GDI latch for designing sense amplifier-based flip-flops is presented in this article (SAFF). A GDI-based output stage latch topology is used in the new flip-flop, which reduces power consumption and area and delay. By using 45nm technology, the simulation was performed using Tanner EDA platform. Simulation results show that using a GDI technique for designing the latch stage in Sense amplifier based flip flop results in better power consumption and delay and area.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Sun Tracking Solar Panel

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Abstract— Of all the renewable energies, solar energy is the only energy gained its popularity and importance quickly. Through the solar tracking system, we can produce an abundant amount of energy which makes the solar panel's workability much more efficient. Perpendicular proportionality of the solar panel with the sun rays is the reason lying behind its efficiency. Pecuniary, its installation charge is high provided cheaper options are also available. This project is discussed all about the design and construction mechanism of the prototype for the solar tracking system having a single axis of freedom.

The main control circuit is based upon NodeMcu microcontroller. Programming of this device is done in the manner that the LDR sensor, in accordance with the detection of the sun rays, will provide direction to the DC Motor that in which way the solar panel is going to revolve. Through this, the solar panel is positioned in such a manner that the maximum amount of sun rays could be received. In comparison with the other motors, DC motor is the simplest and the suave one, the torque of which is high and speed of which is slow enough. We can program it for changing the direction notwithstanding the fact that it rotates only in one direction subject to exception as far as programming is concerned. 1985, first time ever it was witnessed for production of the silicon solar cells with an efficiency of 20%. Though a hike in the efficiency of the solar panel had a handsome increase still perfection was a far-fetched goal for it. Below 40%, most of the panels still hover to operate. Consequently, peoples are compelled to purchase a number of panels in order to meet their energy demands or purchase single systems with large outputs. Availability of the solar cells types with higher efficiencies is on provided they are too costly to purchase. Ways to be accessed for increasing solar panel efficiencies are a plethora in number still one of the ways to be availed for accomplishing the said purpose while reducing costs, is tracking. Tracking helps in the wider projection of the panel to the Sun with increased power output. It could be dual or single axis tracker.

Duality ragged up with better compatibility as far as tracking of the sunlight from both the axis is concerned. Commercially single tracker is cheaper to use through booming of power is considerable and therefore a minuscule increase in the price is worthy and acceptable, provided maintenance cost should float around on an average level.

I. INTRODUCTION

Bustling civilization is the vein through which modern civilization is operated. Energy day by day is put to use at its best to fulfil the desires and ambition of the peoples at large. Each and every corner of our life is caged with various layers of impediment and in this response, energy is becoming an indispensable factor. Therefore, the source of energy needs to be endless/ perpetual in order to carry this colossal population ahead. Human beings being evolutionary in nature are perhaps the best ever creation of nature is always in the race of envisaging the probable and available comforts and benefits in every possible angle in this perilous world. The evidential matrix manifests that in a dichotomy of various opinions what options best expedite the scarcity of energy in an immensely heterogeneous society like ours. Our motto is to endeavour in forwarding such noble goal of energy conservation.

Taking a look at the present scenario it is evident that conventional sources of energy such as coal, natural gas, oil, etc. are at the edge of extinction. Being in mortal combat with time itself to fulfil every demand for energy the demand for these resources for energy has escalated to its zenith. The conventional use of energies due to the burning of fossil fuels like coal, oil and natural gas, the whole environment is getting polluted. The present project, therefore, is orchestrated with components like LDR module, DC Motor, Photovoltaic array etc. according to which while the functioning of, unlike other use of the conventional energies, would not emit any pollution and in turn act as a reservoir of energy taken from the Sun itself. As adumbrated no other energy is more abundant than solar energy as per as its availability and freeness are concerned, utilization of which, compounded with rest of the fact of its conversion into electrical energy. Historically if counted, in the year 1881 for the first time ever solar panel was invented. Later on, all through the hands of Russell Ohl in the year, 1941 concept of the solar cell was conceived and subsequently workability of a solar panel has also advanced in comparison with the earlier span. Though it is improbable still it is not impossible as per as tracking of the mother energy is concerned in furtherance to which attempt has been taken through this project to confine every drop of energy from being left out.

II. LITERATURE SURVEY

The paucity of available resources has forced contemporary society to look for measures to consummate the demands of the latter. With the nurturing civilization, the depletion of conventional fuels, due to human practices has been an alarm to sustainable development issues. The scarcity of energy and its source guided us towards the optimistic approach of using the alternative resources bestowed to humankind–Solar, tidal etc.

The Sun has been looked upon as an imperative source of energy. Solar energy is an eco-friendly resource as compared to its counterparts. The advancement of technology has out-turn foster techniques to utilize this

energy into its own good use. Be it as thermal energy, electricity, fuel production and many more. Photovoltaic or concentrated solar power (CSP) systems are operated to transfigure the solar power expropriated by the earth into electricity. Solar tracking device utilizes this expropriated solar power through the channel of photovoltaic arrays, an oriented scaffolding of photovoltaic/solar cells.

Solar cells, also known as photovoltaic cells are used to convert light energy into electricity. Photovoltaic cells work on the principle of the photovoltaic effect, which is similar to the photoelectric effect. Differences being that the electrons in photovoltaic are not emitted instead contained in the material around the surface, creating a voltage difference. Solar cells are forged with crystalline silicon. It is the most commonly used material in a solar cell. The use of silicon in the solar cell has been very efficient and low cost. Two forms of crystalline silicon can be used to make solar cells. Other than silicon, solar cells can be fabricated with cadmium telluride (CdTe), Copper indium gallium (di)selenide (CIGS) etc. the fabrication of solar cells with materials other silicon is slightly expensive, thus making silicon the best material to be used in solar tracking systems.

One of the finest and extensively used material, monocrystalline silicon has an efficiency of about 15-20%. While under high temperature the performance of the cell material drops by 10-15% of the initial.

Polycrystalline silicon is another form, cheaper than the latter but has the same band gap as that of monocrystalline silicon. Though it has the same band gap energy, it lags in efficiency, hence this material is used in low-cost products.

Amorphous silicon cells can work under extremely high temperatures, but the efficiency of these cells is comparatively lower than the other silicon forms.

The technologies which use CdTe, CIGS, Amorphous Thin-Film Silicon (a-Si, TF-Si) in the fabrication of solar cells are known as thin film photovoltaic modules. These thin-film solar cells are relatively cost-effective than the solar cells of crystalline silicon.

There are several other factors on which the efficiency of a solar cell depends.

Cell temperature

Energy Conversion Efficiency

Maximum power point tracking

Solar panels are a cumulative orientation of photovoltaic cells. The PV cells are arranged in a solar panel or a PV array such that is serves the purpose of exciting the electron of the material consisting inside the solar cells using photons. The average amount of sunlight received by solar panels particular depends on the position of the sun.

Being a repository of energies, Sun witnessed to be the eminent and ever continuing source of emitting radiation from it. A part of this source of natural energy is received by the solar panel. Certain ways have been developed to utilize this energy source as an alternative to other nonrenewable sources. Considering its multitudinous flourishing ways in which it can be applied to bring about the change in conserving other resources, the manipulation of the energy source is encouraged.

III. METHODOLOGY:

In this paper we have proposed a new architecture called as Face Mask Detection for Preventing Respiratory Infections using Arduino UNO to detect weather a person wearing mask or not. The proposed architecture is easier to implement as well as the cost is also low . The system is designed to detect the faces and to determine whether the person wears a face mask or not. Using the above data, we can decide whether the concerned person can be allowed inside public places such as the market, or a hospital. This project can be used in the hospital, market, bus terminals, restaurants, and other public gatherings where the monitoring has to be done.

This project consists of a camera that will capture the image of the people entering public places and detect whether the person wears a face mask or not using their facial features.

IV. RESULT AND DISCUSSION:

The results for the project were gotten from LDRs for the solar tracking system and the panel that has a fixed position. The results were recorded for four days, recorded and tabulated. The outputs of the LDRs were dependent on the light intensity falling on their surfaces. Arduino has a serial that communicates on digital pins 0 and 1 as well as with the computer through a USB. If these functions are thus used, pins 0 and 1 can be used for digital input or output.

Arduino environment's built in serial monitor can be used to communicate with the NodeMcu board. To collect the results, a code was written that made it possible to collect data from the LDRs after every one hour

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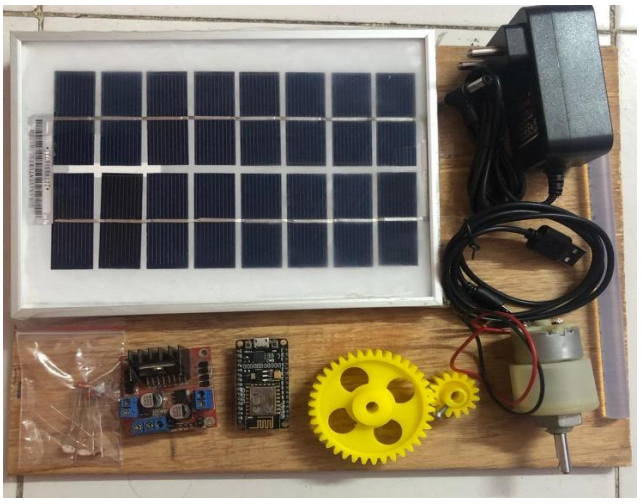

Figure: 4.1 Implementation of project.

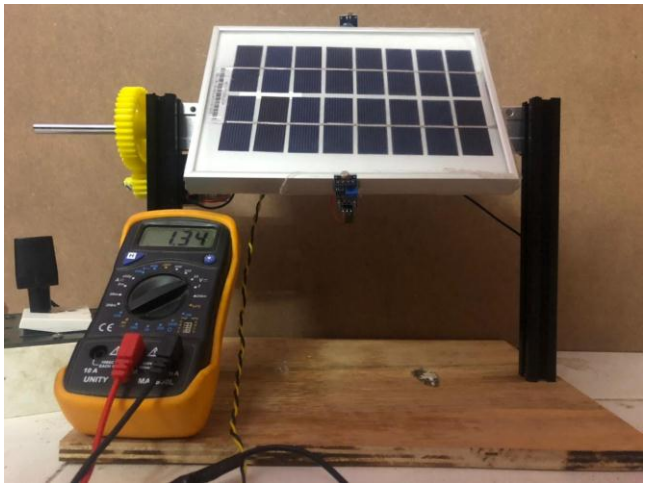

Figure: 4.2 Power supply to the kit.

The values from the two LDRs are to be read and recorded at the given intervals. The LDRs measure the intensity of light and therefore they are a valid indication of the power that gets to the surface of the solar panel. The light intensity is directly proportional to the power output of the solar panel

From the tables, it can be seen that the maximum sunlight occurs at around midday, with maximum values obtained between 1200 hours and 1400 hours. In the morning and late evening, intensity of sunlight diminishes and the values obtained are less that those obtained during the day. After sunset, the tracking system is switched off to save energy. It is switched back on in the morning.

For the panel fitted with the tracking system, the values of the LDRs are expected to be close. This is because whenever they are in different positions there is an error generated that enables its movement. The motion of the panel is stopped when the values are the same, meaning the LDRs receive the same intensity of sunlight. For the fixed panel, the values vary because the panel is at a fixed position. Therefore, at most times the LDRs are not facing the sun at the same inclination. This is apart from midday when they are both almost perpendicular to the sun.

Days with the least cloud cover are the ones that have the most light intensity and therefore the outputs of the LDRs will be highest. For cloudy days, the values obtained for the tracking system and the fixed system do not differ too much because the intensity of light is more or less constant. Any differences are minimal. The tracking system is most efficient when it is sunny. It will be able to harness most of the solar power which will be converted into energy. In terms of the power output of the solar panels for tracking and fixed systems, it is evident that the tracking system will have increased power output. This is because the power generated by solar panels is dependent on the intensity of light. The more the light intensity the more the power that will be generated by the solar panel.

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15th-16th July, 2021 – Virtual Conference

High Frequency Square Wave Modulation for MMC Based DC-DC SST for Interconnection of HVDC Grids

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Abstract— Voltage ratings for HVDC point-to-point connections are not standardized and tend to depend on the latest available cable technology. DC/DC conversion at HV is required for interconnection of such HVDC grids which are at different high voltage levels, as well as to interface dc wind farms, solar parks and other renewable sources. MMC Based DC-DC solid state transformer (SST) is an option to interconnect such HVDC grids. MMC based voltage converters offers lower switching losses compared to two or three-level VSCs. The SST offers flexible interconnection, buck, boost, and DC circuit breaking operations efficiently. Typical HF dual-active phase-shift modulation principle is analyzed. HF voltage, current and power characterization, and different kinds of rating current of the SST during different modulations are analyzed for the same transmission power. An efficient high frequency square wave modulation technique is proposed over other modulation techniques for better performance, simple control. High frequency will reduce the size of the transformer and other passive elements significantly in the circuit. Finally MATLAB simulation results verify the theoretical analysis.

Index Terms— MMC, SST, HF, Square wave modulation, HVDC grids, DC-DC converter

I. INTRODUCTION

A number of high-voltage dc (HVDC) projects are currently under development and consideration in the world. The interest in HVDC is driven by the expansion of renewable generation capacity in places such as Scotland, Germany, India, China, USA, as a means to efficiently transmit the generated power to far away load centers. As most of the currently or already built projects are of the point-to-point type which, coupled with the absence of a common standardized dc grid code like ac grid standards, allows the voltage ratings to be freely chosen by each developer. As a result the voltage rating is often a function of the available cable technology at the time of development [1]-[4]. At some point in future interconnection of point-to-point projects will require dc/dc voltage conversion technology for HVDC applications. The voltage conversion ratio has important effects on the future converter technology as it influences the magnitude of currents and amount of stress imposed on the DC-DC converter. A low step ratio could be used to interconnect existing HVDC networks of different nominal voltages (up to 1.5). Connections to a dc collection grid of an off-shore wind farm may require a medium step ratio (1.5 to 5) [5]-[7]. This paper presents a possible dc/dc system for low to medium step-ratio applications. It consists of two HF dc/ac converters coupled through a transformer in front to-front connection. The transformer provides galvanic separation between the two dc connections as well as the voltage step. This arrangement is called DC-DC SST. Such a SST system could be used to interconnect existing HVDC network in building a larger HVDC network [8]-[10]. It may also be used to connect an off-shore wind park to existing HVDC link. Furthermore, the galvanic separation is provided by the HF transformer[11].

The modular multilevel converter (MMC) is attracting more and more attention in HVDC research field because of its advantages, such as high modularity, better harmonic characteristics, low losses, and high reliability. But, most research efforts of the MMC in the world have focused on LF ac to dc conversion, such as transmission power characterization, circulating current suppression, voltage balance strategy, dynamic models, and new topologies [12]. This improves the performance of the MMC up to some level. But there is already a research trend to employ an MMC in dc–dc converter bases SST. But there is already a research trend to employ an MMC in a dc–dc converter based SST. The SST based on the MMC is used to step up or step down dc in medium-voltage dc (MVDC) and HVDC applications [12].

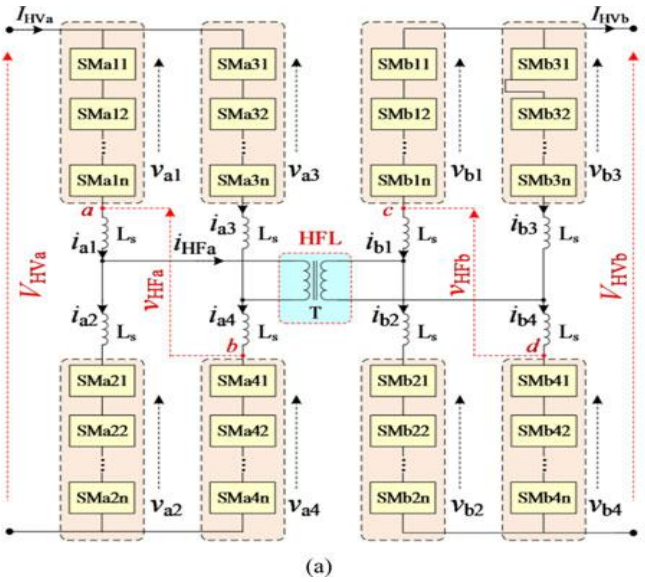


Fig.1. (a) Topology of SST

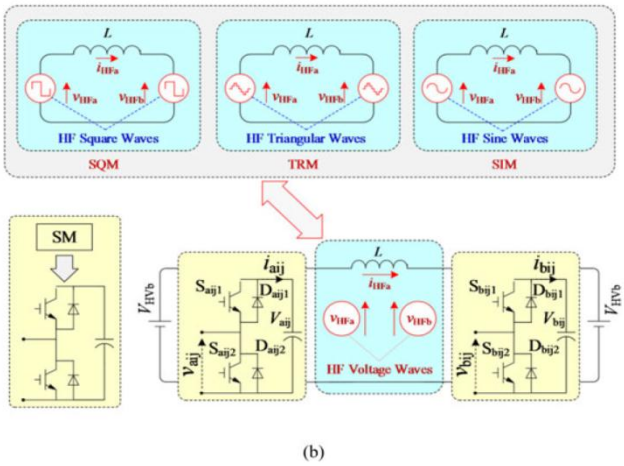


Fig.1. (b) Dual-active phase-shift principle of SST

These topologies have internal HF link but the full power is not processed by a traditional intermediate ac transformer. In order to develop interconnects between HVDC grids, a HF front-to-front dc–dc converter based on the MMC (SST) is proposed as shown in Fig. 1(a) [13]. This MMC can increase the voltage level of the SST. This SST operates as a dc circuit breaker to cutoff the connection of two HVDC systems and be designed with redundancy to improve the reliability.

In general applications of the MMCs, ac output is modulated with a sine wave, to reduce the harmonic content. The conversion efficiency will be high. But the aim of the SST is to transfer dc power; ac link is only a middle transition link, so no requirement of strict sine waves [14]. Triangular modulation was also discussed for the HF MMC, the harmonic content of triangular modulation is lower than square wave modulation and modulate algorithm is simpler than sine wave modulation, but voltage utilization ratio is the lowest. Square wave modulation is a suitable method for the HF SST. However, the square wave modulation will cause a large circulating power in HF link, especially when terminal voltages do not match the transformer ratio [15].

This paper gives a comprehensive theoretical analysis and simulation verification of HF link modulation of the SST. This paper is organized as follows. Section II analyzes typical HF link dual-active phase-shift principle and square wave modulation for the SST. Section III gives detailed analysis of HF link voltage and current and power characterization. Section IV gives a detailed switching characterization of the SST in all operating states and gives the suitable control methods. Section V gives MATLAB simulation results. Section VI gives conclusion and the future scope of the paper.

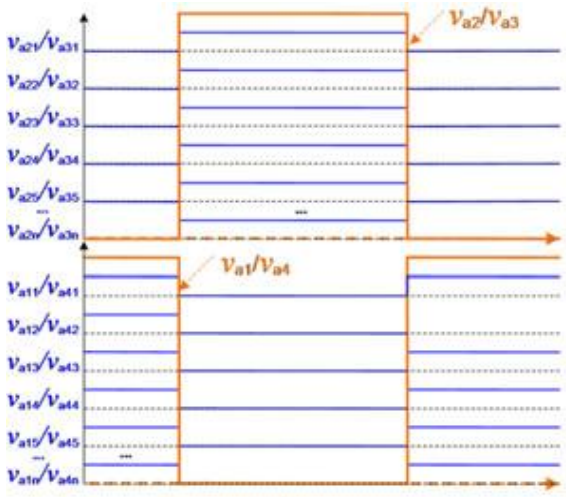
II. DUAL-ACTIVE PHASE-SHIFT MODULATIONS FOR SST

Dual-Active Phase-Shift Principle

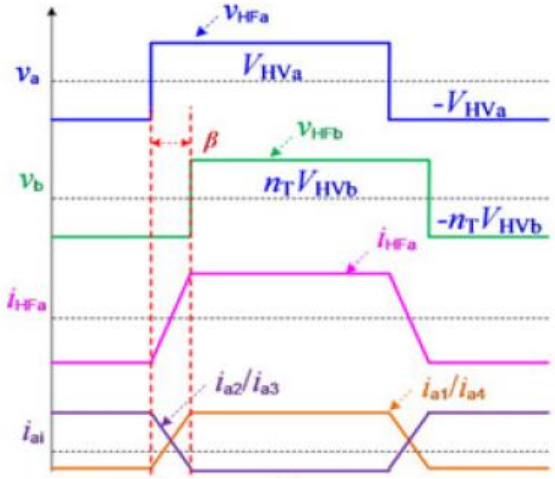
Fig.1. (b) gives dual-active phase-shift principle for the SST. The whole system can be equivalent to two HF waves connected with an inductor, the magnitude and direction of power flow can be adjusted by controlling the magnitude and direction of phase shift angle between two HF waves [16]. Because the magnetizing inductance is small compared with HF link series inductance in the dual-active phase-shift converter, so it is usually neglected in general theoretical analysis. Thus, the equivalent inductance L shown in Fig. 1.(b) contains leakage inductance L_T of the transformer and equivalent HF link inductance of arm inductor in the MMC, because the equivalent HF link inductance of an MMC is L_S , thus, $L = 2\ L_S\ + L_T$. In Fig. 1(b), v_{HFa} and v_{HFb} are equivalent voltages of the HF link in HV_a side, v_{HFa} is positive when the voltage of point *a* is higher than that of point *b*, v_{HFb} is positive when the voltage of point *c* is higher than that of point *d*; i_{HFa} is the current in HF link; V_{HFa} , V_{HFb} and I_{HFa} , I_{HFb} are the voltage and current at the $HVDC_a$ and $HVDC_b$ sides, respectively; v_{aij} is the voltage of the sub module in the ac side; $v_{a1} \sim v_{a4}$ and $i_{a1} \sim i_{a4}$ are voltage and currents of whole arms, respectively; and L is the equivalent inductance of the arm inductor and the HF transformer [17].

Square High-Frequency-Link Modulation

The square modulation of high-frequency-link based on dual active phase shift for the SST is shown in Figs. 2(a) and 2(b). Each sub module generates 50% duty-ratio square voltage, whose positive and negative voltages are V_{ca} and 0, respectively, where V_{ca} is the average dc voltage of capacitor in HV_a side. In the analysis, dc voltages of capacitors are assumed the same because of balancing control [18]-[19]. There is no phase-shift angle between different sub modules in the same arm, and all the output voltages of different sub modules are almost the same. In this case, the ac current will not be multilevel and sine waves. The maximum values of HF link voltages are V_{HVa} and $n_T V_{HVb}$. In this thesis, we assume $n_T = 1$, and the square HF link modulation is defined as SQM. If we employ the ideal square modulation, the arm inductors may experience very high voltage stresses when all SMs in the same arm are simultaneously inserted or bypassed, so we will add a very small phase-shift angle between neighboring SMs in practice to decrease voltage stress, thus the voltage step is just V_{HV}/n. Because the phase-shift angle is very small, this is far smaller than that in TRM. So the performance of SQM in practice can be approximated with the ideal square modulation in theoretical analysis [20].



(a)



(b)

Fig.2. (a) Voltage waveform (b).Current waveform for Square High-Frequency-Link Modulation

III. VOLTAGE, CURRENT AND POWER CHARACTERIZATION FOR SQM MODULATION

Voltage Characterization

Assuming that dc voltages of all capacitors are adjusted the same by balancing control. For SQM, the HF square voltages can be derived based on Fourier transform as

$$v_{\mathrm{HF}a\_Sq}=\sum_{k=1,3,5,\ldots}\frac{4V_{HVA}}{k\pi}\sin(kw_0t) \tag{1}$$

Because the MMC on side *b* has the same operation with side *a*, for HF link voltage V_{HFb}, we just need to adjust the phase angle of voltage V_{HFa} with β.

Current Characterization

For dual-active phase-shift control, the HFL current can be derived as

$$i_{\mathrm{HF}a(t)}-i_{\mathrm{HF}a(0)}=\int_0^t\frac{v_{HFa}-v_{HFb}}{L}dt \tag{2}$$

Considering the symmetry in one switching cycle, and the average current of inductors over one switching period should be zero in steady state, we have

$$i_{\mathrm{HF}a}\left(\frac{\pi}{w_0}\right)=-\,i_{\mathrm{HF}a}\,(0) \tag{3}$$

Where

$w_0 = 2\pi f_S$ is the angular frequency and f_S is the switching frequency. Then, From (1)–(3), the HFL current of SQM can be derived as

$$i_{\mathrm{HF}a\_Sq}=\sum_{k=1,3,5,\ldots}\frac{4}{k^2\pi w_0L}\sqrt{A^2+B^2}\sin\left(kw_0t+\tan^{-1}\frac{\mathrm{A}}{\mathrm{B}}\right) \tag{4}$$

Where

$$\mathrm{A}=V_{HVB}\cos(k\beta)-V_{HVA},\quad \mathrm{B}=V_{HVB}\sin(k\beta) \tag{5}$$

Power Characterization

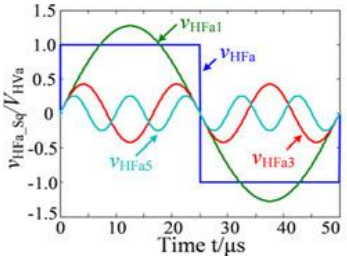
The average power during one switching period can be described as

$$P=\frac{1}{T}\int_0^T v_{HFa}(t)i_{HFa}\,(t)dt \tag{6}$$

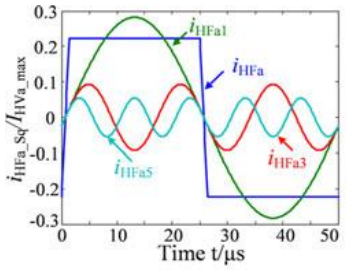
Where $T = 1/f_S$ is the switching period.

From (1)–(6), the active power can be derived as

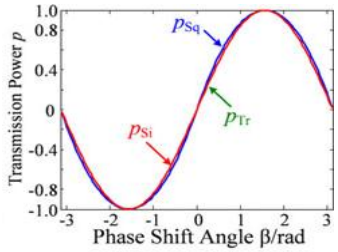
$$P_{Sq}=\sum_{k=1,3,5,\ldots}\frac{8V_{HVA}V_{HVB}}{k^3\pi^2w_0L}\sin(k\beta) \tag{7}$$



(a)



(b)



(c)

Fig.3.(a) HF link voltage,(b) Current (c) Transmission Power characterization

HF link Voltage, Current and Transmission Power characterization for SQM are shown in Fig.3.(a),(b) and (c) respectively. The voltage is normalized by dc voltage V_{HVa} in Fig.3.(a), and in (b) the current is normalized by maximum dc current $V_{HVa\text{-}MAX}$ .The transmission power characterization is shown in Fig.3.(c), where transmission power is normalized by $P_{sq\text{-}max}$. The transmission power achieves the maximum value when $\beta = \pi/2$ for SQM.

Where

$$P_{Sq\_max} = \frac{\pi V_{HVA} V_{HVB}}{4 w_0 L} \tag{8}$$

In practice, the power transmission ability can also be adjusted by adjusting the HF link inductance L.

Circulating Power

The circulating power is synonymous with reactive power, which can be described as HFL power factor,

That is

$$\lambda_{\mathrm{Sq}} = \frac{P_{Sq}}{S_{Sq}} = \frac{P_{Sq}}{V_{HFa\_Sq} I_{HFa\_Sq}} \tag{9}$$

Where $V_{HFa\text{-}sq}$, $I_{HFa\text{-}sq}$ are HF link RMS voltage and RMS current values of square wave modulation.

From (1) and (4), The HF link RMS voltage can be derived as

$$V_{HFa\_Sq} = \frac{2\sqrt{2}}{\pi} V_{\mathrm{HVA}} \sqrt{\sum_{k=1,3,5,..} \frac{1}{k^2}} \tag{10}$$

The HF link RMS current can be derived as

$$I_{HFa\_Sq} = \frac{2\sqrt{2}}{\pi w_0 L} \sqrt{\sum_{k=1,3,5,..} \left(\frac{\sqrt{A^2+B^2}}{k^2}\right)^2} \tag{11}$$

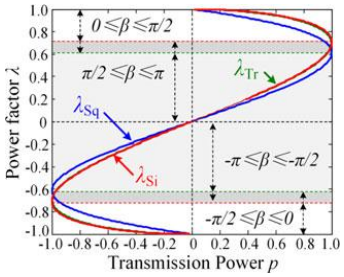


Fig.4. circulating power

From Fig.4 The power factor when $\pi/2 \le \beta \le \pi$ and $-\pi \le \beta \le -\pi/2$ is lower than that when $\pi/2 \ge \beta \ge 0$ and $0 \ge \beta \ge -\pi/2$, because the transmission power characterization is the same, so the phase-shift angle β just need to be designed during $[-\pi/2, \pi/2]$ in practice.

According to the above analysis, the SQM can get higher power transfer ability, but also the SQM has higher circulating power with the same transmission power.

HF Link RMS Current, Arm RMS Current, Arm Average Current and Current Stress for Switches

1. *HF Link RMS Current*

The HF link RMS currents for square modulation is given in (11) and maximum dc current is given as

$$I_{\mathrm{HVa\_max}} = \frac{P_{Sq\_max}}{V_{HVa}} = \frac{V_{HVb}}{4 w_0 L_{Sq}} \pi \tag{12}$$

2. *Arm RMS Current*

The arm currents of the MMC can be considered as the sum of half of ac current, half of dc current, and a circulating current. Additional harmonic components will appear, if the circulating current is left uncontrolled. To simplify the analysis in this paper, the harmonic components of arm current are ignored. Thus, for the SST, the arm current can be derived as

$$i_{a1} = i_{a4} = \frac{I_{\mathrm{HVa}}}{2} + \frac{i_{\mathrm{HFa}}}{2}$$
$$i_{a2} = i_{a3} = \frac{I_{\mathrm{HVa}}}{2} - \frac{i_{\mathrm{HFa}}}{2} \tag{13}$$

Then, the arm RMS current can be derived as

$$I_{\mathrm{Arm}} = \sqrt{\left(\frac{P_{\mathrm{HFa}}}{2V_{\mathrm{HVa}}}\right)^2 + \left(\frac{I_{\mathrm{HFa}}}{2}\right)^2} \tag{14}$$

and, the SQM has the lowest arm RMS current.

3. *Arm Average Current*

According to the given analysis, the arm average current for the SQM can be calculated as

$$I_{\mathrm{Arm}} = \frac{1}{T} \int_0^T \left| \frac{i_{\mathrm{HFa}} + I_{\mathrm{HVa}}}{2} \right| dt \tag{15}$$

Where I_{Arm} is the absolute average value of the arm current. The arm average current is useful for the analysis of

conduction loss of switches. Similar to the arm RMS current arm average current is also lowest for square modulation.

4. *Current Stress for Switches*

In this paper, the current stress for switches is defined as the maximum peak value of the arm current. According to the given analysis for SQM, the current stress will be achieved at $w_0t = \beta$ or $w_0t = \pi$.

Then, the current stress for switches can be deduced as

$$I_{\mathrm{ArmM\_Sq}} = \frac{P_{\mathrm{Sq}}}{2V_{\mathrm{HV}a}} + \sum_{k=1,3,5,\cdots} \frac{2V_{\mathrm{HV}a}}{k^2\pi w_0 L_{\mathrm{SQM}}}[1-\cos(k\beta)] \quad (16)$$

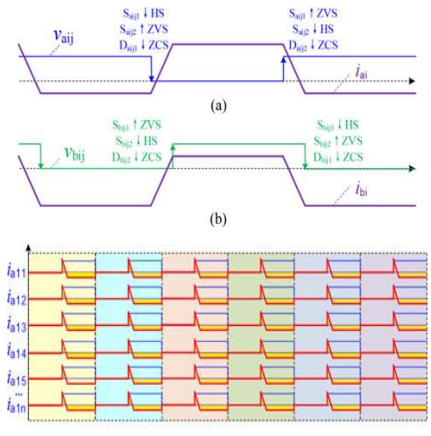
Where I_{ArmM} is the current stress of the switches

IV. SWITCHING CHARACTERIZATION OF SST FOR SQM

The SST has the symmetrical topology, the turn off behavior is the same when the power flow direction changes, we just need to exchange the turn off behaviors of HV*a* and HV*b* sides, so the analysis of switching characterization is carried out when the power flows from the HV*a* side to the HV*b* side. In addition, the turn on loss of diode is very small. In practice, it is ignored in the analysis.

Switching Characterization for SQM

For SQM, there is no phase-shift angles between different sub modules in the same arm, all the output voltages of different sub modules are the same, so all the sub modules have the same switching behavior. For the MMC in the V_{HVa} side, which generates power, the switching characterization is shown in Fig.5. If $v_{aij}: 0 \rightarrow V_{ca}$, then the current is positive; when v_{aij}: $V_{ca} \rightarrow 0$, then the current is negative. Then, during one switching period, soft switching behaviors are as follows: S_{aij1} turn ON with zero voltage switching (ZVS), D_{aij2} turn OFF with zero-current switching (ZCS), S_{aij2} turn ON with ZVS, and D_{aij1} turn OFF with ZCS; the hard switching (HS) behaviors are as follows: S_{aij2} turn OFF and S_{aij1} turn OFF.



(c)

Fig.5 Switching characterization of SST (a) HVa side (b) HVb side (c) Current characterization

MMC in the V_{HVb} side that absorbs power, the switching characterization is shown in Fig. 5(b). If $V_{bij}: 0 \rightarrow V_{cb}$, then the current is positive, if V_{bij}: $V_{cb} \rightarrow 0$, then the current is negative. MMC in the HV*b* side has the same switching behaviors with the MMC in the HV*a* side. From the above analysis, for SST with SQM, all the switches are turn ON with ZVS, all the diodes turn OFF with ZCS. The HS behavior is just to turn OFF for all the switches. According to the aforementioned analysis, the switching behaviors of the HV*a* and HV*b* sides are the same for all types of modulations. The switching behavior is simple for SQM. Every turn ON behavior of switch will be accompanied with a turn OFF behavior of the diode.

Control Characterization

For the SST, the key is to control the voltage balance of discrete capacitors for all sub modules. As analyzed in the previous section, the current flows through the capacitor just when S_{aij1} is turned ON. For SQM, there are no phase-shift angles between different sub modules in the same arm, $S_{aij1} \sim S_{aij2}$ have the same switching states, so the currents of dc capacitors during one switching period are the same. As shown in Fig. 5(c), the voltage of dc capacitors in the same arm can be balanced automatically in theory. In practice, because of the deviation of component values and driving pulses, the voltage balance of SMs may not be achieved naturally, for all the modulations, the assist capacitor voltage balance control method is still needed.

V. MATLAB SIMULATION RESULTS

To verify the above cited analysis, a 2-kW SST MATLAB Simulation platform is built, the main parameters are as follows: the HVDC voltages $V_{HVa} = V_{HVb} = 400$V, the number of sub modules $m = n = 4$, the rated voltages of dc capacitors $V_{aij} = V_{bij} = 100$V, the transformer ratio $n_T = 1:1$,the leakage inductance of transformer $L_T = 40\mu$H, the arm inductor $L_S = 30\mu$H, the switching frequency $f_S = 20$ kHz. The phase shift angles for the sub modules are zero

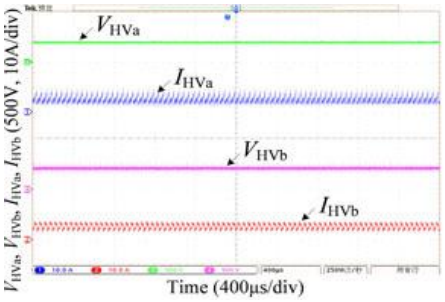


Fig.6. HVDC voltage and current waveforms in SST

Fig.6 gives HVDC voltage and current waveforms with square modulation in the SST. It is seen that the HVDC buses can operate normally during square modulation. The current and voltage conversions of the SST operate as required. For square modulation, because of the dc capacitor cannot filter the ripple of the HF link current completely; there is a dc current ripple in HVDC currents that has the same frequency with HF link current.

Fig.7 gives output voltage waveforms of all the SMs with different modulations in the SST. There is no phase-shift angle for square modulation between different sub modules in the same arm.

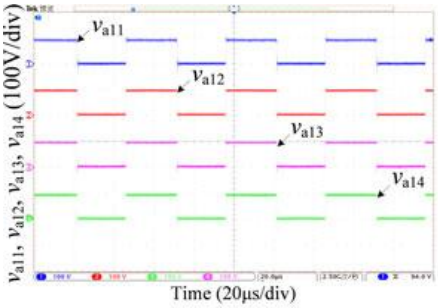


Fig.7. Output voltage waveforms of all the SMs in SST

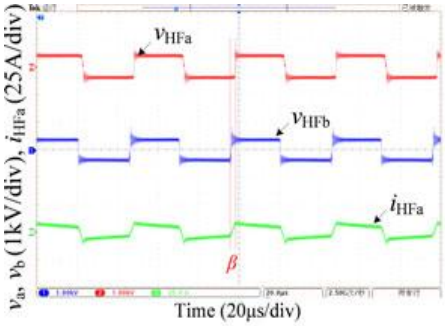


Fig.8. HF link voltage and current waveforms in SST

Fig.8 gives HF link voltage and current waveforms with square modulation in the SST. It is confirmed that, for the square modulation, v_a and v_b are high-frequency ac waves with 20-kHz frequency, and there is a phase-shift angle between v_a and v_b. However, the voltage and current are two-level waves for square modulation.

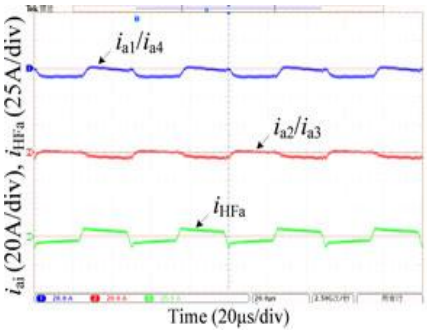


Fig.9 gives arm current waveforms for square modulations in the SST. It is confirmed that all the arm currents are also high-frequency ac waves with 20-kHz frequency that are similar to HF link currents, however, there is a dc bias. The arms 1 and 4 have the same current, the arms 2 and 3 have the same current, the arms 1/4 and 2/3 are having the complementary currents.

VI. CONCLUSION AND FUTURE SCOPE

This paper presents a detailed theoretical analysis and simulation verification of HF link modulation for the SST, especially the performance of SQM is analyzed and simulated. From the theoretical and simulation results, the SQM is having higher transmission power ability but has the higher circulating power. Due to the circulating power SQM has low power factor. SQM always has the best switching performance, especially all the turn ON switching behaviors of the SST with SQM are soft switching, which can decrease power loss. Apart from that, because of zero phase-shift angles between different sub modules in SQM, the voltage balance of the dc capacitor is achieved easily and the control is also simple. The SQM will be the best scheme for the MMC-based dc/dc converter to increase power transfer capacity and efficiency. The MMC based SST can also be scaled to 1100KV transmission voltages and tens of Giga watts of power in near future with the availability of semiconductors and efficient control methods.

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Design and Architecture of High Throughput Even Part CSDA

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Abstract— This work offers a low-cost, high-throughput multi standard transform (MST) core that supports MPEG-1/2/4 (8 8), H.264 (8 8, 4 4), and VC-1 (8 8, 8 4, 48, 44) transformations. EIGHTH PART Common sharing distributed arithmetic (CSDA) combines factor sharing and distributed arithmetic sharing approaches to reduce the number of adders while allowing for high hardware sharing. In comparison to the direct implementation method, this results of a reduction in adders in the proposed MST. The suggested MST core offers an eightfold operating frequency throughput rate thanks to its eight parallel computation pathways. As a result, the CSDA-MST core achieves a high throughput rate while still allowing for multi-standard transformations at a reasonable cost.

I. INTRODUCTION

1.1 GENERAL:

H.264 and VC-1 are known conventional video compression techniques. The VC-1 codec is designed to achieve state-of-the-art compressed video quality at bit rates that may range from very low to very high [1]. For high quality video, The codec justifies easily and handle 1920 pixel × 1080 pixel representation at 6 to 30 megabits per second (Mbps). VC-1 can handle the higher resolutions like 2048 pixels × 1536 pixels for digital videos, and of a maximum bit rate of 135 Mbps. For case study consider example of minimum bit rate video like as 160 pixel × 120 pixel process at 10 kilobits per second (Kbps) for modem design. The main function of VC-1 introduces a block-based motion compensation and spatial transform scheme also familiar to used in another video compression justifications since MPEG-1 and H.261. However, VC-1 includes a number of innovations and optimizations that make it distinct from the basic compression scheme, resulting in excellent quality and efficiency [1-3]. This reduces complexity and provides greater flexibility to device manufacturers. .

II. EXISTING SYSTEM

A conventional system consist of research has been conducted to efficiently combine and implement the transform units for multiple codec's. Some of cases research is focused on the design of multi-quantized unit. Among the multiple-transform units, a unified Inverse Discrete Cosine Transform (IDCT) architecture to support five standards (such as, AVS, H.264, VC-1, MPEG-2/4 and JPEG) is presented [1]. The authors in offer an area efficient architecture to perform a DCT-based transform for JPEG, MPEG-4, VC-1 and H.264 using delta mapping [3]. The design is an IDCT and IQ circuit for H.264, MPEG-4 and VC-1. The MJPEG standard defines quantization as the division operation of the DCT coefficient coming from the transform unit by the corresponding Q value (specified by the quantization matrix). In this work proposed the Q-matrices uses facilitates the allocation of more bits for the representation of coefficients which are allowed by MJPEG.

The main problem is that so inconvenient between the video devices standard for intercommunications, thus video codec supporting all standards are more applicable and more attractive. So, low cost very large scale integration (VLSI) architecture is preferred for multi standard inverse Discrete Cosine transform. It is used in multi standard decoder of MPEG-2, MPEG-4 ASP, and VC-1 [4] .Two circuit share strategies, factor share (FS) an adder share (AS) are applied to the inverse transform architecture for saving its circuit resource. In this work improved the operational speed by use Pipelined stages for Multistandard inverse transform.

Here considered hierarchical prediction structures are used for temporal scalability with several layers. Hierarchical prediction structures increasing the coding effectives and the quality and spatial scalable coding. To improve the coding efficiency inter-layer prediction of motion and residual need of spatial scalable and quality scalable coding [2]. The concept of key pictures for efficiently controlling the drift for packet-based quality scalable coding with hierarchical prediction structures. Single motion compensation loop decoding[5] for spatial and quality scalable coding providing a decoder complexity close to that of single-layer coding.[4]

III. PROPOSED SYSTEM

The proposed CSDA algorithm combines the FS and DA techniques. By expanding the coefficients matrix at the bit level [5]., In FS method initially each coefficient at same factor. The DA method consists of the same combination at the input among each coefficient position. In a matrix inner product, an example of the proposed CSDA algorithm is as follows: the suggested CSDA incorporates the FS and DA approaches. [5]. The FS technique is used first to find elements that can improve hardware resource sharing capabilities, with hardware resource defined as the number

of adders used.. Next, the DA method is used to find the shared coefficient based on the results of the FS method. The suggested CSDA circuit will come after the adder-tree circuits. As a result, the CSDA approach seeks to limit the number of nonzero items to a minimum. The number of adders in the CSDA loop is estimated and compared using the CSDA shared coefficient.

The proposed 2-D CSDA-MST core is made up of two 1-D CSDA-MST cores (Core-1 and Core-2) with a memory that is transposed (TMEM). The word lengths for each arithmetic, MUX, and register in Core-1 and Core-2 are different, and the TMEM is designed with sixty-four 12-bit registers, where the output data from Core-1 can be transposed and fed into Core-2.. Each core contains four pipeline stages: two in the CSDA circuit's even and odd parts, and two in the ECATs. As a result, the proposed 2-D CSDA-MST core has a delay of 16 clock cycles (= 4 + 8 + 4), and when 8 pixels are input, the TMEM executes transposed operation after 12 clock cycles (= 4 + 8).

Supporting MPEG-1/2/4, H.264, and VC-1 MSTs, the CSDA-MST core provides great performance, a high throughput rate, and a low-cost VLSI design. The suggested CSDA approach effectively reduces the number of adders and MUXs in the MST core With only 30 k logic gates, it can support the digital cinema format (4928 2048@24 Hz). This technique will help fulfil the expanding high-resolution demands and future needs, as visual media technology has grown rapidly.

IV. PROPOSED 2-D CSDA-MST CORE DESIGN

We introduces the proposed 2-D CSDA-MSTcore implementation. Neglecting the scaling factor, the onedimensional(1-D) eight-point transform can be defined asfollows

$$\begin{bmatrix} Z_0 \\ Z_1 \\ Z_2 \\ Z_3 \\ Z_4 \\ Z_5 \\ Z_6 \\ Z_7 \end{bmatrix} = \mathbf{C} \cdot \begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{bmatrix}$$

Where,

$$\mathbf{C} = \begin{bmatrix} c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 & c_4 \\ c_1 & c_3 & c_5 & c_7 & -c_7 & -c_5 & -c_3 & -c_1 \\ c_2 & c_6 & -c_6 & -c_2 & -c_2 & -c_6 & c_6 & c_2 \\ c_3 & -c_7 & -c_1 & -c_5 & c_5 & c_1 & c_7 & -c_3 \\ c_4 & -c_4 & -c_4 & c_4 & c_4 & -c_4 & -c_4 & c_4 \\ c_5 & -c_1 & c_7 & c_3 & -c_3 & -c_7 & c_1 & -c_5 \\ c_6 & -c_2 & c_2 & -c_6 & -c_6 & c_2 & -c_2 & c_6 \\ c_7 & -c_5 & c_3 & -c_1 & c_1 & -c_3 & c_5 & -c_7 \end{bmatrix}$$

The eight-point transform for MPEG-1/2/4, H.264, and VC-1 standards can use the same mathematicderivation because the eight-point coefficient structures are the same. The 1-D eight-point transform in (8) can be separated into even and odd two-four-point transforms, Ze and Zo,

as described in (9) and (10), respectively, based on the symmetry property.

$$\mathbf{Z}_e = \begin{bmatrix} Z_0 \\ Z_2 \\ Z_4 \\ Z_6 \end{bmatrix} = \begin{bmatrix} c_4 & c_4 & c_4 & c_4 \\ c_2 & c_6 & -c_6 & -c_2 \\ c_4 & -c_4 & -c_4 & c_4 \\ c_6 & -c_2 & c_2 & -c_6 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_3 \end{bmatrix} = \mathbf{C}_e \cdot \mathbf{a}$$

$$\mathbf{Z}_o = \begin{bmatrix} Z_1 \\ Z_3 \\ Z_5 \\ Z_7 \end{bmatrix} = \begin{bmatrix} c_1 & c_3 & c_5 & c_7 \\ c_3 & -c_7 & -c_1 & -c_5 \\ c_5 & -c_1 & c_7 & c_3 \\ c_7 & -c_5 & c_3 & -c_1 \end{bmatrix} \begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} = \mathbf{C}_o \cdot \mathbf{b}$$

Where

$$\mathbf{a} = \begin{bmatrix} x_0 + x_7 \\ x_1 + x_6 \\ x_2 + x_5 \\ x_3 + x_4 \end{bmatrix}, \quad \mathbf{b} = \begin{bmatrix} x_0 - x_7 \\ x_1 - x_6 \\ x_2 - x_5 \\ x_3 - x_4 \end{bmatrix}.$$

The even part of the operation in (10) is the same as thatof the four-point H.264 and VC-1 transformations. Moreover,the even part **Z***e* can be further decomposed into even and oddparts: **Z***ee* and **Z***eo*

$$\mathbf{Z}_{ee} = \begin{bmatrix} Z_0 \\ Z_4 \end{bmatrix} = \begin{bmatrix} c_4 & c_4 \\ c_4 & -c_4 \end{bmatrix} \begin{bmatrix} A_0 \\ A_1 \end{bmatrix} = \mathbf{C}_{ee} \cdot \mathbf{A}$$

$$\mathbf{Z}_{eo} = \begin{bmatrix} Z_2 \\ Z_6 \end{bmatrix} = \begin{bmatrix} c_2 & c_6 \\ c_6 & -c_2 \end{bmatrix} \begin{bmatrix} B_0 \\ B_1 \end{bmatrix} = \mathbf{C}_{eo} \cdot \mathbf{B}$$

Where,

$$\mathbf{A} = \begin{bmatrix} a_0 + a_3 \\ a_1 + a_2 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} a_0 - a_3 \\ a_1 - a_2 \end{bmatrix}.$$

Design Environment Enhancements

With the breadth of advances and capabilities that the Virtex®-6 and Spartan®-6 programmable devices deliver coupled with the access provided by the associated targeted design platforms, it is no longer feasible for one design flow or environment to fit every designer's needs. System designers, algorithm designers, SW coders, and logic designers each represent a different user-profile, with unique requirements for a design methodology and associated design environment. Instead of addressing the problem in terms of individual fixed tools, Xilinx targets the required or preferred methodology for each user, to address their specific needs with the appropriate design flow. At this level, the design language changes from HDL (VHDL/Verilog) to C, C++, MATLAB® software, The design abstraction moves up from the block or component level to the system level in these higher-level languages, which are more often employed by these designers. The end result is a methodology and a complete design pipeline that caters to each user profile and includes design conception, implementation, and verification.. The design abstraction

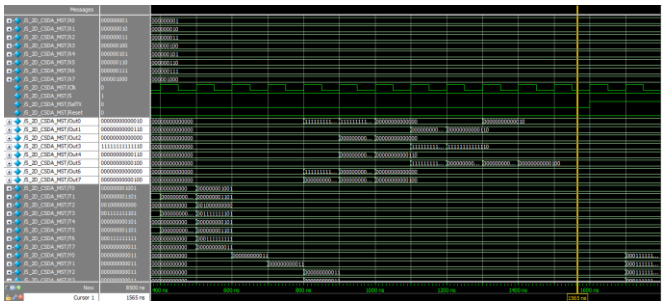
moves up from the block or component level to the system level in these higher-level languages, which are more often employed by these designers. The end result is a methodology and a complete design pipeline that caters to each user profile and includes design conception, implementation, and verification.To completely comprehend the user profile of a "logic designer," one needs analyse the varied degrees of knowledge represented by this demography, which is indicative of the problem's complexity. The "push-button user," who wants to complete a design with no effort or understanding, is the most basic category in this profile.

The push-button user just needs “good-enough” results. Contrastingly, more advanced users want some level of interactive capabilities to squeeze more value into their design, and the “power user” (the expert) wants full control over a vast array of variables. Add the traditional ASIC designers, tasked with migrating their designs to an FPGA (a growing trend, given the intolerable costs and risks posed by ASIC development these days), and clearly the imperative facing Xilinx is to offer targeted flows and tools that support each user's requirements and capabilities, on their terms. The most recent release of the ISE Design Suite includes numerous changes that fulfil requirements specifically pertinent to the targeted design platform. The new release features a complete tool chain for each top-level user profile (the domain-specific personas: the embedded, DSP, and logic/connectivity designers), including specific accommodations for everyone from the push-button user to the ASIC designer.

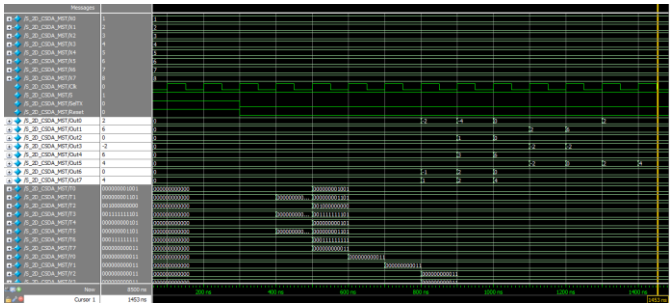
The closer integration of embedded and DSP flows allows for a more seamless integration of designs containing embedded, DSP, IP, and user blocks in a single system. The new ISE Design Suite allows designers to target specific areas of their designs to increase productivity and assist customers better manage the complexity of their designsBy simply picking a design goal in the setup, you can improve speed, performance, or power. The tools then do particular optimizations to assist in achieving the design aim. Furthermore, the ISE Design Suite has significantly faster place-and-route and simulation run times, resulting in 2X faster compile times for users. Finally, Xilinx has implemented the FLEXnet Licensing method, which uses a floating licence to follow an application.

Verilog A Hardware Description Language (HDL) is a programming language for describing hardware (HDL). A Hardware Description Language (HDL) is a language for describing digital systems, such as a computer or a computer component. A digital system can be described on numerous levels. An HDL might, for example, describe the switch level arrangement of wires, resistors, and transistors on an Integrated Circuit (IC) device.. It could also refer to the logical gates and flip flops in a digital system, which is referred to as the gate level. The registers and the transfers of information vectors between registers are described at a higher level. The Register Transfer Level is what it's called (RTL). All of these levels are supported by Verilog. This handout, however, only covers the parts of Verilog that enable the RTL level.

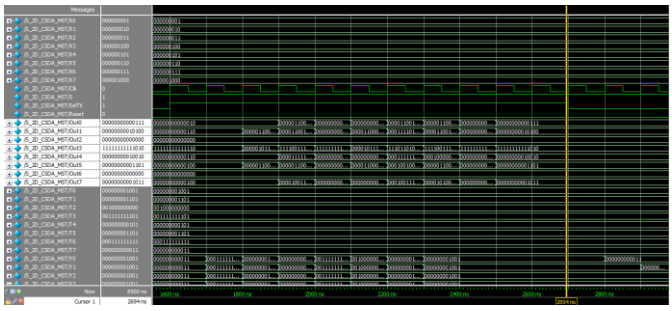
Top module 2D CSDA_MST CORESelTx&Rst=0:



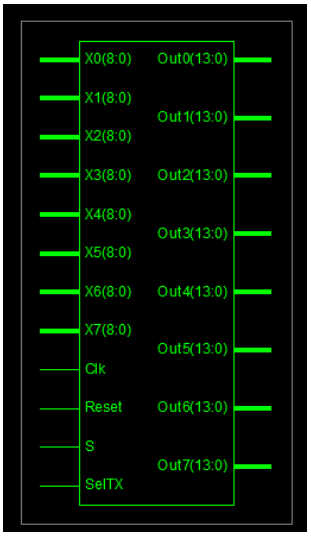
Top module 2D CSDA_MST CORESelTx&Rst=0 Decimal:



Top module 2D CSDA_MST CORESelTx=1:



RTL SCHEMATIC:



DEVICE UTILIZATION SUMMARY

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	704	7,168	9%	
Number of 4 input LUTs	2,048	7,168	28%	
Logic Distribution				
Number of occupied Slices	1,239	3,584	34%	
Number of Slices containing only related logic	1,239	1,239	100%	
Number of Slices containing unrelated logic	0	1,239	0%	
Total Number of 4 input LUTs	2,158	7,168	30%	
Number used as logic	2,048			
Number used as a route-thru	110			
Number of bonded IOBs	188	221	85%	
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	23,799			
Additional JTAG gate count for IOBs	9,024			

V. CONCLUTION

Supporting MPEG-1/2/4, H.264, and VC-1 MSTs, the CSDA-MST core provides great performance, a high throughput rate, and a low-cost VLSI design. The suggested CSDA approach effectively reduces the number of adders and MUXs in the MST core. The CSDA-MST core has a throughput rate of 1.28 G-pels/s and can accommodate (4928 2048@24 Hz) digital cinema format with only 30 k logic gates, according to the results. This technique will help fulfil the expanding high-resolution demands and future needs, as visual media technology has grown rapidly.

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A Comparative Analysis of Involvement of Urban and Rural Physicians in Unethical Drug Promotion Practices in Madhya Pradesh

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Abstract— Introduction: Indian Pharmaceutical Industry has a noticeable position and known for its rapidly creating presence in the Worldwide Drugs industry. India positions third to the extent drug creation by volume and fourteenth by value. India is the greatest provider of generic meds from one side of the planet to the other and furthermore supplies 62% of the worldwide necessities of vaccines. In drug promotion the consumer isn't the king yet the components of promotion are more centered on convincing the doctors for more prescriptions. The Multinational, National and local pharmaceutical companies compete each other aggressively for getting control over a larger share of market, offering me too drugs, pushing high value brands, promoting irrational drug combinations and to earn higher profits the stakeholders does not hesitate to adopt the unethical drug promotion practices. The pharmaceutical companies put unendurable stress on sales representatives to accomplish higher sales target. The physicians also understand the greedy intentions of the pharmaceutical companies and take advantage by active involvement in negotiation on business dealings.

This outcome is the unscrupulous drug promotion practices by pharmaceutical companies and doctors to procure a huge benefit at the expense of patient care. Pharmaceutical Companies and the doctor's connection are getting ravenous and unholy. The pharmaceutical companies are aggressively promoting the drugs in urban and rural market and do not hesitate to elevate the medications to the non-qualified medical care staff for deals. The study aims to investigate and compare the involvement of urban and rural physicians in unethical drug promotion practices in Madhya Pradesh.

Methods: The primary data is collected with the help of a structured questionnaire. The purposive sampling is used in which the 100 physicians are chosen for study those are open to discuss about the unethical promotion practices. Out of which 50 physicians are working in urban areas and 50 are working in rural areas of Madhya Pradesh state.

Results: The mean scores of involvement of urban physicians in unethical drug promotion practices are comparatively higher than the mean scores of rural physicians.

Conclusion: The urban physicians are more involved in unethical drug promotion practices comparatively to rural physicians.

Index Terms—Drug Promotion, Pharmaceutical Marketing, Pharmaceutical Promotion, Unethical drug promotion

I. INTRODUCTION

Indian pharmaceutical has a prominent position and known for its quickly developing presence in the Global Pharmaceuticals. India positions third as far as drug creation by volume and 14th by value. India is the biggest supplier of generic medications all around the world and also supplies 62% of the global requirements of vaccines. More than 80% of the antiretroviral drugs utilized all around the world to battle AIDS (Acquired Immune Deficiency Syndrome) are provided by Indian drug firms. The domestic pharmaceutical industry incorporates a network of more than 3000 pharmaceutical companies and more than 10500 manufacturing units. As indicated by the Indian Economic Survey 2021, the homegrown market is required to develop 3x in the following decade. India's homegrown drug market is assessed at US$ 41 billion in 2021 and liable to arrive at US$ 65 billion by 2024 and additionally extend to arrive at ~US$ 120-130 billion by 2030.

In pharmaceutical promotion the consumer is not the king but the elements of promotion are more focused on persuading the physicians for more prescription. The medical representatives of domestic and multinational pharmaceutical companies through detailing and sharing the scientific information promote their drugs and doctors prescribe the medicines to the patients. Poor regulation, work stress of MRs, offering “me too “products and introduction of many fixed dose combination drugs, pushing high-cost brands, the pharmaceutical companies compete each other fiercely to obtain the larger share of the market.

This results in unethical drug promotion practices by pharmaceutical companies and physicians to earn a gigantic profit at the cost of patient care. Pharmaceutical companies and the physician’s relation are getting greedy and unholy. Gadre and Shukla (2016) also depicted the influence of pharmaceutical promotional malpractices of companies on physicians prescription and the active involvement of physicians demanding incentives, sponsorship and benefits to boost business. The pharmaceutical companies are aggressively targeting the urban and rural market and often hesitate to promote the drugs to the non-qualified health care personnel for sales. The study aims to compare the involvement of urban and rural physicians in unethical drug promotion practices.

II. OBJECTIVE

The objective is to compare the average scores of unethical drug promotion practices of physicians working in urban and rural areas of Madhya Pradesh.

III. RESEARCH METHODOLOGY

The study was undertaken in Madhya Pradesh state and the physicians working in urban areas are chosen from Indore, Bhopal, Jabalpur and Gwalior cities and the physicians working in rural areas are chosen from the rural areas of the state. Primary data was collected with the help of structured questionnaire and the physician's responses are recorded. The questionnaire consists of 16 questions designed to measure the unethical promotional practices of physicians. As the data is sensitive in nature, a sample of 100 physicians was chosen purposefully who agreed to discuss about the unethical drug promotional practices of physicians in the state. Out of 100 physicians, 50 physicians are taken from urban areas and 50 physicians are selected from the rural areas. The responses in the form of statements are recorded with the help of 5 point Likert scale ranging from 5= "strongly agree" to 1= "strongly disagree".

IV. STATISTICAL ANALYSIS OF DATA

For comparing the means scores of unethical drug promotional practices of urban and rural physicians, independent sample t test is used and tested at 0.01 percent level of significance. The data is analyzed with the help of SPSS (statistical package for social sciences version 20).

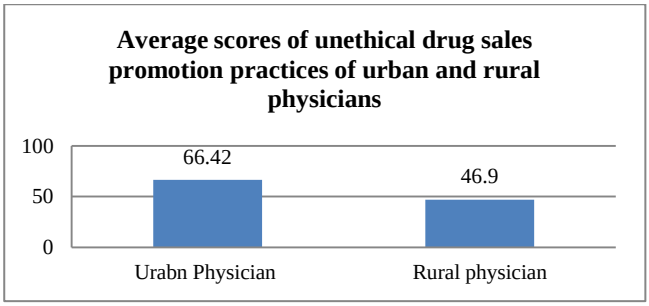
A. HYPOTHESIS

Null (H_0): There is no significant difference in the average scores of unethical drug promotion practices of physicians working in urban and rural areas.

Table: t value showing the average scores of unethical drug sales promotion practices of urban and rural physicians

Category	Sample size (N)	Average scores	standard deviation	"t" score	Degree of freedom	Remarks
Urban Physicians	50	66.42	5.08	17.18	98	Significant
Rural Physicians	50	46.9	6.22			

** Significant at 0.01 level



B. INTREPRETATION

The objective was to compare the average scores of unethical drug sales promotion practices of physicians of urban and rural areas. There were two categories of physicians, namely Urban Physicians and Rural physicians. The data were examined with the help of independent t test and the outcomes are presented in the above table.

From the above table it is apparent that the t value is 17.18 which is significant at 0.01 level of significance at 98 degree of freedom. It shows that the average scores of unethical drug promotion practices of physicians working in urban and rural areas vary significantly. Thus the null hypothesis that there is no significant difference between the average scores of unethical drug promotion practices of physicians working in urban and rural areas is not accepted. Further, the average score of unethical drug promotion practices of urban physicians is 66.42 which is altogether significantly higher than the rural physicians whose average scores of unethical drug sales promotion practices is 46.90.

C. FINDINGS

It may therefore be said that the urban physicians were discovered to be more associated with unethical drug promotion practices comparatively to rural physicians.

V. DISCUSSIONS

The special promotional instruments are presented to physicians by the sales representatives of pharmaceutical companies. The sales representatives meet the doctors in their private clinics, hospitals and during meetings and advance their brands. The density of populace is high in urban areas and the quantity of high qualified physicians with different specialties having high business potential serving patients in their private facilities and hospitals. These potential physicians are the primary target of pharmaceutical companies and the aggressive and deceptive promotional strategies are utilized to impact the prescription behavior of physicians to gain huge sales to earn massive profits.

There are in excess of 1300 pharmaceutical companies working in urban areas and offering me too brands, fixed dose combination drugs and pushing high cost brands to doctors for prescription. To procure a larger share of the market and to excel in the competition the companies move from moral to dishonest advancement of drugs.

The selling tactics and the promotion trends has changed from giving medical scientific information through detailing and providing literature to generation of business by whatsoever the means or any practice . The ethical conduct is overlooked and ignored which was done earlier

and now the total focus is to generate more and more business.

The urban doctors having various specialties to fame had a more extensive selection of brands of same drug ingredient which are produced by numerous drug organizations. The profit intentions of pharmaceutical companies are well understood by the doctors and the dealings and negotiations on business is made by these doctors with the companies. The doctors center on those companies who satisfy their interest. The job which was before played by drug organizations inciting doctors are switched and now the doctors are actively demanding costlier gifts and individual help and are the initiators of the business transactions.

Physicians procure benefits by selling the medications straightforwardly to patients. They get the drugs/vials/infusions straightforwardly from propaganda organizations or from the drug companies in lesser cost contrasted with retail price and sell those products to patients in hospitals and in their private facilities.

Doctors/hospitals additionally constrain the patients to buy meds from close by chemists and drug stores in the hospitals and get commission from such physicists on giving business. They by and large make agreement for the common advantage.

In rural regions, the thickness of populace is low. The rural doctors are RMP (Rural Medical Practitioners), BAMS, BUMS, and the quacks; the GP expert relieving the overall sicknesses of patients has poor business potential. These doctors demand for additional samples, medical devises, small gifts and low month to month cash sum for prescription. These rural doctors are auxiliary to drug organizations because of feeble business potential.

The propaganda cum distribution organizations ordinarily focus on these RMP, BAMS, BUMS, specialists and initiate them to endorse allopathic medications principally antibiotics and steroids which are not needed for general kind of sicknesses like cold and influenza and in everyday infections. Because of absence of information these provincial doctors endorse more antibiotics and steroids to general patients which could make them antibiotic resistant and could have contraindications.

MCI (Medical Council of India) has set down mandatory code of conduct for medical professionals' .The code portrays the set of principles for the doctors and their connection with pharmaceutical companies. These codes restrict the physicians to get any expensive blessings from any drug or unified medical services industry or through the salespeople. The medical professionals will not acknowledge any travel trips, excursions trips for themselves and for their relatives for going to any conference, seminars, CME (Continuous Medical education) programs. They ought not to accept any hospitality services like hotel stay nor will they acknowledge any money or financial awards from drug organizations.

VI. CONCLUSIONS

Despite various ethical regulations by MCI on drug promotion practices, the ethics are continuously violated and overlooked at the ground level by the physicians working in urban and rural regions of Madhya Pradesh. The study shows the urban physicians are more associated with the unethical drug promotion practices than the physicians working in rural regions of Madhya Pradesh.

VII. RECOMMENDATIONS

Strict action should be taken and punitive measures against such practitioners violating the rules such as censure or removal from registration temporarily or permanently. Effective monitoring system must be introduced for monitoring and reporting of any unethical promotion of drugs.

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Vehicles License Detection using QR Code

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Abstract— We proposed a system in which the work of traffic police and driver (user) is simplified. In this system the driver will register to RTO services and the license will be issued to the user. The RTO officer will generate a QR code attached to the license card for user. The RTO officer will generate a QR code in the driving license can be used by traffic control authorities in case of a default. The QR code has all details about you which the traffic control authorities have. It has the details like name, address, age, phone number, fingerprint, digital signature, photo etc.

Index Terms— Windows XP/7/10, JavaScript, Html, Flask Framework, SQLite, Anaconda prompt, QR Code.

I. INTRODUCTION

In [1] this paper we have different modules in which they store different information and having different service. In RTO it has process for registration of vehicle, their documents data all are stored in database in which they access from here. They provide QR code for each and every new license with respect to the age of the customer. Now a days people who are below 18 are making the use of fake license by editing their details with the original license details, this is the most offensive crime going in the cities and leads to accidents and also violating traffic rules. Here comes the QR code provided on the license in to play, the traffic police should have a scanner app so, that he can scan the QR code then immediately he will be able to see the details of the user and make sure to match the both details, if the details are not matching then the user is using a fake license and he will be charged and also gives them counselling along with their parents. This paper makes traffic police work easy by scanning QR code.

In this user will register to RTO services like name, address, age, phone no., vehicle type, badge number etc.RTO service member will login and then produce a QR codewith that user information and can scan whenever needed. After scanning the QR code traffic police can to know all the details about the driver, using this fake user can be easily identified. This makes traffic police work easy in reducing fake users license card.

II. LITERATURE SURVEY

Komal chorhgade, Piyush Dahiwele, Prof. Prajakta pise (2018) [2] has developed RTO AUTOMATION USING QR CODE, in this project there are different modules that are used to store information. In RTO it had process of registration of driving license, their documents data to be stored in the database in which they access from that database whenever required.

It is used to provide the feature for detecting of the fake user. Administrator had rights to enter and process the data of applicants. Any person who has been authorized by the administrator can utilize the services of his system. An authorized user should have a user name and a password.

Prof. Chandrakant Umarani et al., "Smart RTO Web and Android Application. In "Smart RTO Web and Android Application" [3] it describes smart RTO & web application consist of web application for RTO administrator and the android application for the user. The user has to register for the services like insurance, license & RC book. If the traffic police caught the driver and asks for the license, insurance and vehicle documents the driver had to tell him the license number, insurance number manually and the traffic police will enter the details in his mobile app and the data stored on the server will be fetched regarding the documents.It influenced by RTO management system. This information was stored in database at server through on inline registration and server-side end is in PHP.

On client side an android application was provided to police. After police logins into the system was able retrieve vehicle and license related information from the RTO database. If authentication fails, the information is provided to the police to retry else information about the use is displayed.

Manjunath S. Patil, Basavaraj K. Madagouda, Vinodh C Desai (2013) has developed E-RTO MANAGEMENT SYSTEM. [4] The author developed a system which provides services driving licenses. Administrator is the power user; he has power to verify the data entered and also process the data and he can provide access for the authorized users to utilize the services of the system.

III. PYTHON

What is Python? We may have found this book because we want to learn to program but don't know anything about programming languages. Or we may have heard of programming languages like C, C++, C#, or Java and want to know what Python is and how it compares to "big name" languages.

Python concepts

Python is one of the best languages available and that is why it's a great one to start programming with.

• Open-source general-purpose language.

• Object Oriented, Procedural, Functional

• Easy to interface with C/ObjC/Java/Fortran

• Easy to interface with C++ (via SWIG)

• Great interactive environment

Python is a high-level, interpreted, interactive and object-oriented scripting language. Python is designed to be highly readable. It uses English keywords frequently where as other languages use punctuation, and it has fewer syntactical constructions than other languages.

3.1 Python libraries

There are 20 libraries that we use the most. Requests, Scrapy, wxPython, Pillow, SQLAlchemy,

BeautifulSoup, Twisted, NumPy, SciPy, Matplotlib,

Pygame, Pyglet, pyQT, pyGtk, Scapy, pywin32, Natural Language Toolkit, nose, SymPy, IPython.

3.2 Python modules

Python allows us to store our code in files. In doing this, we are essentially defining our own modules, just like the modules defined already in the Python library.

To support this, Python has a way to put definitions in a file and use them in a script or in an interactive instance of the interpreter. Such a file is called a *module* definition from a module can be *imported* into other modules or into the *main* module.

3.3 Python Web Frameworks

A web framework is a code library that makes a developer's life easier when building reliable, scalable and maintainable web applications.

Why are web frameworks useful?

Frameworks make it easier to reuse code for common HTTP operations and to structure projects so other developers with knowledge of the framework can quickly build and maintain the application.

Frameworks provide functionality in their code or through extensions to perform common operations required to run web applications. These common operations include:

URL routing, HTML, XML, JSON, and other output format templating, Database manipulation, Security against Cross-site request forgery (CSRF) and other attacks, Session storage and retrieval.

Not all web frameworks include code for all of the above functionality. Frameworks fall on the spectrum from executing a single use case to providing every known web framework feature to every developer.

IV. IMPLEMENTATION OF VECHILE LICENSE DETECTION USING QR CODE

The Implementation of the paper design can be divided into two sections; Hardware and Software implementations.

4.1 Hardware Requirements

1. System : Pentium IV 2.4 GHz
2. Hard Disk : 100 GB
3. Monitor : 15 VGA Color
4. Mouse : Logitech
5. RAM : 1 GBs

4.2 Software Requirements

1. Operating System : Windows XP/7/10
2. Coding Language : JavaScript, Html
3. Development Kit : Flask Framework
4. Database : SQLite
5. IDE : Anaconda prompt

4.3 IMPLEMENTATION STEPS

- Start (Initial Stage).
- Enter the user details like Name, Address, Email Id, Contact Number etc.
- Register with given details of the user.
- And then login into the URL Page where QR code is obtained.
- Enter all the information into the cloud database.
- Then view the License obtained by the details of the user.
- And finally, logout of the page.
- Stop (final stage).

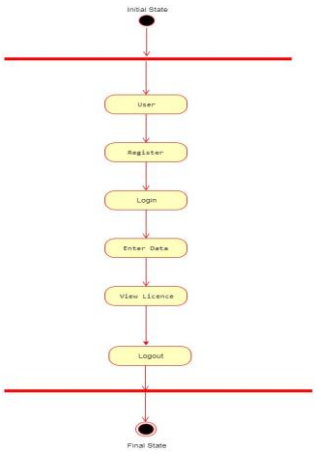

Figure 1: Flow Chart

The flow chart explains that how the user is created and registered using his personal details like fingerprint, digital signature, mobile number and the address of the user. Then login using the username and password. Then enter the data into the cloud data base. Then view the obtained license and then logout.

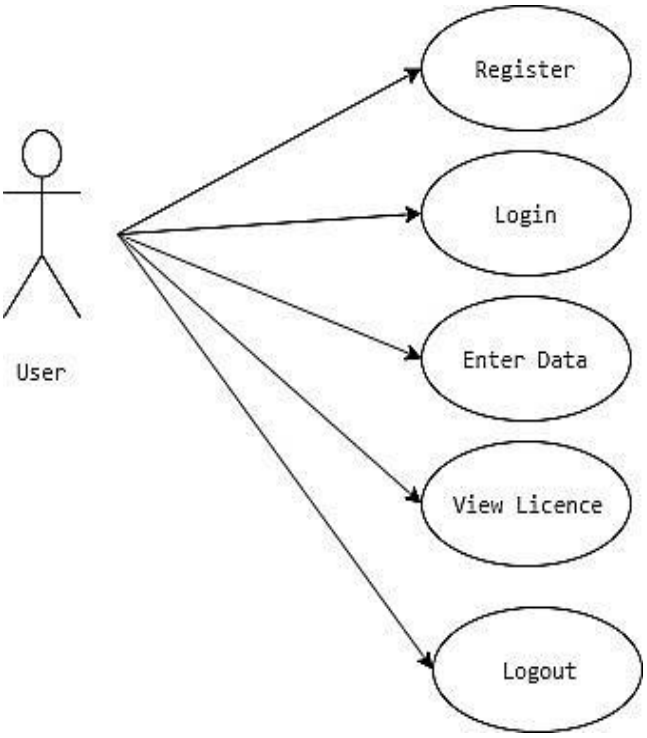

Figure 2: Use Case Diagram

The use case diagram at its simplest is a representation of a user's interaction with the system and depicting the specifications of a use case. A use case diagram can portray the different types of users of a system and the various ways that they interact with the system. This type of diagram is typically used in conjunction with the textual use case and will often be accompanied by other types of diagrams as well.

V. PROPOSED SOLUTION

- License card with QR code which can be easily scanned through the scanner app and every traffic police who are using smart phones can easily detect by scanning QR code.
- Considering the positive aspects of the QR, the proposed method if brought into actual practice will definitely prove to be a boon.
- The proposed project analyses the vehicle document tracking based on QR code. By using this application, it is not necessary to carry all the documents and license every time. Simply you have to carry QR code in your Smartphone.
- By using our system, the driver goes through the verification process through a reliable and efficient manner. QR code is being widely used for implanting messages such that people can easily use their Smartphone's to capture the code and gain relevant data from OR code reader.
- User can get QR code by simply registering with the system.
- In Future the QR Codes of Vehicle Owner is linked to Aadhaar Card.
- Any Person need to Purchase the New Vehicle need to Produce Aadhaar Card.
- Hence QR Codes and Aadhaar Card is linked which taken into consideration to Purchase new Vehicles depends on Size of Family Members .

VI. RESULTS AND DISCUSSIONS

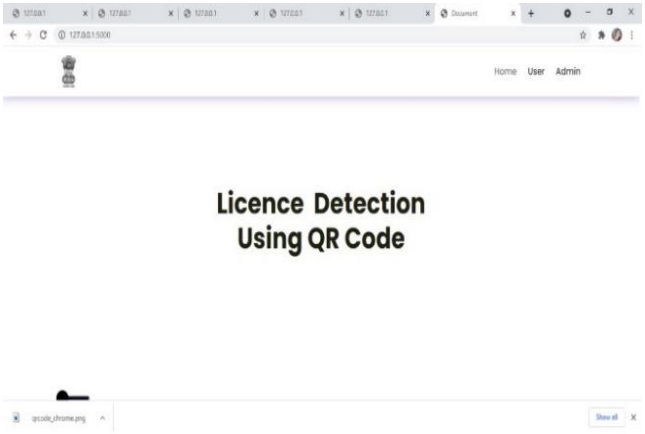

Figure 3: Home Page

This figure 3 shows the initial step that is home page.

After writing code in Python, we should write this code in Anaconda prompt and run then we a link by pasting this link in Google chrome we get the home page.

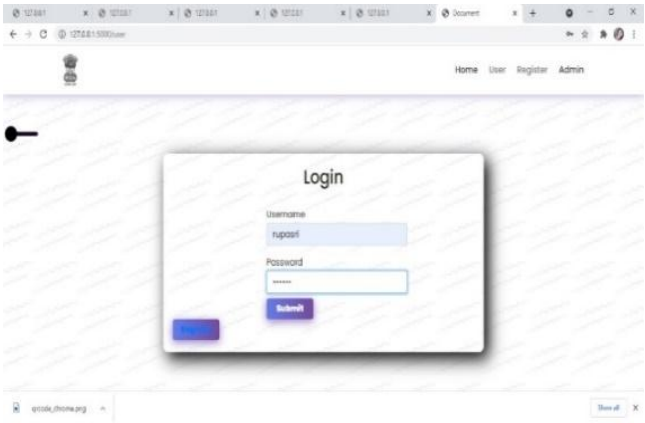

Figure 4: Login Page

The above figure 4 shows the second step for login into the page to insert the details like username and Password.

Figure 5: QR Code

The above figure 5 of QR code we get after entering the login details of username and password.

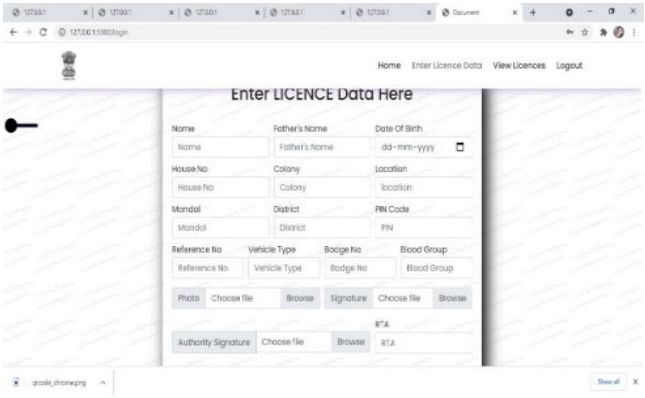

Figure 6: Registration Page

The above figure 6 shows the registration page for the user to enter details like name, address, passport size photo, Digital signature.

harika	venkat reddy	1999-10-03	macha bollaram	View
krishna sahith	sathyanarayana	2000-08-26	banswada	View
rupasri	venkat reddy	2000-01-28	patancheruvu	View
surya teja	yadagiri	1999-09-20	balanagar	View
sudha chandrika	P.Dakshina Murthy	1977-05-06	Gangasthan	View

Figure 7: Details of Users with unique QR code

After entering the details of the user for registration process we get the user details with a unique QR code for each member.

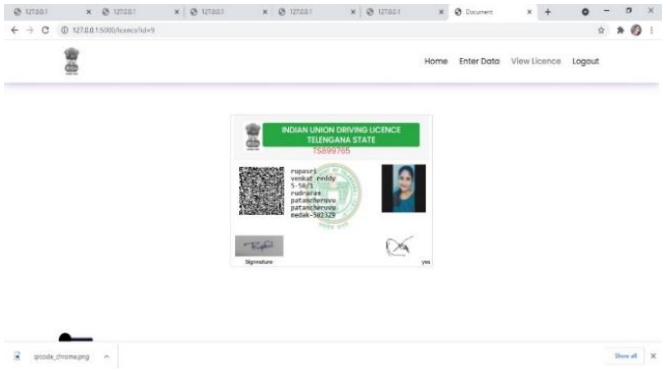

Figure 8: DRIVING LICENSE WITH QR CODE User 1

The figure 8 is obtained after entering all the details and the QR code prints along with the License.

After Creating user 1 by entering all the details of the user and then by registering the details saving it in the cloud base and attaching the QR Code to license and then by viewing we can see license along with QR code.

Figure 9: User 2

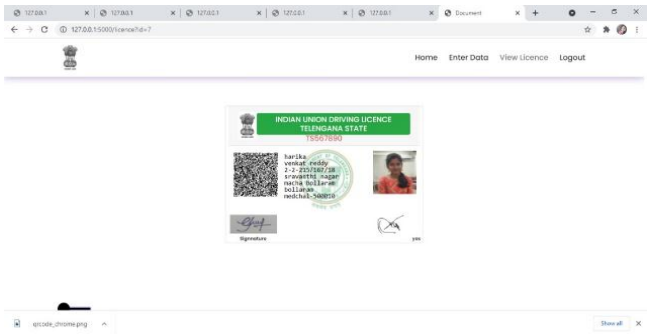

Figure 10: User 3

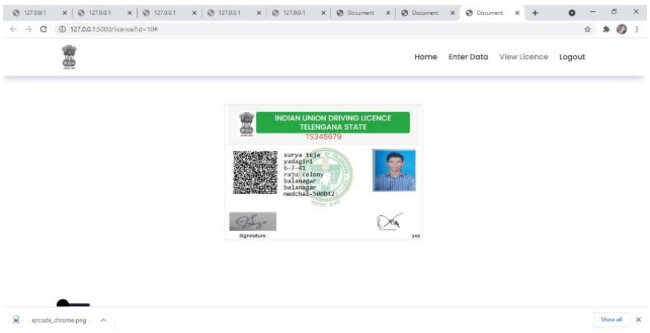

Figure 11: User 4

Figure 12: User 5

The above figures 9,10,11,12 shows the different users registered with different QR codes.

Similarly Creating user 2,3,4,5 by entering all the details of the user and then by registering the details saving it in the cloud base and attaching the QR Code to license and then by viewing we can see license along with QR code.

VII. CONCLUSION

Traffic police have to just scan QR code to see the license and reduces fake users. From this system we can also conclude that by using the scanning of QR code for obtaining the details of the user it is the faster method of reading the information from smart chip and also, we don't need any magnetic card readers that may cost around 1000-2000. Now-a-days most of the people use smart phones and the user can utilize the QR code as default with free of cost.

VIII. SCOPE FOR FUTURE WORK

It is not possible to develop a system that makes all the requirements of the user. User requirements keep changing as the system is being used. Some of the future enhancements that can be done to this system are:

1. As the technology emerges, it is possible to upgrade the system and can be adaptable to desired environment.

2. Based on the future security issues, security can be improved using emerging technologies like single sign-on.

IX. ACKNOWLEDGEMENT

Authors would like to thank ECE Department, CMR Technical Campus, Hyderabad, Telangana for providing necessary infrastructure and Lab Facilities to carry out the required work.

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Designing a Less Energy and Less-Size Shift Register for VLSI Circuit Using Pulsed Handles

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Abstract— This process solves the timing problem between pulsed latches by using multiple non-overlap postponed pulsed clock signals rather than the traditional single pulsed clock signal. This paper proposes a minimal-power and area-efficient shift register using pulsed latches. The architecture of the shift register is very simple. An N-bit shift register consists of series connected N data switch-flops. The rate from the switch-flop is less important compared to area and power consumption because there's no circuit between switch-flicks within the shift register. The region and power consumption are reduced by changing switch-flops with pulsed latches. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using CMOS process with. The suggested shift register saves area and power in comparison towards the conventional shift register with switch-flops. Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop. However, the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches.

Index Terms— Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.

I. INTRODUCTION

Lately, as how big the look data is constantly on the increase because of the popular for prime quality image data, the term entire shifter register increases to process large image data in image processing ICs. A picture-extraction and vector generation VLSI nick utilizes a 4K-bit shift register. A Ten-bit 208 funnel output LCD column driver IC utilizes a 2K-bit shift register. A shift register may be the fundamental foundation inside a VLSI circuit. Shift registers are generally utilized in many programs, for example digital filters, communication receivers, and image processing ICs [1]. A 16-megapixel CMOS image sensor utilizes a 45K-bit shift register. Because the word entire shifter register increases, the region and power use of the shift register become important design factors. The architecture of the shift register is very simple. An N-bit shift register consists of series connected N data switch-flops. The rate from the switch-flop is less important compared to area and power consumption because there's no circuit between switch-flicks within the shift register. The tiniest switch-flop is appropriate for that shift register to lessen the region and power consumption. Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop [2]. However, the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches. This paper proposes a minimal-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap postponed pulsed clock signals rather than the traditional single pulsed clock signal. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. Another option would be to insert clock buffers and clock trees to transmit rapid clock pulse having a small wire delay. However this boosts the area and power overhead.

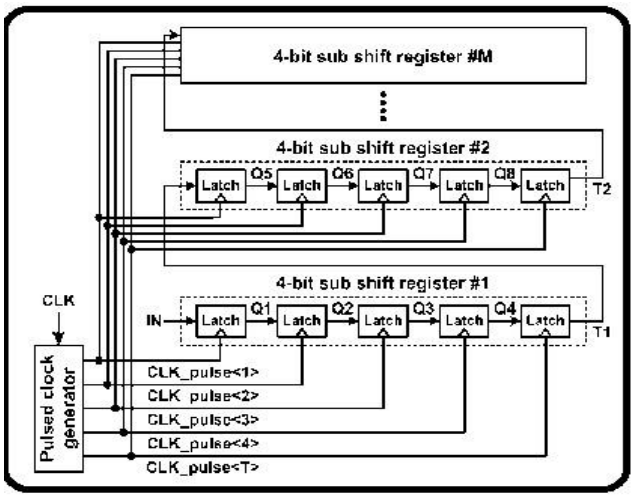

Fig.1.Block diagram of proposed shift register

II. PROPOSED METHOD

An expert-slave switch-flop using two latches could be changed with a pulsed latch composed of the latch along with a pulsed clock signal. All pulsed latches share the heart beat generation circuit for that pulsed clock signal. Consequently, the region and power use of the pulsed latch become nearly half of individuals from the master-slave switch-flop [3]. The pulsed latch is an attractive solution for small area and occasional power consumption. The pulsed latch can't be utilized in shift registers because of the timing problem. The shift register includes several latches along with a pulsed clock signal (CLK_pulse). The operation waveforms are the timing issue in the shifter register. The

output signal from the first latch (Q1) changes properly since the input signal from the first latch (IN) is constant throughout the clock pulse width. However, the second latch comes with an uncertain output signal (Q2) because its input signal (Q1) changes throughout the clock pulse width. One solution for that timing issue is to include delay circuits between latches. The output signal from the latch is postponed and reaches the following latch following the clock pulse. The output signals of the foremost and second latches (Q1 and Q2) change throughout the clock pulse width , however the input signals from the second and third latches (D2 and D3) become identical to the output signals of the foremost and second latches (Q1 and Q2) following the clock pulse. Consequently, all latches have constant input signals throughout the clock pulse with no timing problem happens between your latches. However, the delay circuits cause large area and power overheads. Another solution is by using multiple non-overlap postponed pulsed clock signals. The postponed pulsed clock signals are produced whenever a pulsed clock signal experiences delay circuits. Each latch utilizes a pulsed clock signal that is postponed in the pulsed clock signal utilized in its next latch. Therefore, each latch updates the information after its next latch updates the information. Consequently, each latch includes a constant input during its clock pulse with no timing problem happens between latches. However, this solution also requires many delay circuits. Inside a lengthy shift register, a brief clock pulse cannot via a lengthy wire because of parasitic capacitance and resistance. In the finish from the wire, the time pulse shape is degraded since the rising and falling occasions from the clock pulse increase because of the wire delay. An easy option would be to improve the time pulse width to keep the time pulse shape [4]. However, this lessens the maximum clock frequency. Another option would be to insert clock buffers and clock trees to transmit rapid clock pulse having a small wire delay. However, this boosts the area and power overhead. Furthermore, the multiple clock pulses result in the more overhead for multiple clock buffers and clock trees. The utmost clock frequency within the conventional shift register is restricted to simply the delay of switch-flops because there's no delay between switch-flicks. Therefore, the region and power consumption tend to be more important compared to speed for choosing the switch-flop. The suggested shift register uses latches rather than switch-flops to lessen the region and power consumption. In nick implementation, the SSASPL, the tiniest latch, is chosen. The initial SSASPL with 9 transistors is modified towards the SSASPL with 7 transistors by getting rid of an inverter to create the complementary data input (Db.) in the data input (D). Within the suggested shift register, the differential data inputs (D and Db.) from the latch range from differential data outputs (Q and Qi) from the previous latch [5]. The SSASPL uses the tiniest quantity of transistors (7 transistors) also it consumes the cheapest clock power because it features a single transistor driven through the pulsed clock signal. The SSASPL updates the information with three NMOS transistors also it supports the data with four transistors in 2 mix-combined inverters.

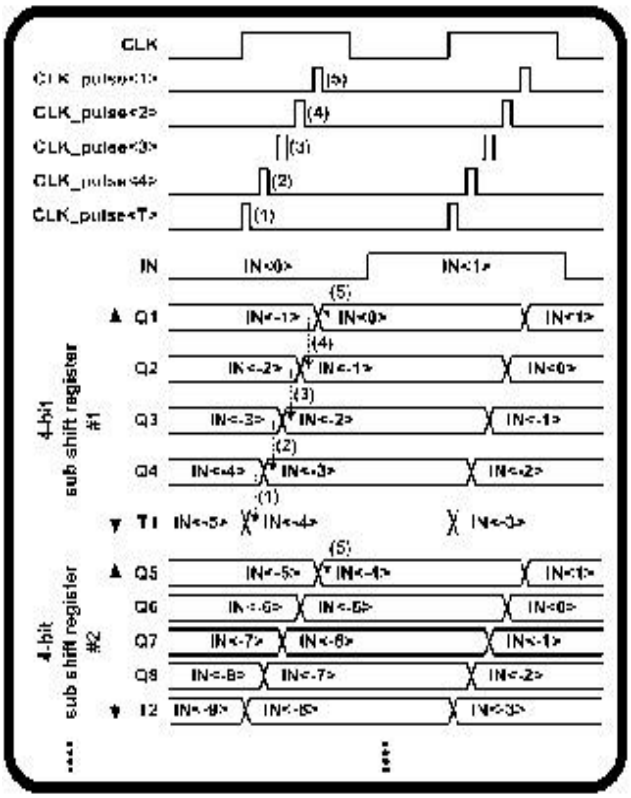

Fig.2.Proposed shift register waveform

CIRCUIT DIAGRAM:

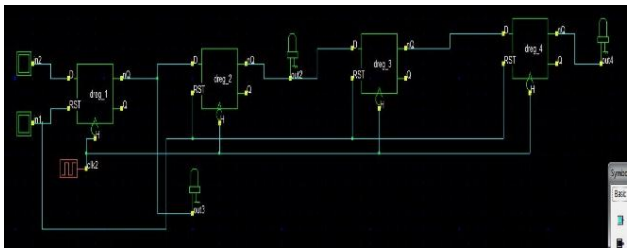

Fig : Pulsed Latch Circuit

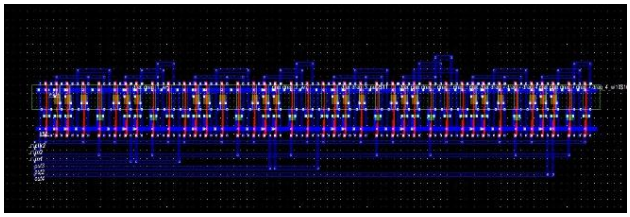

Fig : Lay Out

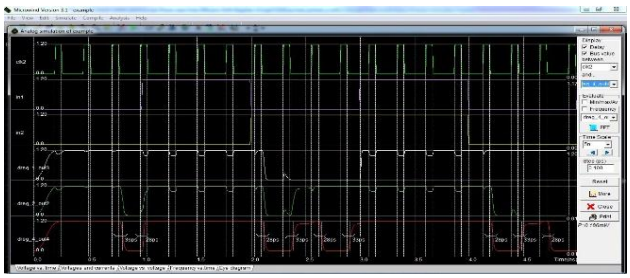

Fig: Result Wave Forms

III. CONCLUSION

Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop. However the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches.

A 256-bit shift register was fabricated utilizing a .18 CMOS process with. It consumes 1.2 maw in a 100 MHz clock frequency. This paper suggested a minimal-power and area-efficient shift register using pulsed latches. The suggested shift register saves 37% area and 44% power in comparison towards the conventional shift register with switch-flops. The shift register reduces area and power consumption by changing switch-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap postponed pulsed clock signals rather than just one pulsed clock signal. A small amount of the pulsed clock signals can be used by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches.

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Fractional Ordered Systems Stability through FOTF Viewer

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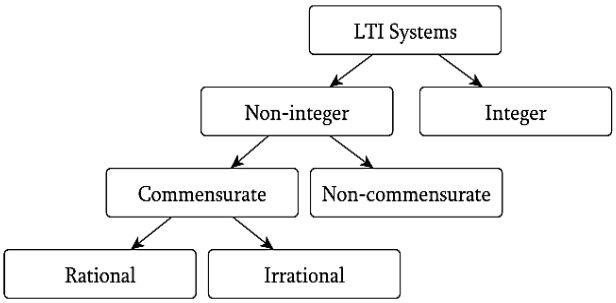
Abstract— In this work, we present the fractional ordered systems (FOS) with reference to transfer functions in time domain, frequency domain and to carry out the stability analysis of such systems. In time domain method, the analysis is carried out through step responses and for frequency domain method, the analysis is carried out through bode plots. As the stability of LTI integer ordered systems (IOS) differ from these fractional ordered systems, Matignon's stability theorem is used to analyze the stability of FOS. Matignon's stability theorem states that the fractional ordered transfer function G(s)=Z(s)/P(s) is stable if and only if the following condition is satisfied in σ-plane i.e., |arg(σ)|>qπ/2, where 'q' is the approximated fcarctional order. In this work, different transfer functions picked up from real-time applications is being presented and suitable analysis is carried out for mathematical simplication of such transfer functions using Pade approximation method, Hankel-norm approximation and validation for the responses through FOTF Viewer of MATLAB along with the stability analysis.

Index Terms— Fractional Ordered Systems, FOTF, FOMCON, Stability, Matignon's theorem

I. INTRODUCTION



The above diagram represents the classification of LTI systems. An LTI system means linear time invariant systems. Linearity is defined as the system that satisfies the principle of superposition and a time invariance system is defined as if the system behavior and characteristics of the system are prefixed over time. So if a system satisfies these two conditions i.e. linearity and time invariance, that system is referred to as a linear time invariant system. These LTI systems are classified into two types one is integer and the other is non-integer. Integer and non-integer systems are differentiated by their order. Order of a function is defined as the highest degree of the denominator polynomial in case of a transfer function and it is defined as the number of state variables used with reference to a state space model. In this paper, we are referring to non-integer ordered systems because of the limitations of integer ordered systems such as limited stability region, less parameters tuning, limited approach for real time applications and less DOF etc. This non-integer (fractional) ordered systems are again classified into two types they are commensurate order systems as and Non-Commensurate order systems.

The system is said to be a commensurate order system if all the orders of derivation are integer multiples of base order γ such that $\alpha_k, \beta_k = k_\gamma, \gamma \in R$ and which cannot be expressed as integer multiples are called as non-commensurate systems. Commensurate order systems are classified into two types one is rational and the other is irrational.

Equation (1) represents the fractional-order continuous-time dynamic system which can be given by a fractional differential equation in the following form[2]

$$H(D^{\alpha_o \alpha_1 \ldots \alpha_n})y(t) = G(D^{\beta_o \beta_1 \ldots \beta_n})u(t),$$

$$H(D^{\alpha_o \alpha_1 \ldots \alpha_n}) = \sum_{k=0}^{n} a_k D^{\alpha_k},$$

$$G(D^{\beta_o \beta_1 \ldots \beta_n}) = \sum_{k=0}^{m} b_k D^{\beta_k} \quad \ldots \quad (1)$$

Where, a_k, $b_k \in R$.

In direct form, eq.(1) can be written as:

$$a_n D^{\alpha_n} y(t) + a_{n-1} D^{\alpha_{n-1}} y(t) + \ldots + a_0 D^{\alpha_0} y(t) = b_m D^{\beta_m} u(t) + b_{m-1} D^{\beta_{m-1}} u(t) + \ldots + b_0 D^{\beta_0} u(t) \quad .(2)$$

The system can be described as a **commensurate-order** if in Eq. (2), all the orders of derivation are integer multiples of a base order γ such that $\alpha_k, \beta_k = k_\gamma, \gamma \in R$.

The above system can then be viewed as in eq. (3) as [7]

$$\sum_{k=0}^{n} a_k D^{k_\gamma} y(t) = \sum_{k=0}^{m} b_k D^{k_\gamma} u(t) \quad \ldots \quad (3)$$

If in eq. (3) the order is approximated with γ = 1/q, where q ∈ Z, [4] then the system is said to be in rational order. Now by applying Laplace transforms to Eq.(1) by assuming zero

initial conditions, the relation between input and output variables of the fractional ordered system can be represented in the form of a transfer function as given below- [8]-[10]

$$G(s)=\frac{Y(s)}{U(s)}=\frac{b_m s^{\beta_m}+b_{m-1}s^{\beta_{m-1}}+.....+b_0 s^{\beta_0}}{a_n s^{\alpha_n}+a_{n-1}s^{\alpha_{n-1}}+.....+a_0 s^{\alpha_0}} \quad \ldots (4)$$

In case, if the given transfer functions (system) is of commensurate type LTI system with an order γ, then the continuous-time transfer function would be given by the following equation as given in eq. (5).

$$G(s)=\frac{\sum_{k=0}^{m} b_k (s^{\gamma})^k}{\sum_{k=0}^{n} a_k (s^{\gamma})^k} \quad \ldots (5)$$

By approximating $\lambda = s^{\gamma}$, the function given in eq (5) can be viewed as a **pseudo-rational function** H(λ), where

$$(\lambda)=\frac{\sum_{k=0}^{m} b_k \lambda^k}{\sum_{k=0}^{n} a_k \lambda^k} \quad (6)$$

Based on the concept of the pseudo-rational functions, a state-space representation of LTI systems can be represented in the form as given in eq. (7)

$$D^{\gamma} x(t)=Ax(t)+Bu(t)$$
$$y(t)=Cx(t)+Du(t) \quad (7)$$

As much similar to the integer ordered LTI systems, the state-space representation of fractional ordered systems as shown in eq. (7), can be transformed in to its equivalent transfer function model through the equation given in eq (8) [11]-[14]

$$G(s)=C(s^{\gamma}I-A)^{-1}B+D \quad \ldots (8)$$

Where, 'I' is the identity matrix, 'A' is the system matrix, 'B' is the input matrix, 'C' is the output matrix and 'D' is the transition matrix. The main advantage of representing the systems through state-space model is that, it permits the users to work on multi-input, multi-output (MIMO) fractional ordered systems.

II. TIME DOMAIN ANALYSIS

The primary focus of this work is to understand the principles behind fractional ordered systems and to plot the step response for understanding the system's dynamic behavior. To this end, few fractional ordered transfer functions were chosen for mathematical analysis flowed by its step response. Hence, the time domain analysis is being presented to get the transient response of fractional-order dynamic systems. A transient response is the reaction of a network which switches from an equilibrium or a steady state. The transient response is not exactly limited to immediate incidents but to any incidents that changes the equilibrium of the network.

Mathematical Approach of Time Domain Analysis

There are different solutions for analysing the systems through mathematical simplifications, where one type of solution is using the inverse Laplace transforms and the other is through Mittag-Leffler functions which are given by Podlubny. But, the drawback of this type of approach is lengthy, complex and huge time taking procedure. [15]-[17]

There is an another method which requires analytical calculation of fractional-order derivatives which can be implemented by using a revised Grünwald-Letnikov definition given under eq. (9)

$${}_a D_t^{\alpha} f(t)=\lim_{h\to 0}\frac{1}{h^{\alpha}}\sum_{j=0}^{\left[\frac{t-a}{h}\right]}\omega_j^{(\alpha)} f(t-jh) \quad \ldots (9)$$

Where, '*h*' is defined as the computational step-size and $\omega_j^{(\alpha)}=(-1)^j\binom{\alpha}{j}$ can be assessed repeatedly in the form as shown below in eq. (10)

$$\omega_0^{(\alpha)}=1,$$
$$\omega_j^{(\alpha)}=\left(1-\frac{\alpha+1}{j}\right)\omega_{j-1}^{(\alpha)},\ j=1,2,... \quad \ldots (10)$$

To obtain an approximated numerical solution for the above expression, firstly, we should obtain the signal $\hat{u}(t)$ by using the algorithm in Eq. (1), where

$$\hat{u}(t)=b_m D^{\beta_m}u(t)+b_{m-1}D^{\beta_{m-1}}u(t)+....+b_0 D^{\beta_0}u(t) \quad ..(11)$$

Therefore, with the above specified mathematical approximations, now we can obtain the time response of the fractional ordered system by using the following equation y(t) as given in equation (12).

$$y(t)=\frac{1}{\sum_{i=0}^{n}\frac{a_i}{h^{\alpha_i}}}\left[u(t)-\sum_{i=0}^{n}\frac{a_i}{h^{\alpha_i}}\sum_{j=0}^{\left[\frac{t-a}{h}\right]}\omega_j^{(\alpha)}y(t-jh)\right] \quad (12)$$

Time domain methodprovides the required information regarding the transient response of any system that is to be analyzed in terms of time domain specifications and also it givesinformation about both electrical degrees and mechanical degrees.

III. FREQUENCY DOMAIN ANALYSIS

Frequency response/domain analysis is a method to analyze the mathematical functions or signals in terms of frequency instead of time.

Some of the very common fields and transforms in which they can be used are Fourier transforms, Fourier series, Z transforms, Laplace transforms and wavelet transforms. Fourier transforms can be used in case of non-repetitive signals and transients. Fourier signals can be used in case of repetitive signals and signals with oscillating nature (sustained oscillations).

Mathematical Approach of Frequency Domain Analysis

In frequency domain method, the response can be plotted by simplifying the transfer functions through substituting $s = j\omega$ in the given transfer function G(s),

From eq. (4), the general representation of a fractional ordered transfer function is given by

$$G(s) = \frac{Y(s)}{U(s)} = \frac{b_m s^{\beta_m} + b_{m-1} s^{\beta_{m-1}} + \ldots\ldots + b_0 s^{\beta_0}}{a_n s^{\alpha_n} + a_{n-1} s^{\alpha_{n-1}} + \ldots\ldots + a_0 s^{\alpha_0}}$$

In order to deal with frequency domain method, let us substitute $s = j\omega$ in the above fractional ordered transfer function,

$$G(j\omega) = \frac{Y(j\omega)}{U(j\omega)} = \frac{b_m (j\omega)^{\beta_m} + b_{m-1} (j\omega)^{\beta_{m-1}} + \ldots\ldots + b_0 (j\omega)^{\beta_0}}{a_n (j\omega)^{\alpha_n} + a_{n-1} (j\omega)^{\alpha_{n-1}} + \ldots\ldots + a_0 (j\omega)^{\alpha_0}} \quad (13)$$

On further simplifying eq (13), the complex frequency response for the range of frequencies ω ∈ (0; ∞) can then be computed through the following equation given in eq (14):

$$R(\omega) = \frac{P(j\omega)}{Q(j\omega)} = \frac{b_m (j\omega)^{\beta_m} + b_{m-1} (j\omega)^{\beta_{m-1}} + \ldots\ldots + b_0 (j\omega)^{\beta_0}}{a_n (j\omega)^{\alpha_n} + a_{n-1} (j\omega)^{\alpha_{n-1}} + \ldots\ldots + a_0 (j\omega)^{\alpha_0}} \quad (14)$$

Where, j is the complex (imaginary) operator

The main advantage of frequency domain method is that, it offers simplified approach for mathematical analysis using Fourier transforms.

In this work, the frequency response analysis is carried out through Bode plots (combining magnitude and phase plots). The specifications like gain and phase crossover frequencies, gain and phase margins are being calculated for ensuring the stability of fractional ordered systems and these plots are being verified using FOTF Viewer in MATLAB.

IV. STABILITY ANALYSIS

The mathematical approach and the applications of fractional ordered systems has a considerable significance over the past few years as most of the real time applications are associated with fractional ordered transfer functions. Stability of such systems always plays a key role in designing a suitable system or tuning the parameters of any such system to meet the industrial requirements [6].

We already know about the classical stability approach for integer order LTI systems like RH criteria and other stability tools like root locus, Nyquist, bode and so on. As we cannot directly apply the above listed stability tools for the fractional ordered systems due to different math approach, here we deal with Matignon's stability theorem for the stability analysis of fractional ordered systems

(Matignon's Stability Theorem): It states that, the fractional transfer function $G(s) = \frac{Z(s)}{P(s)}$ is stable if and only if the following condition is satisfied in σ-plane:[5]

$$|\arg(\sigma)| > q\frac{\pi}{2}, \forall \sigma \in C, P(\sigma) = 0 \quad \ldots \quad (15)$$

Where, $\sigma = s^q$.

- When σ = 0, the system has a single root for P(s), and hence the system cannot be stable. For q = 1, this becomes a classical theorem of pole location in the complex σ plane: and hence no pole is in the closed right plane of the **first Riemann sheet.**

The general representation of the commensurate fractional-order system is

$$D^q \omega = f(\omega) \quad (16)$$

Where, q ranges from 0 to 1 and $\omega \in R^n$ then the equilibrium points are calculated by solving the following equation $f(\omega) = 0$.

Here, the obtained points would be in equilibrium state and the system can be said to be asymptotically stable if all the Eigen values λ_k of the Jacobean matrix J = ∂f/∂w, can be evaluated at equilibrium, which can satisfy the following condition given in eq (17)

$$|\arg(eig(J))| = |\arg(\lambda_k)| > q\frac{\pi}{2}, k = 1,2,\ldots\ldots,\ldots n \quad (17)$$

In other ways, the condition for stability can be justified by the simple equality given in eq. (18) for state-space models of the system

$$|\arg(eig(J))| > q\frac{\pi}{2} \quad (18)$$

Where, q ranges from 0 to 1 and eig (A) means the Eigen values of the state-space matrix A

Unlike integer-order systems, a stable continuous-time fractional-order system can have roots in the right half of the complex plane. The details are exhibited in Fig.1.

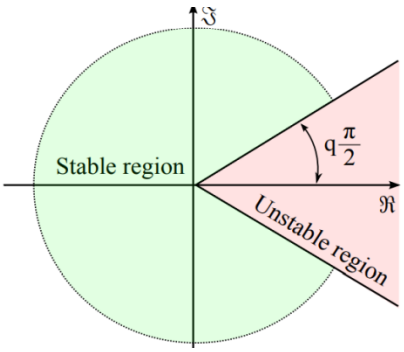


Fig 1 stability region of fractional order system

V. IMPLEMENTATION & DISCUSSION

I. Example-1

$$G(s)=\frac{-2s^{0.63}+4}{2s^{3.501}+3.8s^{2.42}+2.6s^{1.798}+2.5s^{1.31}+1.5}$$

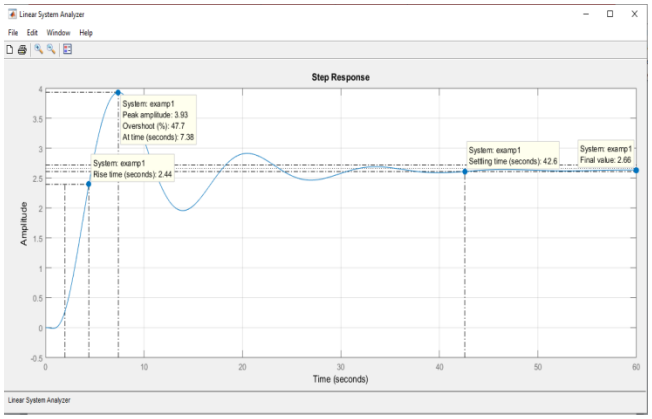


Fig.2 step response of example 1

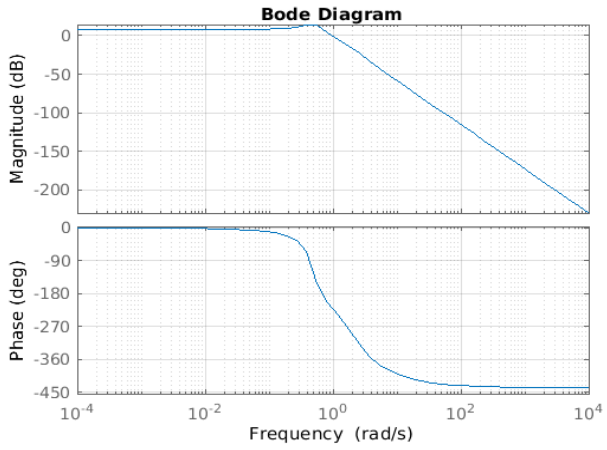


Fig 3. Bode response of example 1

Fig.2 indicates the step response for the given transfer function obtained through FOTF viewer of MATLAB. The response is being indicated with the help of time domain specifications Rise time, settling time, overshoot and the final value.

Fig. 3 indicates the frequency response through bode plot for the given transfer function obtained through FOTF viewer of MATLAB. The response consists of magnitude plot and phase plot. The values of the frequency domain specifications like gain crossover frequency and phase crossover frequency were calculated and it has been observed that both gain and phase margins are positive values, which is an essential condition for stability.

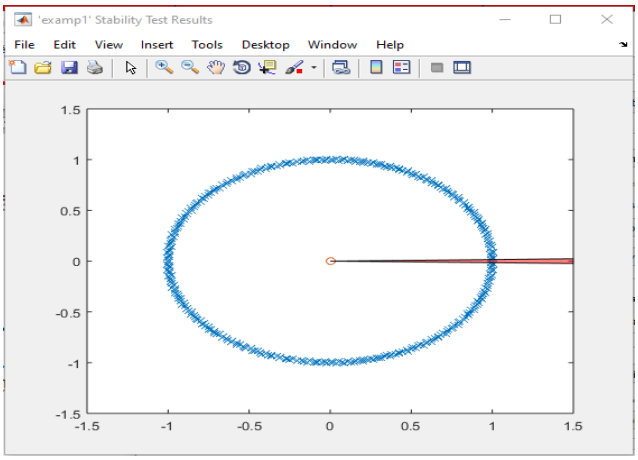


Fig 4. stability response of example 1

Fig. 4 depicts the region covered by the system poles and it has been observed according to Matignon's stability theorem that, the given commensurate system is completely stable with a fractional order, q=0.01 as shown in the dialogue box in fig 5.

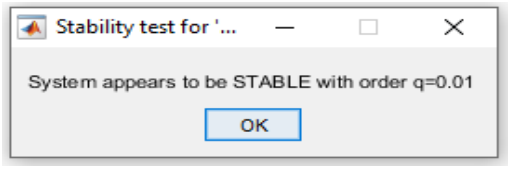


Fig.5 q value of example 1

II. Example-2

$$G(s)=\frac{s^4+9s^{3.2}+31s^{2.4}+58.01s^{1.6}+60.01s^{0.8}+16.03}{s^{4.8}+6s^4+48s^{3.2}+286s^{2.4}+935s^{1.6}+1580s^{0.8}+888}$$

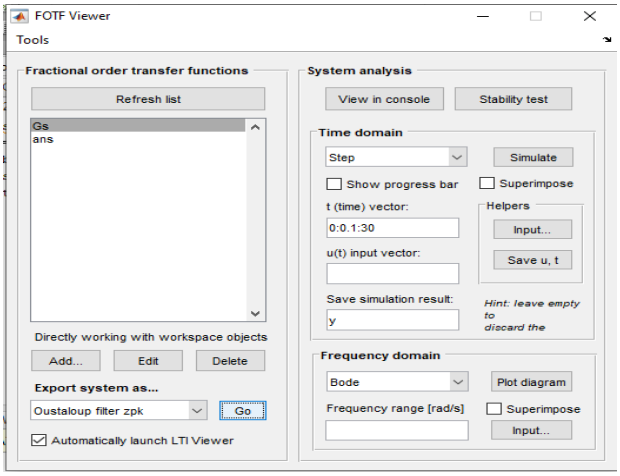


Fig.6 FOTF viewer for step response of example 2

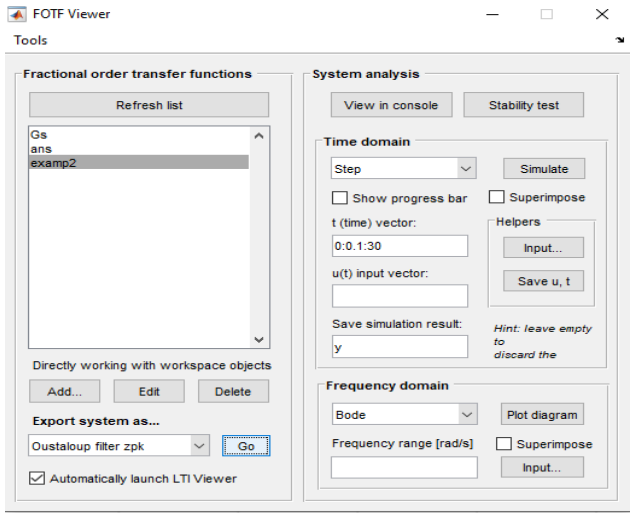


Fig.7 FOTF viewer for bode response of example 2

Figs 6 and 7 indicate the basic representation of fractional order transfer function (FOTF) viewer in MATLAB. It is needed to add a transfer function in the FOTF viewer and save to the workspace. On adding the fractional ordered transfer function, the FOTF viewer offers features like step response, bode plots, polar plots, Nyquist plots and the stability test.

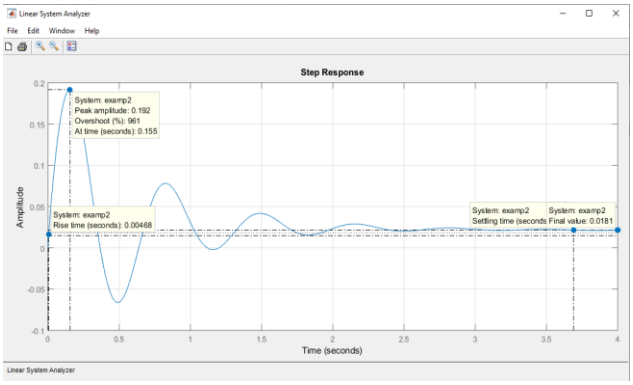


Fig.8 step response of example 2

Fig.8 indicates the step response for the given transfer function obtained through FOTF viewer of ATLAB. The response is being indicated with the help of time domain specifications Rise time, settling time, overshoot and the final value. Fig. 9 indicates the frequency response through bode plot for the given transfer function obtained through FOTF viewer of MATLAB. The response consists of magnitude plot and phase plot.

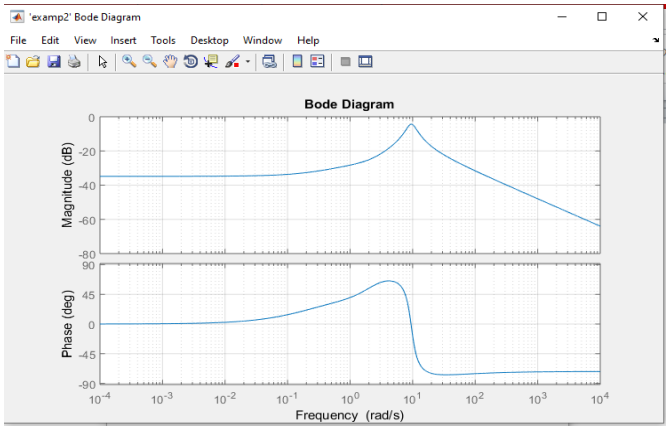


Fig.9 bode response of example 2

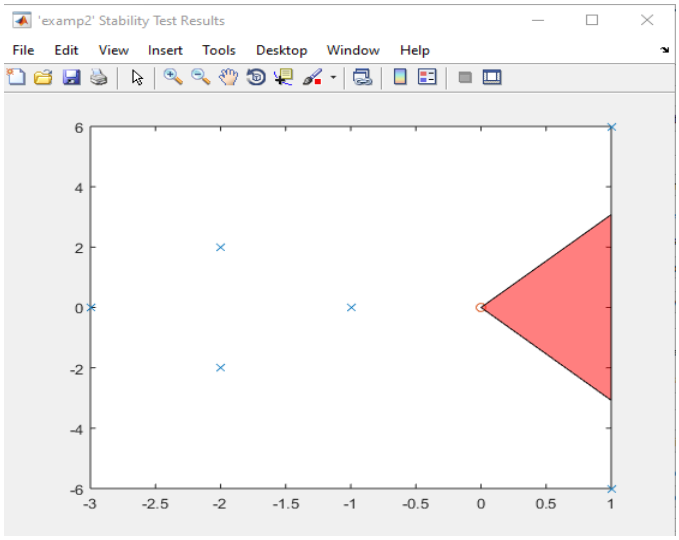


Fig.10 stability response of example 2

Fig.10 depicts the region covered by the system poles and it has been observed according to Matignon's stability theorem that, the given commensurate system is completely stable with a fractional order, q=0.8 as shown in the dialogue box in fig 11.

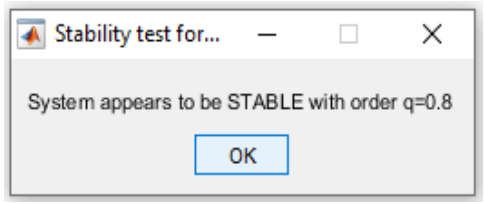


Fig.11 q value of example 2

VI. CONCLUSION & FUTURE WORK

In this work, stability analysis of fractional ordered systems is carried out through time response and bode plots both through theoretical approach and using FOTF viewer of MATLAB. Fractional ordered systems are extremely useful in design solutions to robust and non-linear control, measurements of the electrical impedance of biological tissues, modeling the electrical properties of biological materials, tissues, or cell, design aspects of PMSMs using

FO-PI controller etc.,. Some of the real time applications includes wind turbine generator which is useful for power generation, electro hydraulic systems for lifting heavy weights, twin rotor systems, precision positioning system which is a global navigation satellite system positioning method that calculates error as small as few centimeters, it can be used in military applications. These can also be used in magnetic levitation system as propels in trains and for contactless welding.

These fractional ordered systems can be extended to implement suitable filtering methods, for auto tuning using methods and strategies, improving stability using PID controlling actions [3], [18]-[20] on usage with AI techniques like ANNs, Fuzzy [2] and so on.

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Design and Implementation of an Advanced ATM Crime Prevention Using GSM Module

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Abstract— The Idea of Designing an Advanced ATM Crime Prevention System is born with the observation of ATM crime incidents happening around the world.
This paper deals with the prevention of ATM crime. Whenever robbery occurs, magnetic switch sensor is used to detect the opening and closing the door of the ATM machine. This system uses AURDINO UNO microcontroller based embedded system to process real time data collected using the sensor. Once the movement is sensed the beep sound will occur from the buzzer. DC Motor is used for closing the door of ATM. RTC used to capture the robber occur time and send the robbery occur time with the message to the nearby police station through the GSM. At the same time this system also deals with the safety of the customer by alerting the surrounding people and nearby police station whenever the customer is in dangerous situation.
This system will prevent the crime and the person involving in crime can be easily caught.

Index Terms— Aurdino uno microcontroller-AT89C51, magnetic switch Sensor, GSM module, DC Motor, Buzzer, Transformer, Rectifier

I. INTRODUCTION

Today, ATM has become an irreplaceable communication and service channel between banks and cardholders due to its fast, convenience and human resource saving advantages; since the introduction of the first automated teller machine (ATM) in 1967, perpetrators have been devising ways to try to steal the cash inside. Because ATMs eliminate the need for round-the clock human involvement and tend to be located in places that make them more vulnerable to attack. According to estimates by Retail Banking Research, there are more than 2.2 million ATMs deployed worldwide. This is a figure forecasted to exceed 3 million by 2016. As the number of ATMs in use increases, so do the frequency and sophistication of security threats, making the development of crime prevention measures a top priority for financial institutions (FIs) and ATM manufacturers.

But with the prosperity of installed ATM, the reported ATM crime also has been dramatic grown (Figure 1), causing big loss for cardholders and banks. To build safe ATM use environment, maintain bank's brand image and protect bank assets, all the involved organizations, institutions, and persons must research, develop and takes measures to meet the challenges faced by ATM crimes.

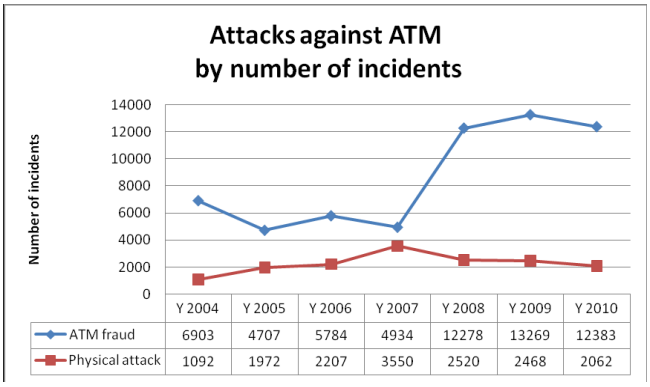


FIGURE 1: ATM RELATED ATTACKS. SOURCE: EAST

The above statistics necessitates the implementation of ATM crime prevention system. Therefore, this paper suggests the method of providing security to both the ATM and the customers whoever using ATM services. So by using the GSM technology, magnetic switch sensor, DC Motor, Aurdinon uno the theft can be easily caught. Here DC Motor is used to close the door of the ATM.It is used to alert the surrounding people and nearest police station whenever the customers are in dangerous situation.

II. PROPOSED SYSTEM

A. Architecture of the proposed system:

The architecture of the proposed system is shown in Figure2.When the Magnetic switch sensor detects any movement of ATM ,it sends a signal to the AT89C51 via GPIO pins.whenever the received signal level is greater than the threshold value then controller activates the output devices such as dc motor, buzzer and GSM.DC motor closes the door of the ATM. At the same time buzzer gives continuous beep sound and message will be send to the

nearest police station via GSM module. This gives a continues message which will alert the surrounding people and gsm alerts the nearest police station by sending a message that the customer is in dangerous situation.

COMPONENTS USED

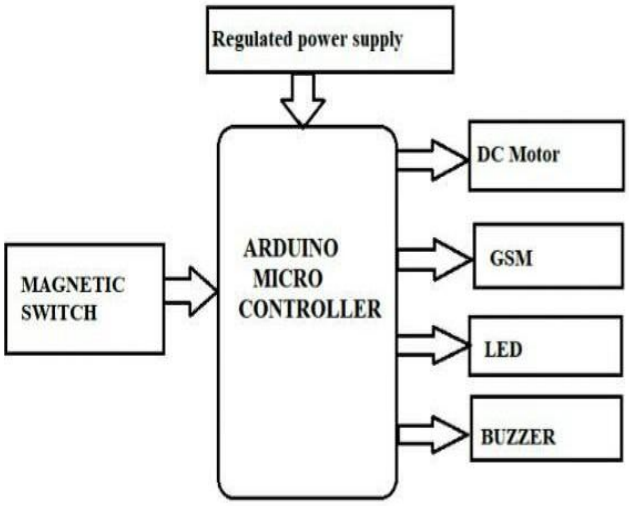
Magnetic switch Microcontroller GSM module LED

Buzzer

Power supply

Here all The components are interfaced to AURDINO Microcontroller (AT89C51)

BLOCK DIAGRAM:



HARDWARE MODULES

MAGNETIC SWITCH

The magnetic switch used in this project work is assembled in a glass container and when the heavy magnet is brought near to this magnetic switch; the contact of the switch gets closed automatically due to the magnetism. In this project work one such magnetic switch is used and is installed in the ATM machine door or the cash box door. A permanent magnet is installed near the wall of the door.

Microcontroller:

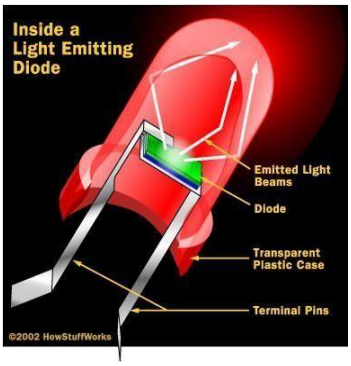
Microcontroller is widely used embeded system products. Micro controller is a programmable device. A microcontroller has a CPU in addition to a fixed amount of RAM, ROM, I/O ports and a timer embedded all on a single chip. The fixed amount of on-chip ROM, RAM and number of I/O ports in microcontrollers makes them ideal for many applications in which cost and space are critical.

GSM module:

This GSM Modem can accept any GSM network operator SIM card and act just like a mobile phone with its own unique phone number.Applications like SMS Control, data transfer, remote control and logging can be developed easily.

LED:

A light-emitting diode (LED) is a semiconductor light source. LED's are used as indicator lamps in many devices, and are increasingly used for lighting.



Transformer:

A transformer is a device that transfers electrical energy from one circuit to another through inductively coupled conductors without changing its frequency. A varying current in the first or primary winding creates a varying magnetic flux in the transformer's core, and thus a varying magnetic field through the secondary winding. This varying magnetic field induces a varying electromotive force (EMF) or "voltage" in the secondary winding. This effect is called mutual induction

GSM Module: This GSM Modem can accept any GSM network operator SIM card and act just like a mobile phone with its own unique phone number. Advantage of using this modem will be that you can use its RS232 port to communicate and develop embedded applications. Applications like SMS Control, data transfer, remote control and logging can be developed easily.The modem can either be connected to PC serial port directly or to any microcontroller through MAX232. It can be used to send and receive SMS or make/receive voice calls. It can also be used in GPRS mode to connect to internet and do many applications for data logging and control. In GPRS mode you can also connect to any remote FTP server and upload files for data logging.This GSM modem is a highly flexible plug and play quad band **SIM900A** GSM modem for direct and easy integration to RS232 applications. Supports features like Voice, SMS, Data/Fax, GPRS and integrated TCP/IP stac\.

FIGURE: GSM MODEM

Buzzer: A buzzer or beeper is an audio signaling device, which may be mechanical, electromechanical, or piezoelectric. Typical uses of buzzers and beepersinclude alarm devices, timers and confirmation of user input such as a mouse click or keystroke. A joy buzzer is an example of a purely mechanical buzzer. Early devices were based on an electromechanical system identical to an electric bell without the metal gong. Similarly, a relay may be connected to interrupt its own actuating current, causing the contacts to buzz. Often these units were anchored to a wall or ceiling to use it as a sounding board. The word "buzzer" comes from the rasping noise that electromechanical buzzers made. A piezoelectric element may be driven by an oscillating electronic circuit or other audio signal source, driven with a piezoelectric audio amplifier. Sounds commonly used to indicate that a button has been pressed are a click, a ring or a beep.

FIGURE: BUZZER

MAGNETIC SWITCH

The magnetic switch used in this project work is assembled in a glass container and when the heavy magnet is brought near to this magnetic switch; the contact of the switch gets closed automatically due to the magnetism. In this project work one such magnetic switch is used and is installed in the ATM machine door or the cash box door. A permanent magnet is installed near the wall of the door. When the door is perfectly closed, the magnetic switch will be activated and generates a signal. This signal from the magnetic switch is fed to the microcontroller by which it understands that the door is closed. And if the door is opened, no signal will be coming from the magnetic switch, by which the controller understands that the door is opened and generates an eight bit code that is modulated by the RF transmitter at a frequency of 433 MHz and is transmitted from the antenna.

Now coming to the magnetic switches, different shapes and sizes are available in the market. Since technologies of the product have more and more advance, the products need comply with a requirement for more safe, convenient and low cost. The magnetic switches are extremely compact, simple and are easy to install on any small space. These switches are not affected by electrical interference. They can withstand to chemicals, high temperatures and pressures.

When the magnetic field of permanent magnet inside the float is moved to the proximity of the reed switch inside the stationary stem, the reed switch "snaps" the contact together and closes the electrical circuit. When the magnetic field is removed away from the switch the contact of the switch does not touch and the circuit will be in open condition

III. SOFTWARE IMPLEMENTATION

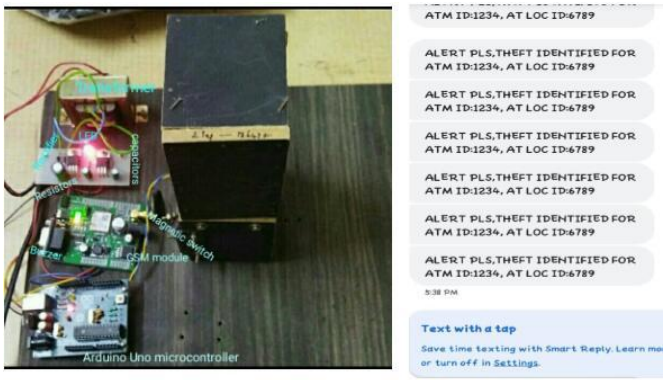
This project is implemented using following software:

Arduino IDE compiler - for compilation part

Arduino IDE (Integrated Development Environment) is the software for Arduino It is used for writing code, compiling the code to check if any errors are there and uploading the code to the Arduino. It is a cross-platform software which is available for every Operating System like Windows, Linux, macOS.

Arduino Software (IDE) - contains a text editor for writing code, a message area, a text console, a toolbar with buttons for common functions and a series of menus. It connects to the Arduino and Genuino hardware to upload programs and communicate with them.There are two required functions in an Arduino sketch, setup() and loop(). Other functions must be created outside the brackets of those two functions. As an example, we will create a simple function to multiply two numbers.

KIT/RESULT



IV. CONCLUSION

As we all know these days most of the ATM have been attacked by the robberies. From the first ATM being installed in the world, ATM has gradually become a target of crimes.

While with the constantly evolving of reported ATM crime, ATM industry has begun to payattention to the safety of ATM, even card holders.

Our project demonstrates how an automation of ATM crime prevention can be implemented using GSM technology, ARDUINO microcontroller, DC motor, buzzer and ATM Machines center. By implementing this project we can easily prevent the crime and also we can save our precious time. Presence of every module has been reasoned out and placed carefully, thus contributing to the best working of the unit. Besides, using highly advanced Microcontroller with the help of growing technology, the project.

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Automatic Test Case Generation Using Genetic Algorithm

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Abstract— Software development process has an important activity that is software testing. Software testing is most efforts consuming phase in software development. To reduce the time and cost effort in software development automatic test case generation is helpful to minimize the effort and maximize the fault detected. So automatic test case generation may be treated as an optimization problem. In this paper the proposed approach is applied to the ATM withdrawal task. Experimental results show that GA was able to generate suitable test data based on a fitness value and avoid redundant data by optimization.

I. INTRODUCTION

Automatic generation of test data plays a major role in software testing process. Software testing is mainly two types that are white box testing and black box testing. White box testing is also called structural testing ad basic path testing is one part of the structural testing. Automatic generation of test case is one of the key research topics in software testing because test case generation is important part of the software testing lifecycle. Today, practitioners as well as researchers use common methods such as notion to perform, random testing and heuristic approaches for generation of the test cases [1]. for larger and complicated programs These methods have some drawbacks in generating test cases So other techniques of artificial intelligence is used so much for automatic test case generation Test data generation in program testing, is the process of identifying a set of test data, which satisfies the given testing criterion[2]

Test data generation is a method which helps a tester in generation of test cases for a given source Code.

In this paper, we discuss Genetic algorithm (GA) for Generating test cases based on a set of basic paths. in a module All the paths selected need to be executed and then generating a large set of test cases for these paths. But this process is quite difficult task. As a result, certain degree of automated process should be carried out to minimize testing resources and to cover all the paths we make control flow graph and then genetic algorithm helps in achieving this goal.

II. NEED OF AUTOMATION

Testing is a process of executing a source code with the intent of finding errors [13].Software testing can also be defined as a series of processes, which is designed to make sure that the source code does for which it was designed and does not do anything unintended [13]. Software should be predictable and consistent, offering no surprises to users. The main objective of testing is to validate the software product that it meets a set of pre-established requirements that is described in software requirement specification. There are two phase to this objective. The first phase is to validate that the requirements specification from which the software was designed is correct. The second phase is to verifying that the design and coding correctly respond to the requirements [14]. Automatic test case generation helps in reducing the execution time and in finding errors. the cost in developing test cases is also reduced by automating the testing process.

III. OVERVIEW OF BASIC PATHS

Path testing is one of the famous structural testing criteria [15]. This method searches the source code for suitable test cases, predefined path is reached when the source code is executing with the test cases ., each path is \tested for efficient functionality Based on the analysis of cyclomatic complexity Practically it is possible to apply path testing for a specific subset of paths in the control flow graph. This aim of this mechanism is to compute the logical complexity of a procedural design and defines a set of execution paths. in such a way Test data are generated that they will execute every statement at least once.

\ the complexity of an algorithm is evaluating by the cyclomatic complexity. It shows the number of test cases that are required to test the method completely, it estimate the number of test cases required to gain maximum code coverage which is very helpful for the tester.The resultant test cases give more effecting testing than statement and branch coverage. Cyclomatic complexity is given by the equation V(G) = e – n + 2, where ‘e’ is the number of edges and ‘n’ are the number of nodes. in a control flow graph(CFG).

IV. GENETIC ALGORITHM

GA is an optimization and machine learning algorithm based loosely on the processes of biological evolution. John Holland created the GA field [10] and it is the first major GA publication. GA provides a general-purpose search methodology, which uses the principles of natural evolution [11].

Genetic algorithm as an effective global smart search method, reveals its own strength and efficiency to solve the large space, optimized for high complicated problems, and thus provides a new method to solve the problems of generating test data [1].GA solves optimization problems by manipulating initial population (individual chromosomes

sampled randomly). Each chromosome is evaluated based on a fitness function which is related to its success in solving a given problem. Given an initial population of chromosomes, GA proceeds by choosing chromosomes to serve as parents and then replacing members of the current population with new chromosomes that are (possibly modified) copies of the parents. The process of selection and population replacement goes on until a stopping criterion (achieving effective test data) has been met [12].

Thus GA has been successfully used to automate the generation of test data. GA begins with a set of initial population which is randomly sampled for a particular problem domain. Then GA is applied, by performing a set of operations iteratively to get a new and fitter generation. Generating test data automatically reduces the time and effort of the tester.

The two common operations that are performed to produce efficient solution for a target problem after selection operation are Crossover and Mutation.

Fitness Function for Basis Paths

A fitness function for test data generation for an ATM withdrawal task is developed based on Bogdan Korel's branch distance function [2]. Consider a path 'P' in the program execution. The goal of the test data generation problem is to find a program input 'x' on which P will be traversed. Without loss of generality, Korel assumed that the branch predicates are simple relational expressions (inequalities and equalities). That is, all branch predicates are of the form: E1 opE2, where E1 and E2 are the arithmetic expressions and op is one of {<, ≤, >, ≥, =, ≠} the operator. In addition, he assumed that predicates do not contain AND's or OR's or other Boolean operators. Each branch predicate E1 opE2 can be transformed to the equivalent predicate of the form F rel 0, where F and rel are given in Table-2.

This concept was used in our approach to test the ATM withdrawal task. We generated test data for a feasible basis path in the CFG. From CFG, we can compute the number of paths required to be tested. We have generated test data for a single feasible with respect to an ATM withdrawal task[13].

V. PROPOSED SYSTEM

The concept of GA has been applied to the problem of automated test data generation process. Here the test data is referred to as population in GA. In initial population, each individual bit string (chromosome) is a test data. This set of chromosomes is used to generate test data for feasible basis paths.

The system for generating automated test data for feasible basis paths using GA has been coded in MATLAB. It randomly generates the initial population, evaluates the individual chromosome based on the fitness function value and applies the GA operations such as selection, crossover and mutation to produce next generation. This iterative process stops when the GA finds optimal test data.

Fitness Function Design for Our Approach

We have taken up a case study, describing a customer's activity of withdrawing money from an ATM [13]. Each customer in the bank system has an account and an ATM debit card. The scenario considered here for design of fitness function is that the customer tries to withdraw certain amount from the ATM machine (this withdrawal amount is the initial test data generated randomly, with an assumption that customer entering the withdrawal amount is random).Figure-1 shows the sequence of operations performed in ATM withdrawal task by the customer.

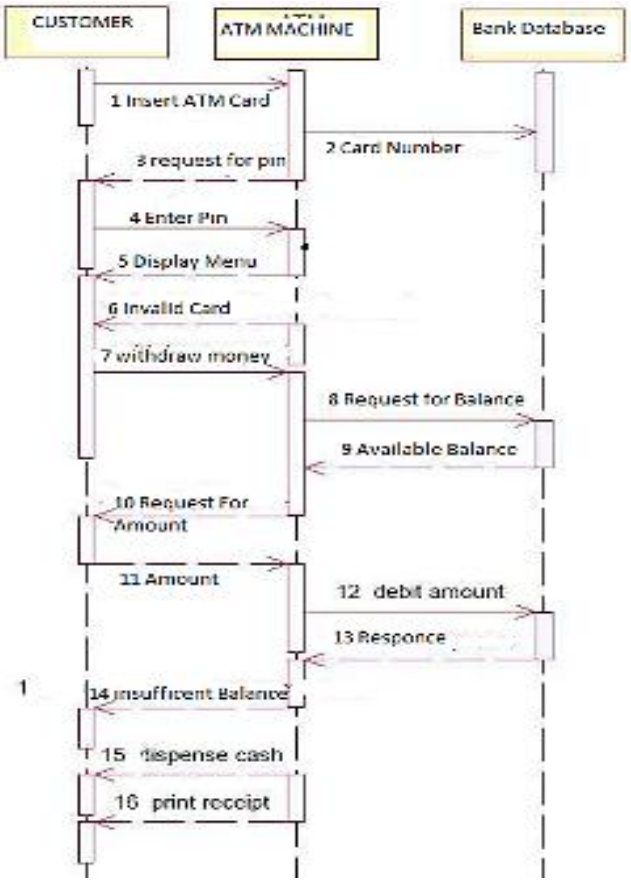

Fig 1. Sequence diagram for ATM Withdraw

So now taking equality condition into consideration, A = B implies A – B = 0; as GA for test data generation is minimization the fitness function 'f' is given as 1 / (A - B). But this functional value 'f' will evaluate to infinity when A – B=0, so to avoid this condition a small delta value is added to the fitness function. Hence the fitness function in general is given as: f = 1 / ((abs (A - B) + 0.5) ^ 2).

Applying Genetic Algorithm for Path Testing

The principle of GAs has been applied to generate test data automatically. The developed system generates optimal test data automatically on the basis of basis paths in the control flow graph. The first generation is generated randomly and then by performing the basic GA steps, fitness of individuals gets improved. The system first generates the individual test data randomly, and then calculates fitness for

each individual chromosome (test data) and on the basis of their fitness values it performs mutation and crossover. This process continues until all individuals reach to the maximum fitness. The system performs all operations from initial population to last generation automatically; it does not require the user interference. Generating test data automatically reduces the time and effort of the tester.

Genetic Algorithm for Test Data Generation

The following steps show the algorithmic approach followed to generate test data for the basis path derived from CFG using GA.Figure-4 shows the schematic representation of test data generation using GA. Algorithm:

Input: Randomly generated numbers (initial population act as test data) based on the target path to be covered.

Output: Test data for the target path.

1. Gen = 0
2. While Gen < 500
3. do
4. Evaluate the fitness value of each chromosome based on the objective function.
5. Use Elitism as selection operator, to select the individuals to enter into the mating pool.
6. Perform two-point cross over on the individuals in the mating pool, to generate the new population.
7. Perform bitwise Mutation on chromosomes of the new population

8 Gen = Gen +1

9 Go to Step 3

10 end

11 Select the chromosome having the

Best fitness value as the desired result

(Test data for target path).

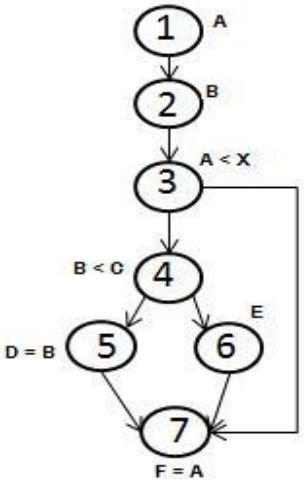

Fig 2. Control Fow Graph For Withdraw From ATM

Experimental Settings

The following sets of parameters were considered for test data generation using GA.

a. Fitness function :

f = 1 / ((abs (suc_bal (i) - min_bal) + 0.05) ^2)

b. Coding : Binary String

c. Length of the string in the chromosome : 15bits

d. Population Size (N) :100

e. Selection method :Elitism

f. Two-point crossover and $p_c = 0.5$

g. Mutation probability(p_m) = 0.05

h. Stopping Criteria = number of generation (500) First set of test data was generated Randomly.

The test Data that we derived based on the set of basis paths depends on the programs structure with an aim to traverse every executable statement in the program. The fitness function used was derived on the basis of branch distance [2]. The input variables were represented in binary form. The main objective of using GAs lies in their ability to handle input data which may be complex in nature. Thus, the problem of test data generation is treated entirely as an optimization problem. One of the merits of using GAs is that through the search and optimization process, test data sets are improved in a manner that they are close to the input domain.

VI. RESULTS

The approach followed for test data generation for path testing using GA, the following four basic steps were processed viz., Control Flow Graph Construction, Target Path Selection, Test Data generation and Execution, Test Result Evaluation.

Table-4 shows the fitness value range of test data and the classification of individual chromosome into their respective classes based on fitness value in terms of percentage.

Table 1 Class of Test Data having maximum fitness value

Fitness Value Range		% of Test Data
0 ≤	f(x) < 0.3	61
0.3 ≤	f(x) < 0.7	01
0.7 ≤	f(x) < 1.0	38

Table-4 gives us a clear picture that around 38% of test data have higher fitness value ‘f(x)’and lie in the range between 1.0 and 0.7.

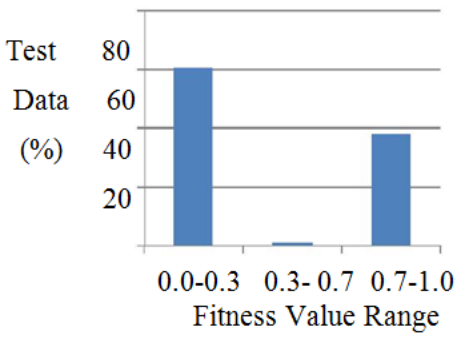

Fig 3 Graphical Representation of fitness

VII. CONCLUSIONS

In software development life cycle, software testing is one of the critical phases. So generation of test data automatically is a key step which has a great influence on code coverage in software testing.

In this paper, a GA based on theory of natural selection was used to generate test data automatically for feasible basis paths. After the generation of initial test data randomly, GA was iterated for 500 generations as in practicality computation time should be finite. This paper makes use of a fitness function based on the condition of the predicate node.

The results in this paper are an indication that GA is more effective and efficient in generating automated test data rather than random testing.

The future perspective of the work would be to enhance automated test data generation for large and complex programs, as of now the existing methods generate test data for smaller and simple programs.

Another prospective area of future study would be to generate test data using a fitness function for multiple paths in the control flow graph. The test data generated using GA can be used in code coverage analysis by comparing with other artificial intelligence techniques such as Particle swarm optimization, Simulated annealing, Clonally selection algorithm etc.

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Impact of Increase in Single Use Plastic Waste due to COVID-19 Pandemic and Mitigation Measures

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Abstract—During the COVID-19 epidemic, plastic goods were crucial in keeping people safe. The increased usage of personal protection equipment disrupted the production, supply chain and waste disposal system of plastic waste. Millions of discarded single-use plastics like used PPE kits, masks, gloves, aprons, used sanitizer bottles etc are being disposed over the land potentially causing a rise in plastics washing up on ocean shores and fouling the seabed. This research aims to evaluate the possible consequences of plastic contamination over land and sea. Since the outbreak, an estimated 1.6 million tonnes of plastic garbage has been produced every day throughout the world. As a result of the COVID-19 epidemic, we estimate that over 3.4 billion single-use facemasks/face shields are wasted every day. COVID-19 appears to have the potential to reverse the momentum of the worldwide fight to minimise plastic waste pollution, which has been ongoing for years. There is a potential to develop new sectors that can design new reusable or non-plastic PPEs as governments want to boost the economy by assisting companies in surviving the epidemic. At present biomedical single use plastic products can't be reused due to fear of contamination. Recycling plastic waste by melting at higher temperatures can be used in both ways as heat disinfection and recycling.

Key Words—Plastic Waste, COVID-19, Biological Contmination, Mitigation

I. INTRODUCTION

During the COVID-19 epidemic, a variety of plastic-based personal protective equipment (PPE) played an important role in keeping people safe. Since the coronavirus pandemic began, there has been a significant increase in single-use plastics (SUPs), such as gloves, protective medical suits, masks, handsanitizer bottles, takeaway plastics, food and polymer products containers, and medical test kits. The handling of trash generated by SUPs is a concerning side effect of the COVID-19 epidemic, which has wreaked havoc on worldwide healthcare systems and thrown economies into disarray (Benson et al., 2021; Vanapalli et al., 2021; Herron et al., 2020; Silva et al., 2020).

COVID-19 virus is extremely infectious, according to data, and might survive for many days on plastic surfaces (Chin et al., 2020; Doremalen et al., 2020; Nghiem et al., 2020).

We offer a system for calculating the number of facemasks produced daily by the world population living in urban and semi-urban regions during the COVID-19 pandemic in this paper. We also calculated the amount of plastic garbage created on a daily basis, as well as by the year 2020. During the management of the COVID-19 pandemic, we also explore the influence of healthcare facilities, quarantine facilities, home and hotel isolation facilities, and other sources on the consumption and disposal of single-use plastics.

II. REASON FOR THE INCREASED USAGE OF SINGLE USE PLASTICS

Since the SARS-CoV-2 outbreak, there has been a significant increase in the amount of discarded single-use surgical and face masks, as well as latex gloves, found littering the streets, highways, medical institutions, parking lots, dumpsites, beaches, gutters, and shopping carts. During the epidemic, demand for plastic items including as disposable gloves, masks, bottled water, disposable wipes, hand sanitizers, and cleaning agents has increased at an unprecedented rate (Syam, 2020; Nzediegwu and Chang, 2020). To combat the spread of the COVID-19 virus, most governments issued lockdown regulations as well as social and physical distancing measures. The COVID-19 epidemic, on the other hand, has exacerbated the plastic pollution problem by reviving consumer demand for single-use items and materials for health and safety concerns. Because of hygienic concerns, single-use fabrics are commonly used to wrap vegetables and fruit in shops and supermarkets.

Furthermore, in order to avoid the transmission of the COVID-19 virus, health personnel are often urged not to reuse their personal protective equipment (PPE), suggesting that tonnes of plastic medical waste are created every day. To limit the community spread of COVID-19, the World Health Organization (WHO), the United States Centers for Disease Control and Prevention, and the European Center for Disease Prevention and Control have all recommended strict physical distancing measures, cancellation of mass gatherings, frequent handwashing, and the closure of educational institutions. Furthermore, practically every country has advocated and adopted the use of facemasks to decrease human-to-human transmission and protect the most vulnerable and at-risk populations (CDC, 2020a). Millions of facemasks have been created, used, and discarded in accordance with this guideline and rigorous directives.

However, there is growing fear that discarded surgical masks, medical gowns, face shields, safety glasses, protective aprons, sanitizer containers, plastic shoes, and

gloves may find up in our aquatic environments as a result of the current coronavirus outbreak. In March 2020, there was an avalanche of COVID-19 cases throughout the world, resulting in a global scarcity of gloves, surgical masks, face masks, and other personal protective equipment (PPE). N95 and KN95 respirators, as well as surgical masks, are common and recommended forms of PPE. They are designed for maximal filtration of aerosols and infectious airborne particles, protecting the user against respiratory illnesses such as bronchitis and pneumonia.

The N95 masks are tight-fitting respirators, but the surgical masks are loose-fitting medical masks that come in a variety of thicknesses and water percolation capacities. Both types of wearables are intended to be discarded after a single usage. Respirators, surgical, and face masks are labelled as "single-use" disposable medical or respiratory protection equipment, according to the Centers for Disease Control and Prevention (CDC), and should be put in a "plastic bag" after use and then thrown away (US FDA, 2020a). This advice is a vital step, but it may exacerbate the plastic waste problem by introducing more single-use plastics into our ecosystem.

The enormous increase in disposable surgical masks and hand gloves may add to the avalanche of plastic pollution (Boyle, 2020; Chaudhuri, 2020). This might compound the existing plastic pollution issues, which are projected to be threatening the health of our ecosystems, global seas, and marine animals due to nearly 10 million tonnes of plastic (Kane

III. THE ENVIRONMENTAL IMPACTS OF BIOMEDICAL PLASTIC WASTES

Land-based human activities, such as the unregulated disposal of biomedical wastes, have long been considered potential sources of hazardous, infectious, and radioactive contaminants (WHO, 2018). Cytotoxic, chemical, pathological, pharmaceutical, sharp, radioactive, and general wastes are some of the most common types of healthcare waste. Plastic is used to make the majority of these wastes, particularly sharp and general wastes including syringes and scalpels, gloves, surgical masks, surgical and isolation gowns, face shields, shoe covers, sanitizer containers, and waterproof aprons. More biological waste in the form of waste plastics has resulted from the COVID-19 epidemic.

According to the WHO, low-income and high-income nations create around 0.2 and 0.5 kilogramme of hazardous biological wastes each day, respectively (WHO, 2018). The Ministry of Ecology and Environment's Emergency Management Office noted a 23 percent rise in the quantity of medical waste created and managed in China, where the COVID-19 was originally recorded (Tang, 2020). As a result, China has amassed 142,000 tonnes of medical waste, with the country's medical waste treatment capacity expanding from 4902.8 tonnes per day prior to the SARS-CoV-2 pandemic to 6022 tonnes per day now.

IV. METHODOLOGY

In this paper, the daily facemasks generated by each country were calculated as a product of the country's total population and an arbitrary percent of the urban population accepting facemasks (Benson et al., 2021; Nzediegwu and Chang, 2020). The daily and monthly facemask generation were calculated as a function of an individual's estimated single facemask use per day and for a thirty-day average, respectively. The following equations were used to create the model:

$$Total\ monthly\ face\ masks\ generated = 3.0 \times 10^{-3}\left(T_p \times U_p \times A_r \times A_c\right) \quad (1)$$

$$Total\ daily\ face\ masks\ generated = \left(\frac{T_p \times U_p \times A_r \times A_c}{10,000}\right) \quad (2)$$

where Tp denotes the country's estimated population, Up denotes the proportion of the country's urban population, Ar denotes the percent face mask acceptance rate, and Ac denotes the average daily face masks per capita. The average number of days in a calendar year.

V. RESULTS AND DISCUSSION

Plastic garbage has been created at a pace of 1.6 million tonnes per day since the pandemic began (Table 1). As a result of the COVID-19 epidemic, we predict that 3.4 billion single-use facemasks or face shields are wasted every day. China, which has the world's biggest population, is expected to create almost 702 million wasted facemasks every day, and 108 million tonnes of plastic garbage by the end of 2020. According to our calculations, Asia will produce the most wasted facemasks per inhabitant every day (1.8 billion). Europe comes in second with 445 million people, followed by Africa with 411 million and Latin America and the Caribbean with 380 million.

Table 1. Reported COVID-19 cases, deaths, and estimated total plastic waste generation by region, measured in tonnes

Region	Population[a]	Total COVID-19 cases[b]	Total COVID -19 deaths[b]	Facemask acceptance rate by population (%)[c]	Average Facemask/capita/day	Estimated daily facemask disposed	Estimated plastic waste generated (Tonnes)	Estimated plastic waste generated per day (Tonnes)
Africa	1,340,598,147	212,271	5,718	70	1	411,814,854	100,544,861	275,465
Asia	4,641,054,775	1,470,640	37,222	80	1	1,875,181,681	348,079,108	953,641
Europe	747,636,026	2,149,248	181,138	80	1	445,022,934	56,072,702	153,623
South America	653,952,454	1,267,858	54,648	75	1	380,414,703	49,046,434	134,373
North America	368,869,647	2,361,458	140,399	80	1	244,335,150	27,665,223	75,795
Oceania	42,677,813	8,896	124	75	1	21,682,379	3,200,836	8,769

In light of existing regulations and COVID-19 guidelines in many countries, mandating the use of single-use facemasks (face shields) might possibly increase the amount of PPE waste generated. For example, the daily facemasks generated if all citizens in China (1.4 billion people), India (1.3 billion people), the United States (331 million people), Brazil (212 million people), Nigeria (206 million people), and the United Kingdom (67 million people) wear and discard a facemask or face shield per day could total at least 702, according to estimates.

These unmanaged wastes potentially make up the majority of littering in terrestrial areas and along coastal shorelines. Furthermore, according to our estimates, over 7.7 billion people will create around 585 million tonnes of plastic garbage by 2020, with around 82 percent of that garbage originating from the top 35 nations indicated in Table 2. (Table S1). The majority of them are from low- and middle-income nations, where waste management infrastructure is lacking. As a result, the percentage of unmanaged plastic wastes is anticipated to rise, culminating in disposal in open landfills or uncontrolled dumpsites with a surplus of plastic trash. Medical and residential waste management, on the other hand, is a huge concern, particularly in poor nations. Plastic-based wastes and other non-biodegradable synthetic substances can float around in the environment, collecting hazardous chemicals and infections on their surfaces, posing health concerns to people and marine species. According to a research conducted by the World Wide Fund for Nature (WWF), if just 1% of surgical and face masks are inappropriately disposed into our terrestrial and marine settings, it may result in a monthly littering of our ecosystem of up to 100 billion masks.

The upshot is that over 405 Mt of SUPs might be added to the existing horrendous plastic pollution problem (Syam, 2020). However, this significant growth in plastic garbage occurs at a time when many nations' recycling initiatives are being halted due to fears of the virus spreading (Hagemann, 2020). As a result, the COVID-19 pandemic has the potential to exacerbate the worldwide plastic waste problem. Previous research has found that infected surfaces are ideal vectors for viral illness transmission (Jones and Gibson, 2020; Park et al., 2015; Vasickova et al., 2010).

Table 2: Estimated daily facemasks and global plastic waste generation by country

Country	Population[a]	Urban Population[a]	Rate (%) of face mask acceptance[b]	Face mask / capita/day[b]	Estimated daily facemask disposed	Estimated plastic waste
China	1,439,323,776	61%	80	1	702,390,003	107,949,283.20
India	1,380,004,385	35%	80	1	386,401,228	103,500,328.90
United States	331,002,651	83%	80	1	219,785,760	24,825,198.83
Brazil	212,559,417	88%	75	1	140,289,215	15,941,956.28
Indonesia	273,523,615	56%	80	1	122,538,580	20,514,271.13
Japan	126,476,461	92%	80	1	93,086,675	9,485,734.58
Russia	145,934,462	74%	80	1	86,393,201	10,945,084.65
Mexico	128,932,753	84%	75	1	81,227,634	9,669,956.48
Nigeria	206,139,589	52%	70	1	75,034,810	15,460,469.18
Pakistan	220,892,340	35%	80	1	61,849,855	16,566,925.50
Bangladesh	164,689,383	39%	80	1	51,383,087	12,351,703.73
Turkey	84,339,067	76%	80	1	51,278,152	6,325,430.02
Vietnam	97,338,579	38%	80	1	29,590,928	7,300,393.42
DR Congo	89,561,403	46%	70	1	28,838,771	6,717,105.22
Thailand	69,799,978	51%	80	1	28,478,391	5,234,998.35
South Africa	59,308,690	67%	70	1	27,815,775	4,448,151.75
Canada	37,742,154	81%	80	1	24,456,915	2,830,661.55
Ukraine	43,733,762	69%	80	1	24,141,036	3,280,032.15
Iraq	40,222,493	73%	80	1	23,489,935	3,016,686.98
Saudi Arabia	34,813,871	84%	80	1	23,394,921	2,611,040.33
Algeria	43,851,044	73%	70	1	22,407,884	3,288,828.30
Egypt	102,334,404	43%	70	1	30,802,655	7,675,080.30
Colombia	50,882,891	80%	75	1	30,529,734	3,816,216.82
Spain	46,754,778	80%	80	1	29,923,057	3,506,608.35
Mozambique	31,255,435	38%	70	1	8,313,945	2,344,157.63
Madagascar	27,691,018	39%	70	1	7,559,648	2,076,826.35
Jordan	10,203,134	91%	80	1	7,427,882	765,235.05
Sweden	10,099,265	88%	80	1	7,109,883	757,444.87
Greece	10,423,054	85%	80	1	7,087,677	781,729.05
Guatemala	17,915,568	52%	75	1	6,987,072	1,343,667.60

Dominican Republic	10,847,910	85%	75	1	6,915,543	813,593.25
United Arab Emirates	9,890,402	86%	80	1	6,804,596	741,780.15
Cuba	11,326,616	78%	75	1	6,626,070	849,496.20
Peru	32,971,854	79%	75	1	19,535,823	2,472,889.05
Australia	25,499,884	86%	75	1	16,447,425	1,912,491.30
Tanzania	59,734,218	37%	70	1	15,471,162	4,480,066.35
Angola	32,866,272	67%	70	1	15,414,282	2,464,970.40
Taiwan	23,816,775	79%	80	1	15,052,202	1,786,258.12
Myanmar	54,409,800	31%	80	1	13,493,630	4,080,735.00
Uzbekistan	33,469,203	50%	80	1	13,387,681	2,510,190.22
North Korea	25,778,816	63%	80	1	12,992,523	1,933,411.20
Netherlands	17,134,872	92%	80	1	12,611,265	1,285,115.40
Yemen	29,825,964	38%	80	1	9,067,093	2,236,947.30
Kazakhstan	18,776,707	58%	80	1	8,712,392	1,408,253.02
Romania	19,237,691	55%	80	1	8,464,584	1,442,826.82
Syria	17,500,658	60%	80	1	8,400,315	1,312,549.30
Ecuador	17,643,054	63%	75	1	8,336,343	1,323,229.05
Uganda	45,741,007	26%	70	1	8,324,863	3,430,575.53
Bolivia	11,673,021	69%	75	1	6,040,788	875,476.57
Belarus	9,449,323	79%	80	1	5,971,972	708,699.22
Nepal	29,136,808	21%	80	1	4,894,984	2,185,260.6
Honduras	9,904,607	57%	75	1	4,234,219	742,845.525
Bulgaria	6,948,445	76%	80	1	4,224,654	521,133.375
Austria	9,006,398	57%	80	1	4,106,917	675,479.85
Denmark	5,792,202	88%	80	1	4,077,710	434,415.15
Zimbabwe	14,862,924	38%	70	1	3,953,537	1,114,719.3
Maldives	540,544	35%	80	1	151,352	40,540.80
Greenland	56,770	87%	80	1	39,511	4,257.75
Hong Kong	7,496,981	N/A	80	1	N/A	562,273.57
Singapore	5,850,342	N/A	80	1	N/A	438,775.65
Kuwait	4,270,571	N/A	80	1	N/A	320,292.82
Venezuela	28,435,940	N/A	75	1	N/A	2,132,695.50

[a]*Data retrieved from https://www.worldometers.info/population/ on June 02, 2020*
[b]*Hypothetical data; N/A – Not available*

Recent research have discovered SARS-CoV-2 in sewage and wastewater samples from the Netherlands (Lodder and de Roda Husman, 2020; Medema et al., 2020), Australia (Ahmed et al., 2020), and the United States (Ahmed et al., 2020). (Wu et al., 2020). SARS-CoV-2 RNA was found in untreated wastewaters and sewage as a result of coronavirus sorption and stability on the surfaces of poorly discarded single-use medical wastes (Chin et al., 2020). Epidemiological studies on the surface stability of SARS-CoV-2 and SARS-CoV-1 show that once a fomite has been infected, the infectious virus particles can survive for few minutes to several days on a variety of surfaces.

Medical and residential waste management, on the other hand, is a huge concern, particularly in poor nations. Plastic-based wastes and other non-biodegradable synthetic substances can float around in the environment, collecting hazardous chemicals and infections on their surfaces, posing health concerns to people and marine species. According to a research conducted by the World Wide Fund for Nature (WWF), if just 1% of surgical and face masks are inappropriately disposed into our terrestrial and marine settings, it may result in a monthly litterin However, this significant growth in plastic garbage occurs at a time when many nations' recycling initiatives are being halted due to fears of the virus spreading (Hagemann, 2020). As a result, the COVID-19 pandemic has the potential to exacerbate the worldwide plastic waste problem. Previous research has found that infected surfaces or fomites are ideal vectors for viral illness transmission (Jones and Gibson, 2020; Park et al., 2015; Vasickova et al., 2010). Recent research have discovered SARS-CoV-2 in sewage and wastewater samples from the Netherlands (Lodder and de Roda Husman, 2020; Medema et al., 2020), Australia (Lodder and de Roda Husman, 2020), and the United States (Lodder and de Roda Husman, 2020). (Ahmed et al., 2020), g of our ecosystem of up to 100 billion masks.

SARS-CoV-2 RNA was found in untreated wastewaters and sewage as a result of coronavirus sorption and stability on the surfaces of poorly discarded single-use medical wastes (Chin et al., 2020). Epidemiological studies on the surface stability of SARS-CoV-2 and SARS-CoV-1 show that once a fomite has been infected, the infectious virus particles can survive for few minutes to several days on a variety of surfaces (Figure 4). SARS-CoV-2 has been found to be more viable and stable for 2–3 days on plastics and stainless-steel surfaces than on cardboard, wood, banknotes,

and copper, according to recent investigations (Chin et al., 2020; Doremalen et al., 2020).

Overall, these findings support the theory that humans can get the virus by coming into contact with infected and poorly dumped plastic-based biomedical waste. This shows that SARS-CoV-2 might spread and become infective through medical waste originating from healthcare institutions, home isolation, and quarantine facilities where infected patients are having treatment, and might be a source of infection (Doremalen et al., 2020; Nghiem et al., 2020; Vasickova et al., 2010; Todd et al., 2009). Although additional environmental variables may influence SARS-CoV-2 survival for long periods of time on contaminated surfaces and plastics (Doremalen et al., 2020).

As a result, present trash collection and treatment systems must be thoroughly revised to eliminate the risk of SARS-CoV-2. Littering, disposal in uncontained landfills, and open dumping of SARS-CoV-2-generated wastes might exacerbate the contamination caused by current marine litter. Globally, land-based trash creation is expected to be the dominant source of plastics in marine environments (Jambeck et al., 2015).

Untreated biomedical and household wastes from the land can, however, be re-distributed into the environment and carried to marine systems by runoff and atmospheric deposition. According to a recent report, effective waste management strategies, such as proper identification, collection, segregation, storage, treatment, and disposal, as well as adequate awareness and training, would be required for the fate and distribution of biomedical wastes during and after the SARS-CoV-2 outbreak (BWS Inc, 2018; CDC, 2020b; Klemes et al., 2020; Patil et al., 2015).

VI. MITIGATION MEASURES TO REDUCE BIOMEDICAL PLASTIC POLLUTION IMPACTS

The devastating effects of the COVID-19 pandemic, combined with strategic response measures implemented by governments and healthcare providers around the world, have posed new challenges in the fight against plastic pollution. COVID-19 will undoubtedly reverse the momentum of a years-long global campaign to reduce single-use plastics. We must learn how to handle plastics if we want to maintain the benefits of plastics without jeopardising the environment. As the world focuses on finding a solution to coronavirus, this study aims to call attention to the need for tighter waste management techniques targeted at minimising coronavirus contamination of the environment.

For single-use medical gloves, surgical masks, surgical suites, face shields, and aprons, this can be accomplished through proper disposal and strict adherence to established hazardous medical waste management standards. The creation of a thorough conservation strategy for appropriate sterilisation and disinfection of surgical gowns and masks should take into account the minimization of dangers that such guidelines may provide to healthcare professionals and COVID-19 patients. Healthcare practitioners might utilise reusable surgical gowns instead of disposable single-use PPE, as suggested by the US FDA (US FDA, 2020b).

Surgical gowns are used as a barrier to microbial and fluid transfer during medical operations and are typically composed of either single-use or reusable fabrics (Ammirati, 2005; Song et al., 2011). Furthermore, healthcare practitioners may prioritise the usage of PPE for various patients. This would result in a significant reduction in the quantity of plastic garbage produced. Used personal protective equipment should be disposed of properly in well-labeled clinical waste containers, followed by recycling at certified biohazard waste treatment facilities, in order to solve the current problem of environmental plastic pollution.

VII. CONCLUSION

Given recent global efforts to battle the highly infectious SARS-CoV-2 virus, the environment may have benefited in terms of carbon footprint reduction and better air and surface water quality. Since the coronavirus epidemic, however, there has been a surge in the demand for, consumption of, and emission of single-use plastics. According to our calculations, since the onset of COVID-19, a massive quantity of single-use plastic garbage has been created globally. According to regional projections, Asia will produce the most wasted facemasks each day (1.8 billion). Europe, Africa, Latin America and the Caribbean, North America, and Oceania, with 445, 411, 380, 244, and 22 million facemasks a day, respectively, followed by Europe, Africa, Latin America and the Caribbean, North America, and Oceania. China (1.4 billion), India (1.3 billion), the United States (331 million), Brazil (212 million), are estimated to generate at least 702, 386, 219 & 140million facemasks per day if all of their citizens wear and discard a facemask or face shield per day. Given these projections, single-use plastic and personal protective equipment (PPE) pose an increasing threat. This has the potential to exacerbate current plastic pollution issues, posing a serious threat to our collective survival as well as the survival of marine creatures. Not only is there a possible environmental risk from poorly disposed non-biodegradable PPE made of plastics, but there are also human health hazards from eating seafood, which is a popular source of nutrition for many people across the world. Macro-, meso-, and microplastics in the environment and marine ecosystems, in particular, might act as potential infection vectors. Fish, turtles, beach seabirds, sea turtles, whales, and other marine animals are examples of marine creatures. In marine mammals it might result in serious damage and death.

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Impact Assessment and Mitigation for Desertificatification in Anantapur District of Andhra Pradesh, India

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Abstract—Desertification is a natural process. There is a need for dynamic desertification assessment at various levels for complete planning and preparedness. The purpose of this paper is to create a desertification vulnerability index (DVI) and anticipate desertification processes in Anantapur District, India. A multivariate index model is developed to prepare DVI based on climate, land use, soil, and socioeconomic characteristics. In 9 distinct locations, 14.2 percent of the land was established as a training dataset for modelling, and the remaining area was evaluated for desertification process prediction. The Desertification Status Map (DSM) of Anantapur District was created as a reference dataset for the computation of accuracy indices as part of the Desertification Status Mapping of India – 2nd Cycle (DSM -2nd Cycle). Overall accuracy rate and kappa index for training datasets were 83.2 % and 73.8%, whereas testing datasets were 72.6 % and 49.4%. The findings of the Random Forest model's variable importance analysis revealed that DVI was the most important predictor of desertification processes, followed by potential evapo-transpiration and NDVI. The current study's findings reveal the amount of desertification in the Anantapur area. Desertification mitigation methods are also identified appropriate for this region.

Key Words— desertification; desertification vulnerability indices, mitigation measures

I. INTRODUCTION

Desertification is the degradation of land in arid, semi-arid, and dry sub-humid regions due to a variety of reasons such as climate change and inappropriate human activity (UNEP, 1992). It impacts a third of the world's land surface, making it particularly vulnerable to overexploitation and irresponsible land use. According to UN estimates, nearly 3.6 billion hectares of the world's land area have already been desertified (UNCCD, 2014), with 5,300 million tonnes of rich soil and 8 million tonnes of plant nutrients lost each year owing to various desertification processes.

Desertification is caused by a variety of processes including vegetation deterioration, erosion, waterlogging and salinization, and loss of soil fertility (Dregne & Chou, 1992).In the case of India, rising human and cattle populations are putting enormous strain on land resources, resulting in considerable soil degradation. About 228 Mha (69%) of India's total geographical area (328 Mha) is dry (arid, semi-arid, or dry sub-humid), and these regions are densely inhabited and more subject to environmental stress**.**

According to Sehgal & Abrol (1994), 57 percent of India's land area has been degraded in some fashion, with areas under agriculture being the most deteriorated, followed by grazing land and forests. According to Singh (2009), the country's salinity and sodicity issue has deteriorated 6.73 million hectares.The Indian government has performed several desertification status assessment and monitoring initiatives at various sizes as a signatory to the United Nations Convention to Combat Desertification (UNCCD) (Ajai et al., 2009; Singh, 2009).

The process of compiling an inventory of India's desertification state was recently completed by the Space Application Centre (ISRO) in Ahmedabad, in partnership with 19 partner institutes (SAC, 2016). According to the research, diverse desertification processes affected 82.64 Mha of the country's arid, semi-arid, and dry sub-humid areas between 2011 and 2013, up 1.16 Mha from 2003-05. In arid regions, wind erosion is the most prominent mechanism of desertification, but in semi-arid and dry sub-humid areas of the nation, plant degradation and water erosion predominate.

In the MEDALUS technique, the Environmental Sensitivity Index (ESI) is calculated by combining the Soil Quality Index, Climate Quality Index, Vegetation Quality Index, and Management Quality Index (Kosmas et al., 1999). Though the model has its own flaws, such as equal weight for all indices (Salvati et al., 2009), it is a useful index, especially in Mediterranean climates, due to its ease of model construction and flexibility in indicator selection (Trott et al., 2015), and the model requires expert judgement for assigning scores to the various classes (Giordano et al., 2003). In a typical Mediterranean farmland environment, Karamesouti et al. (2015) employed the PESERA and TERON models to quantify soil erosion rates and the MEDALUS approach to quantify the total desertification risk. Dasgupta et al. have also employed fuzzy inference algorithms to delineate ecologically susceptible zones (2013). To map the desertification sensitivity index in central Iran, Jafari & Bakhshandehmehr (2013) used fuzzy logic and the ESI. Dutta and Chaudhuri (2005) investigated ecologically sensitive regions in Rajasthan's Jhunjhunun and Sikar districts, finding that

13% of the research area was very vulnerable to desertification.

The goal of this work is to use the multivariate index model to generate desertification susceptibility indicators and to test the Random Forest Model for predicting distinct desertification process for unvisited sites in the Anantapur District of Andhra Pradesh, India. There research uses traditional methods to analyse small areas for desertification impactsand then extrapolating the results to a broader area using machine learning models. Mitigation measures are also made to reduce the impact of desertification.

II. DESCRIPTION OF THE STUDY AREA

Anantapur, India's driest district after Rajasthan, is located in the Rayalaseema area of Andhra Pradesh between 13°40' and 15°15' N latitudes and 76°50' and 78°30' E longitudes (Fig.1). The District's total geographical area (TGA) is 19130 km2. Anantapur's climate is hot all year and is mostly characterised as a hot desert bioclimatic state. The average temperature is constantly over 23° C, and the warmest months are April and May, with average temperatures of 32-35°C. The average rainfall is 552 millimetres. The average annual potential evapo-transpiration is 1857 mm, which is about three times the yearly rainfall. Red soils are dominant in the area followed by black cotton soils and sandy soils.

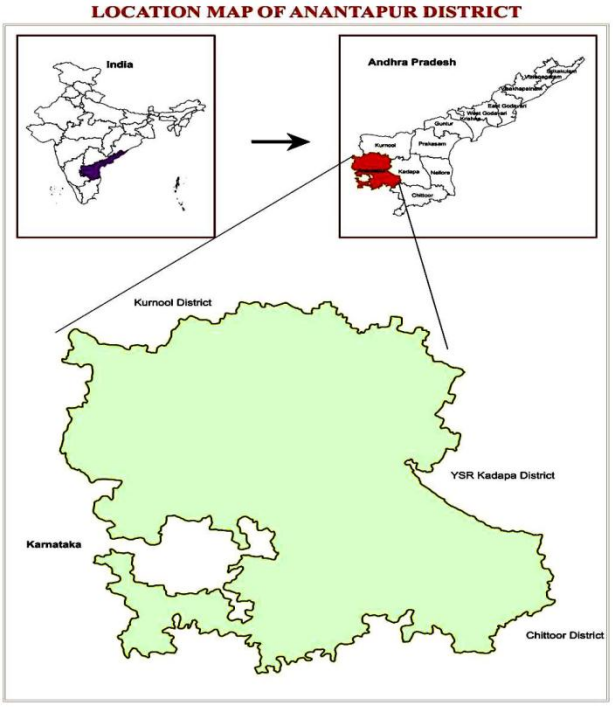

Fig-1. Location of Study Area

III. METHODOLOGY

To assess the impact of desertification, the following indices and models are to be analysed for the study area.

Desertification vulnerability index

It's crucial to estimate the risk of desertification so that suitable conservation measures may be put in place to avoid it (Dasgupta et al., 2013). To generate the desertification vulnerability index, we employed a multivariate index model. Rather of using the traditional method of categorising land degradation, which divides each parameter into upper and lower limit values, we employed a modified weighted index to categorise the various parameters. In biophysical index, climate, soil, and land use indicators are created independently in the form of geographical layers and merged in a GIS context to identify ecologically vulnerable areas for desertification (BPI). The socioeconomic index (SEI) is also used to estimate the risk of desertification. The final desertification index, knowledge of all indices is essential for accurate assessment.

Socio-Economic Index

Desertification is influenced by society and its economic conditions, which have an indirect or direct impact on every piece of land. In combination with poverty, population pressure, unemployment, and illiteracy constitute a major danger to the environment (Vu et al., 2014). In Italy, Salvati et al. (2009) used population growth and density to produce a land vulnerability index. Symeonakis et al. (2016) used an old age index and education level, as well as population growth and density, to analyse the island of Lesvos' susceptibility to desertification (Greece).

Bio-Physical Index

Aridity index is used to determine the climate index. The Aridity index was calculated using annual average rainfall data from 1981 to 2011 (IMD, 2013) and potential evapo-transpiration. The aridity index (P/PET) was determined and divided into two categories: arid 0.2 and semiarid 0.2-0.5. The soil index was created using the soil map of the Anantapur District (NBSS&LUP, 2008). This was categorised into five groups based on soil depth, drainage, and soil texture, as well as available water holding capacity (AWC) and rock fragments. Ranks were allocated depending on the range of data (Kosmos et al., 1999). Table 1 shows the criteria that were utilised to evaluate the soil index.The land utilisation index was created using current land use and slope data, and it was divided into three categories: underutilization, optimal use, and overutilization. The LUI identifies the current state of land use and the daner of desertification (Sastry, 2009). In a GIS context, climate, soil, and land usage indexes were merged, and a composie index (BPI) was constructed utilising expert knowledge in the GIS context (Dasgupta et al., 2013).

Soil Index = (soil depth*drainage*soil texture* AWC *Rock fragments)^ 1/5

Spatial prediction of desertification processes using Random forest model

To anticipate the primary desertification processes in the Anantapur District, we utilised the Random Forest 4.6 package (Liaw & Wiener, 2002) in the R environment. The Random Forest Model (RFM) is based on the combination of a number of classification or regression trees (depending on the response variable) with two levels of randomization for each tree in the forest (Breiman, 2001). RFM enhances prediction accuracy and reduces model over-fitting when compared to other prediction models (Breiman 2001; Liaw & Wiener, 2002). The RFM has the benefit of being unaffected by missing data and being able to manage vast amounts of quantitative and categorical data (Grinand et al., 2000).

IV. RESULTS AND DISCUSSION

Desertification Vulnerability Indices

The results of the Desertification Vulnerability Indices (Table 2 and Fig. 2) revealed that 10.2 percent of areas have a very high index. These are high-priority regions in the Anantapur District that require rapid attention to counteract desertification. For desertification vulnerability, 18.7% of lands are classed as high, while 34.4 percent of areas are classed as moderate.

Table.1. Assigned scores of soil quality indices for calculation of DVI

Soil depth			**Soil texture**	
Class	Score		Class	Score
Deep (>100 cm)	4		SL, SCL, CL	3
Moderately deep (75-100 cm)	3		Sandy clay, Clay	2
Moderately shallow(50-100 cm)	2		Sand, Loamy sand	1
Shallow (<50 cm)	1			
Gravelliness			**Drainage**	
Slightly gravelly (<15 %)	1		Well drained	3
Moderate (15-35 %)	2		Mod. Well drained	2
Strong (>35 %)	3		Imperfectly drained	1
AWC			**Soil Quality Indices**	
Very high (>200 mm/m)	3		Very low	1-125
High (150-200 mm/m)	2.5		Low	1.25-1.5
Medium (100-150 mm/m)	2		Moderate	1.50-1.75
Low (50-100 mm/m)	1.5		High	1.75-2.0
Very low (<50 mm/m)	1		Very high	>2.0

SL-sandy loam, SCL-Sandy clay loam, CL-Clay loam

Table. 2. Area under different vulnerability classes

DVI	Area (ha)	Area (%)
Very low	95929.95	5.0
Low	564356.9	29.4
Medium	659957.9	34.4
High	359347.4	18.7
Very high	196411.1	10.2
Settlement	11930.25	0.6
Waterbody	28781.87	1.5

Bio-Physical Index

Soil Index

Soil is crucial in determining an ecosystem's environmental vulnerability. Soil qualities that impact water retention capacity and erosion resistance are linked to desertification. Based on its natural ranges, the soil quality index was divided into five groups. The data show that high quality soils account for 29.39 percent of the total area, followed by extremely low (21.14 percent) and intermediate quality soils (20.7 percent).

Climatic index

The amount of aridity was used to create a climate index. The Anantapur District's average annual rainfall varied from 381 to 693mm, with a mean (μ) and standard deviation (σ) of 552 mm and 67 mm, respectively. The aridity index was created using yearly rainfall and potential evapo-transpiration, and it ranges from 0.07 to 0.32, with a mean (μ) of 0.25 and a standard deviation of 0.02 (σ). The District is classified into two climate classifications based on the aridity index. A semiarid zone encompasses 99 percent of Anantapur District, whereas arid zones cover 1 percent of Anantapur TGA.

Prediction and extrapolation of desertification process using Random Forest model

For the prediction of desertification/land degradation processes in Anantapur District, we employed a Random Forest model (RFM). Anantapur's desertification status map, created as part of the Project Desertification Status Mapping of India-2nd cycle, was used as a reference dataset for evaluating forecast quality. A total of 7373 pixels were chosen as the training dataset in 9 different locations. Based on OOB error estimations, the number of trees (ntree) for the model was finalised. Because the OOB error estimates stabilised at 500 trees, the parameter ntree

for the final model was set at 500. At each split, three factors are tested. The model's OOB classification error rate is 14.46 percent.

Table 3. Confusion matrix of training and testing datasets

Class	Training				Testing			
	No desertification	Salinisation	Vegetal degradation	Erosion	No desertification	Salinisation	Vegetal degradation	Erosion
No desertification	3743	33	124	110	22781	2632	1970	4709
Salinisation	314	220	18	20	92	208	11	25
Vegetal degradation	173	1	1519	43	1741	180	9048	971
Erosion	168	3	59	825	1926	114	675	4815

Table. 4. Accuracy parameters of random forest models

Accuracy parameter	Training	Testing
Overall accuracy	85.54	71.01
Kappa index	75.77	51.80

The confusion matrix findings (Table 3) revealed that 825 pixels of the soil erosion class were accurately predicted out of 1055 pixels (user accuracy 78.1 percent and producer accuracy 82.7 percent). The accuracy of the vegetal deterioration class is 87.5 percent for the user and 88.3 percent for the producer. 3743 pixels were properly predicted out of 4010 pixels with no desertification class (User accuracy-93.3 percent). Due to a lower number of pixels picked for training data, the salinisation process was under forecasted, with user and producer accuracy of 38.7% and 85.6 percent, respectively, when compared to other processes. Overall, 85.54 percent of training datasets are accurate, with a kappa value of 75.77 percent (Table 4).

The analysis of the predicted map revealed that soil erosion, salinisation, and vegetal degradation processes affect 19.2, 2.12, and 19.77 percent of the District, respectively (Table 5 and Fig. 3), compared to 19.6, 6.2, and 22.5 percent of the area actually mapped for soil erosion, salinisation, and vegetal degradation processes, respectively. This model performed well in the soil erosion, vegetative degradation, and no desertification classes, as well as throughout the expected salinisation phase.

Table 5. Actual and predicted area of desertification in Anantapur

S.No	Class	% of Total geographical area	
		Actual (%)	Predicted
1	Soil erosion	19.6	19.24
2	Salinisation	6.2	2.12
3	Vegetal Degradation	22.5	19.77
4	No desertification	51.7	58.99

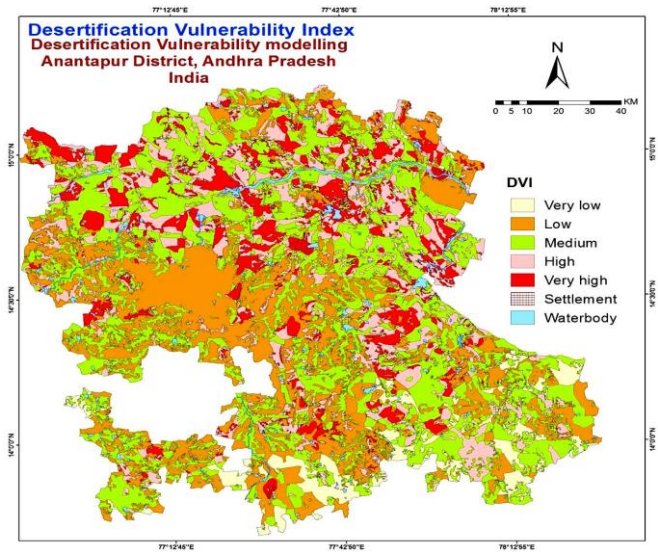

Fig.4. Desertification vulnerability index of Anantapur district

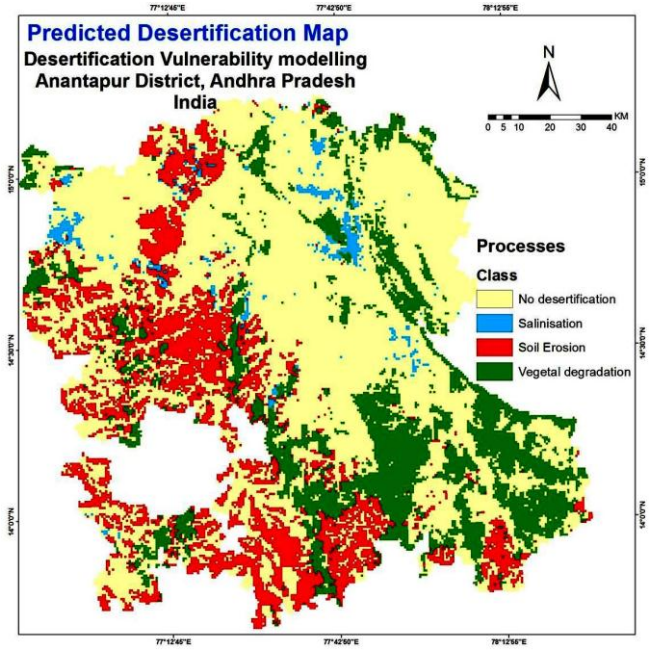

Fig.3. Predicted desertification process map of Anantapur district

V. MITIGATION MEASURES

Desertification mitigation is an essential part of environmental restoration programmes aimed at deforested, degraded, or desert environments. Its mitigation in locations where the desertification process is well underway is unavoidable if the region is to be restored for long-term development. To maintain the ecosystem and ecosystem viable, a balance between fertile land and desert is essential. Stopping deforestation and commencing afforestation are the first stages in repairing desertification-affected regions. To stop the desertification process from spreading to neighbouring places, preventive actions are required. These strategies necessitate environmental education for local residents about desertification as well as their engagement in the repair of damaged regions.(Sastry GS. 2011)

Although it is seldom feasible to restore a decertified place to its pre-decertified form, restorative efforts can help to restore the ecosystem to a new condition that can withstand cultural and land use stresses. Developing a robust vegetation cover of mixed trees, shrubs, scrubs, and grass suited for local requirements, as well as safeguarding soil from unfavourable circumstances, are two specific approaches.

VI. CONCLUSION

Climate, soil, vegetation, and socioeconomic indexes were merged in a multivariate index model to create a desertification susceptibility index. About 10.2 % of the land has been designated as a very highly sensitive region, requiring an immediate response to halt desertification. We also attempted to forecast the desertification map using training set data and compared it to the Anantapur desertification status map that had previously been created. For predicting multiple desertification processes functioning in Anantapur District, we employed a modern machine language methodology called Random Forest model. For OOB and test sites, we found that overall accuracy was 85.54 % and 71.01 % respectively.

In order to mitigate the desertification in Anantapur district, Several water conservation measures are to be taken. State and Central Governments must take construct check dams and provide forestation to increase the ground water levels, to prevent soil erosion.

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Silver Reflective Solar Photo Voltaic System with Low Radiation Using Tilt Sensor and Arduino

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Abstract—Governments around the globe are planning to increase the amount of power generation from renewable energy sources, of which solar energy has tremendous scope to consider in the first place. Different methods are employed to produce solar energy like tracking systems, reflection systems and radiation reduction systems. Among these, reflective solar panels are highly efficient and so would be the best choice. This paper mainly targets both power consumption and reduction of the radiation effect. An analysis of different reflected solar PV panels is carried out of which mirror reflected and silver or aluminum reflected panels are found effective. In the proposed system, to increase power generation, silver reflective solar photovoltaic panels are used. For reducing the radiation effect, such systems must be placed over water resources such as rivers or lakes or water tanks. Silver coated sheets are fixed around the panel to absorb more sunlight throughout the day, and light intensity is monitored using a tilt sensor and Arduino. The silver reflective solar photovoltaic system will work similar to that of a solar tracking system. Solar energy is detected with continuous observation of threshold level values of voltage and current during the day time using a tilt sensor and Arduino. The output power is recorded in various combinations. The results prove that power consumption increases 40% by using the Silver Reflective solar PV system with a low radiation process. Thus, the proposed system is cost-effective with increased panel efficiency.

Key Words— PV system; Tilt sensor; Silver reflection; Arduino

I. INTRODUCTION

Due to the increased interest in the utilization of solar energy, it is essential to enhance the energy collection of solar energy devices. To convert solar energy directly into electrical energy, photovoltaic modules are widely being used. Different techniques such as retrofitting of reflectors and concentrators are adopted to increase the amount of radiation flux falling on the module and the output of the module thereby increases. Most mirrors presently in use employ either silver (domestic and decorative applications) or Aluminum films (automotive applications] for their reflecting surfaces. Mirrors made of silver must be protected from chemical and physical deterioration of the silver; whereas, aluminum mirrors are more resistant to degradation.

Since both silver and aluminum reflecting surfaces in solar applications must retain their highest reflectivity for many years, the reflecting surfaces are protected with transparent covering materials referred to as superstrates. Also, this adds to the physical integrity of the reflector since the superstrate supports the silver. Reflectors are used in the solar technology to concentrate the sunlight onto the solar panels. They employ glass as a base material with a silver coating and a protective layer over it. They elevate the energy input of solar panels as the whole solar spectrum is reflected on them. Materials with more reflective properties are needed to be used to increase the reflectivity and efficiency of solar reflectors. If solar reflectors are used with the solar panels, then their efficiency as well as production from the solar panels will be maximized..This Paper mainly focused on both things power consumption and reduction of the radiation effect. So in the proposed system, to increase power generation, silver reflective solar photovoltaic panels are used. For reducing the radiation effect, such systems must be placed over water resources such as rivers or lakes or water tanks. Solar energy is detected with continuous observation of threshold level values of voltage and current during the day time using a tilt sensor and Arduino.

II. LITERATURE REVIEW

***Reflectors*:**

A **mirror** is an object that reflects light in such a way that, for incident light in some range of wavelengths; the reflected light preserves many or most of the detailed physical characteristics of the original light, called specular reflection. This is different from other light-reflecting objects that do not preserve much of the original wave signal other than color and diffuse reflected light, such as flat-white paint. The most familiar type of mirror is the plane mirror, which has a flat surface.

Curved mirrors are also used, to produce magnified or diminished images or focus light or simply distort the reflected image.

Fig.1: Effect of Angle Orientation of Flat Mirror Concentrator on Solar Panel System Output.

Fig. 2: the dark town that built a giant mirror to deflect the Sun

Silvering is the chemical process of coating glass with a reflective substance. Reflective Silver architectural film keeps homes and offices more comfortable while providing exterior reflectivity that offers privacy, cuts glare, and helps lower energy costs.

- Heat Reduction: blocks up to 80% of the sun's heat saves on air conditioning costs.
- Energy Savings: saves costs in winter too, as the same film retains interior heat.
- Rejects up to 99% of UV rays, slowing fading of furnishings and flooring.
- Glass Breakage Protection: Should a window ever break, Reflective Silver protects you

And your family from flying glass fragments by holding the glass together.

Fig. 3: Silver sheet reflection on solar panel

Fig.4: Parabolic silver sheet reflection

Silver reflectors are produced high intensity compared with the mirror reflectors. Silver is low cost compared with other reflecting and easy process for arrangement. Silver reflectors power consumption is more compared with mirror reflector. Silver reflector shining is more than mirror reflector.

Tilt Sensor with Arduino:

The most common tilt sensor is a ball bearing in a box with contacts at one end. When the box is tilt the ball rolls away and the contact is broken. When the bos tilted to roll the other way the contact is restored since the ball touches the contacts. In this way, the tilt sensor uses the ball as a switch that is turned on or off depending on its inclination. The tilt sensor will give digital information to the Arduino, either a HIGH or LOW signal.

Fig.5: *Tilt Sensor*

Tilt sensors are sensitive sensors and detect movement of around 5 to 10 degrees. To determine if something is shaken, you will need to check how it's been since the state of the tilt senor is changed. If it has not changed for a time you consider significant, the object of the tilt sensor is not shaking.This way, the tilt sensor acts like a switch that is turned on or off depending on its inclination. So, it will give digital information to the Arduino, either an HIGH or a LOW signal.

III. CASE STUDY

There are many problems in power consumption by using Solar PV modules and different types of PV modules are using in different PV system. Like fixed, tracking system but the shading effects, tracking problem in solar PV system environmental effects, season effects, radiation effects, price problems.

The details of problems in solar PV systems are as follows:

- Power consumption is not possible in all the seasons.
- Mainly solar panel are depends upon the sun light. But it will change due to environmental conditions like clouds, etc.
- Tracking system are developed to cover the environmental conditions. But the tracking systems arrangements and maintenance are very difficult and also very expensive.
- Not only the environmental conditions and due to shading effects also panels will not consume the power
- Recently reflection systems are developed those are mirror reflection or boosting system & silver or aluminum reflection system. But problem with the mirrors are maintenance and arrangement processes are difficult with the change of the environmental effects
- Another main problem is radiation problem when power consumption increases.

Till people are trying to reduce the radiation problems.

To overcome all the above problems with better maintenance, the present Solar Photo Voltaic (PV) system will support. To increase power generation, silver reflective solar photovoltaic panels are used. For reducing the radiation effect, such systems must be placed over water resources such as rivers or lakes or water tanks. Silver coated sheets are fixed around the panel to absorb more sunlight throughout the day, and light intensity is monitored using a tilt sensor and Arduino.

IV. PROPOSED SYSTEM

This paper mainly targets both power consumption and reduction of the radiation effect. .

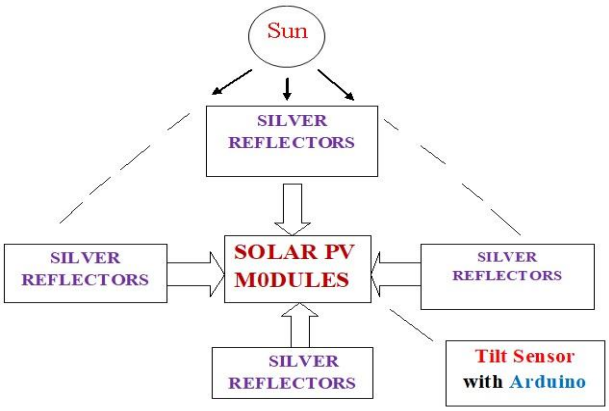

Fig.6: Silver Reflective Solar Photovoltaic System

Step-I: Design:

To increase power generation, silver reflective solar photovoltaic panels are used. So silver coated sheets are fixed around the panels to absorb more sun light entire day. For this 5 W of low rating Solar Photo voltaic panel number in two are used which is easy-to-use mechanism. But the amount of energy generated by solar panels is closely related to the amount of solar radiation. So to reduce the radiation effect, such systems must be placed over water resources such as rivers or lakes or water tanks. Hence the silver reflective solar photo voltaic system is placed on the water tub as shown in the fig 7.

Fig.7: Reflection process

Step-II Testing procedure:

This Silver Reflective Solar PV system tested in the following ways:

1. Test the each module individually and Note down the readings of Voltage and Current.
2. Set the silver to sun light around the solar PV modules silver reflection should be appeared on the solar PV module arrange the as shown in fig 8 and note down the voltage and current readings in different combinations such as series and parallel.

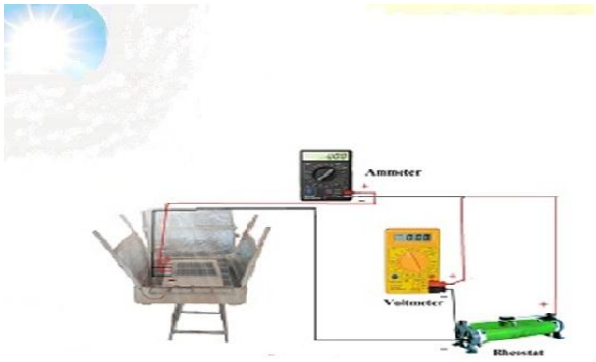

Fig.8: Silver Reflective Solar PV system

3. Calculate Efficiency and the Fill Factor and using below formulas:

$$\text{Efficiency} = \frac{\text{Pmax}}{\text{Area} * \text{Intensity}} * 100$$

$$\text{Fill factor} = \frac{\text{Vmp} * \text{Imp}}{\text{Voc} * \text{Isc}} * 100$$

Step-IV: Programming the Arduino Nano:

The arrangement of the Silver Reflective Solar PV system with Arduino is as shown in fig 9.

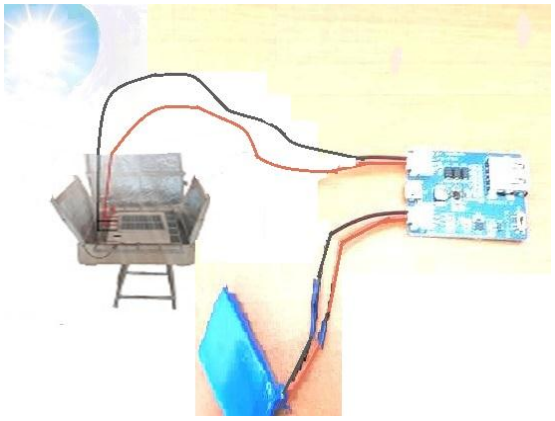

Fig.9: Silver Reflective Solar PV system with Arduino

1. To calculate the possible magnitude of solar energy, here used the light intensity values as a substitute for solar radiation in the formula.
2. So to calculate the magnitude of solar energy approximately the formula is used as below.

*E = A * r * H * PR* is the formula is used for calculating the magnitude of solar energy approximately, where:

A is the area of the solar panel,

r is the efficiency,

H is the average solar radiation and

PR is the performance ratio or coefficient (generally 0.75).

3. Of course, this method does not provide exact solar energy values, but to determine thresholds levels (Low, Moderate, and High) for detecting the performance in a given direction.
4. To show performance levels different colors of LED's red (Low), yellow (Moderate), green (High) - for each direction are used.
5. It is crucial to place the device perpendicular to detect light intensity accurately, so used a tilt sensor (mercury sensor) to check if the device moves into a tilted position. The total setup of proposed system is as shown in fig10.

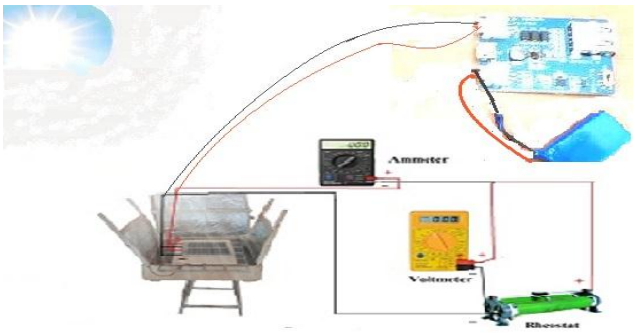

Fig.10: Silver Reflective Solar PV system with tilt sensor using Arduino.

Step-V: Programming steps are:

a) Define indicators (red, yellow, green) for each direction.

b) Define LDR pins for each direction to gather light intensity values.

c) Define the tilt sensor pin.

d) Define the solar panel (SP) specifications, which differ amid different brands. So, change these variables with that of your solar panel.

e) Define thresholds by experimenting.

f) In the *get_Light_Intensity ()* function, gather light intensity data from photo resistors.

g) In the *Tilt ()* function, get notified if the sheets moves into a sloping position.

h) Initiate threshold detection (Low, Moderate, and High) for each direction.

i) In the *Indicate_Thresholds()* function:

j) Print the selected direction with its solar energy value.

k) Adjust threshold indicators (LEDs) according to solar energy values for each direction.

Advantages:

1. Silver reflectors are light in weight.

2. Power consumption is high.

3. Radiation can be controlled by placing on the water sources

4. Maintenance cost is less.

5. It will work similar to that of a solar tracking system.

Applications:

1. It can be used in world wide.
2. It can be applicable in rooftop systems, by placed on the available water sources for house hold appliances and industries etc.
3. The Silver Reflective Solar PV system power plant can be established on the rivers, oceans and water sources etc.

V. RESULTS

Schematics:

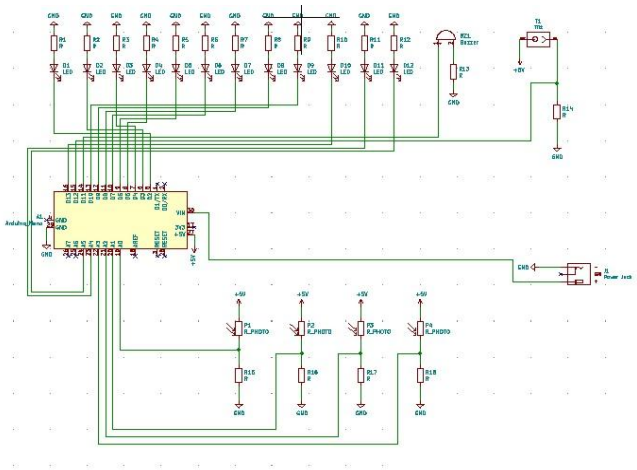

Fig.11 Schematic diagram of Threshold levels absorption

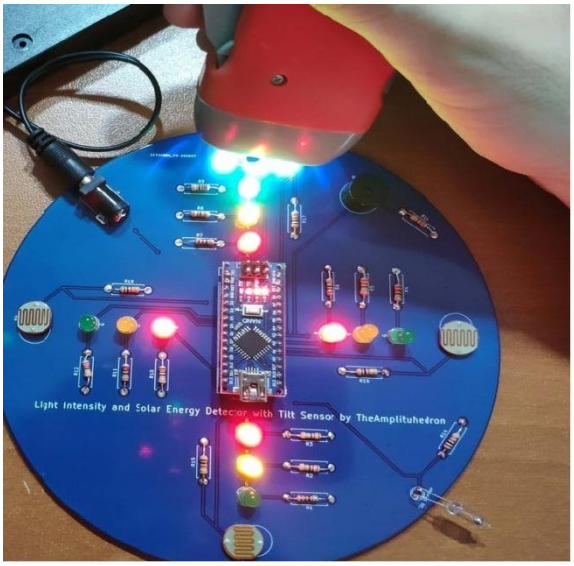

Fig.12.Testing of performance levels Low (Red), Moderate (Yellow) High (Green) in each direction

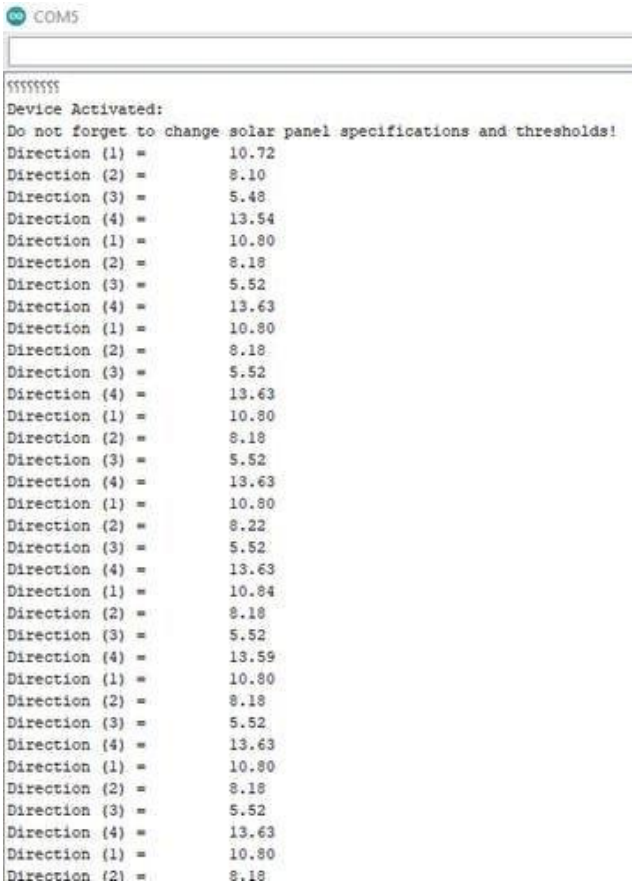

Fig.13. The magnitude of solar energy for each direction on the serial monitor by Arduino

B: VI-Characteristics of Silver Reflective Solar PV System:

The performance of Silver Reflective Solar PV System is observed entire day in different methods one is with & without silver reflectors for power generation and by placing and without placing the above setup on the water tub using the combinations of (Series and Parallel).

The details results are shown in the following table forms and VI characteristics graphs.

Table 1: Series connection without reflector

Complete day

S.NO	Series connection without reflector								
	Morning			Afternoon			Evening		
	voltage	Current mA	Power X 10^{-3} w	voltage	Current mA	Power X 10^{-3} w	voltage	Current mA	Power X 10^{-3} w
1	0	92	0	0	100	0	0	94	0
2	0.22	86	0.018	0.24	90	21.6	0.23	88	0,024
3	0.29	74	0.021	0.3	80	24	0.32	76	0.025
4	0.38	65	0.024	0.4	70	28	0.39	68	0.028

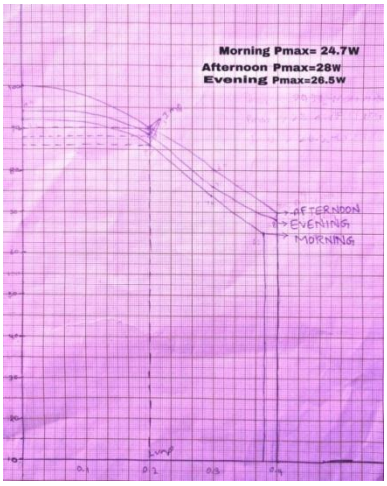

Fig.14.VI characteristics of Series connection without reflector

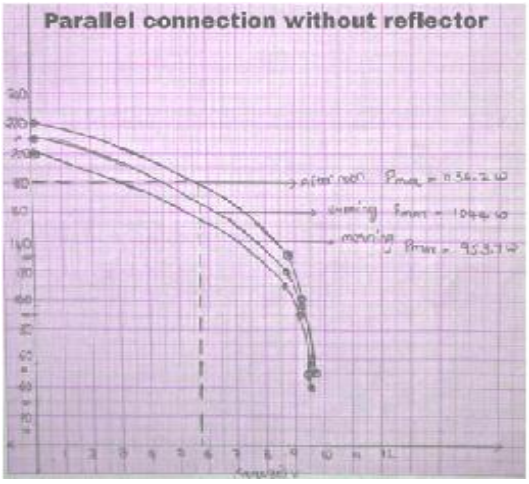

Fig.15.V-I characteristics of Series connection without reflector

Table 1: parallel connection without reflector

Complete day

S.NO	Parallel connection without reflector								
	Morning			After noon			Evening		
	voltage	Current mA	Power X 10^{-3} W	voltage	Current mA	Power X 10^{-3} w	voltage	Current mA	Power X 10^{-3} w
1	0.01	200	2	0.01	220	2.2	0.01	210	2.1
2	8.67	110	953.7	8.74	130	1136.2	8.7	120	1044
3	9.1	90	819	9.2	100	920	9.16	96	879.36
4	9.4	50	470	9.59	60	575.4	9.5	55	522.5
5	9.5	40	380	9.57	50	478.5	9.53	46	438.38

Complete day

Series connection with silver reflector

S.NO	Morning			Afternoon			Evening		
	voltage	Current mA	Power X 10^{-3} w	voltage	Current mA	Power X 10^{-3} w	voltage	Current mA	Power X 10^{-3} w
1	0.01	360	3.6	0.01	380	3.8	0.01	370	3.7
2	1.05	350	367.5	1.08	370	399.6	1.06	360	381.6
3	1.5	340	510	1.53	360	550.8	1.52	350	532
4	1.94	340	659.6	2.01	360	723.6	1.92	350	672
5	2.4	340	816	2.6	360	936	2.5	350	875
6	14.75	310	4572.5	14.85	320	4752	14.82	315	4668.3
7	15.22	290	4413.8	15.42	300	4626	15.32	296	4534.72
8	16.1	240	3864	16.25	250	4062.5	16.18	245	3964.1
9	16.63	180	2993.4	16.73	200	3346	16.69	190	3171.1
10	17.01	130	2211.3	17.11	150	2566.5	17.09	140	2392.6
11	17.4	80	1392	17.48	100	1748	17.44	90	1569.6
12	17.42	80	1393.6	17.47	100	1747	17.45	90	1570.5

Table 2: Series connection with reflector

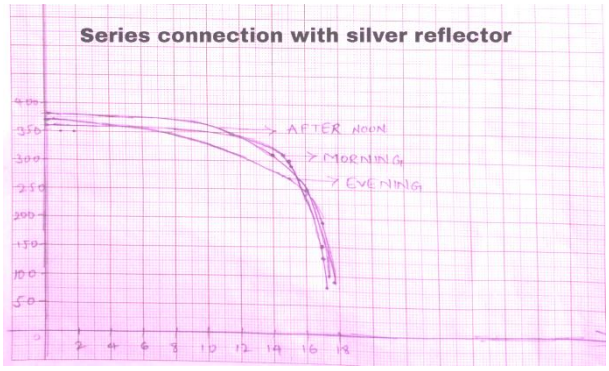

Fig.16.V-I characteristics of Series connection with reflector

Table 3: Parallel connection with reflector

Complete day									
Parallel connection with silver reflector									
	Morning			**Afternoon**			**Evening**		
S.NO	**voltage**	**Current mA**	**Power X 10^{-3} w**	**voltage**	**Current mA**	**Power X 10^{-3} w**	**voltage**	**Current mA**	**Power X 10^{-3} w**
1	0.02	840	16.8	0.02	860	17.2	0.02	850	17
2	0.5	820	410	0.55	840	462	0.53	830	439.9
3	1.47	800	1176	1.57	820	1287.4	1.52	810	1231.2
4	2.85	790	2251.5	3	810	2430	2.89	800	2312
5	7.64	680	5195.2	7.72	700	5404	7.69	690	5306.1
6	8.07	480	3873.6	8.12	500	4060	8.1	490	3969
7	8.25	380	3135	8.34	400	3336	8.3	390	3237
8	8.48	280	2374.4	8.52	300	2556	8.5	290	2465
9	8.73	80	698.4	8.88	100	888	8.81	90	792.9
10	8.9	40	356	8.94	50	447	8.92	45	401.4

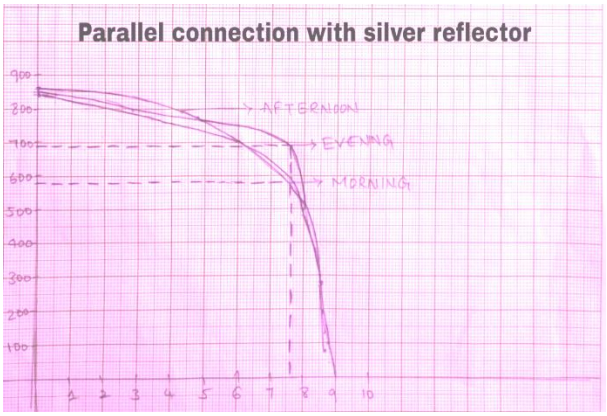

Fig.16.V-I characteristics of Parallel connection with reflector

Complete day			
Silver reflector in parallel connection with low radiation			
S.NO	**voltage**	**Current mA**	**Power X 10^{-3}**
1	**0.08**	**690**	**55.2**
2	**4.19**	**590**	**2472.1**
3	**8.72**	**530**	**4621.6**
4	**8.92**	**430**	**3835.6**
5	**9.04**	**330**	**2983.2**
6	**9.18**	**230**	**2111.4**
7	**9.31**	**150**	**1396.5**
8	**9.34**	**100**	**934**
9	**9.36**	**50**	**468**

Table 4:Silver reflector in parallel connection with low radiation (on the water source):

VI. CONCLUSION

In this paper a new technique is presented to increase the power consumption with minimization of the radiation effect of silver reflective solar PV system. Silver sheet should be fixed in an angle between 45 to 60 degrees or convenient direction around the solar panels, but the amount of energy generated by solar panels is closely related to the amount of solar radiation. So to reduce the radiation effect, such systems must be placed over water resources, but the problem is water is not available in every season so it can be placed on rivers, oceans, ponds and other water sources. Another problem is Silver sheets, these can be easily tearing so, by using the silver coating glasses or standard material and silver coating methods can apply.

Silver reflective solar PV system will work similar to that of a solar tracking system. Solar energy is detected with continuous observation of threshold levels values of voltage and current during the day time using a tilt sensor and Arduino.The output power is recorded in various combinations. The results prove that power consumption increases 40% by using the Silver Reflective solar PV system with a low radiation process. Thus, the proposed system is cost-effective with increased panel efficiency.

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Synthesis and Study of Spin-Lattice Coupling in $DyMnO_3$ Multiferroics

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Abstract—Multiferroics is a term associated with materials that show both ferro/antiferromagnetic and ferroelectric properties and the occurrence of these two properties simultaneously is unique to multiferroics. Multiferroics have potential for applications as actuators, switches, magnetic field sensors, magnetocaloric materials and latest type of electronic memory devices. Few examples for single phase multiferroics are Boracites ($M_3B_7O_{13}X$), Bismuth-based compounds, $RMnO_3$, $BaMF_4$ etc. Among these materials, the rare-earth manganites $RMnO_3$ (R = Dy, Tb, Gd, Sc, Er) are interesting due to their coupling between the ferroic orders, on account of their improper geometrical structure. A polycrystalline $DyMnO_3$ was prepared through the citrate-gel method and the sample crystallized in orthorhombic perovskite structure. A systematic investigation of specific heat studies were carried out over the temperature range 4–80 K. A low temperature dielectric study also was performed on this sample over the temperature range of 8-50K at 1kHz frequency. Based on these studies, the sample is exhibiting three transitions at 40K, 20K and below 10K with different origins. The mechanism causing this type of multiple transition has been discussed in the paper.

Key Words— Multiferroics; Heat Capacity; Low Dielectric Constant

I. INTRODUCTION

Multiferroics are the materials that have strong interaction between magnetic, electric, and elastic orderings. It opens wide opportunities in designing the new devices [1,2]. If ferro/antiferro magnetism and ferroelectricity exist in the same material then those are called magnetoelectric materials. In fact, it is very hard to find materials that are magnetic as well as ferroelectric in the same phase [3]. Most of the multiferroic materials are $RMnO_3$ [R is rare earth metal like Dy, Tb, Eu, La, etc,] and other multiferroic compounds are $BiFeO_3$, $BiMnO_3$ RMn_2O_5, etc,[4]. Multiferroics are two types based on their origin of ferroelectricity and they are type-I and type-II. In type-I materials, the ferroelectricity and magnetism properties turn out at different temperatures due to different mechanisms. The structural distortion occurs at high temperature which gives rise to ferroelectricity, while magnetic ordering sets at low temperature. In Type-II Multiferroics, the metal ions having empty d-orbitals or cations with partially filled orbitals causes magnetic order is which leads to Ferroelectricity.

$RMnO_3$ multiferroics (R=Gd, Tb, Dy, Ho, Y, Lu) are orthorhombic or hexagonal depending on the ionic radius and synthesis conditions. Among all these $RMnO_3$ multiferroics, $DyMnO_3$ formed in orthorhombic and hexagonal structures depending on the synthesis conditions [5]. In orthorhombic $DyMnO_3$, a complex spiral spin order breaks the inversion symmetry, which leads to ferroelectricity [6,7]. The magnetically driven transitions occurred at much lower temperatures. Samantaray et al., [8] studied the room temperature and low temperature dielectric constant of $DyMnO_3$ ceramic, in their investigation the sample exhibits a ferroelectric transition at room temperature.

In the present investigation spin-lattice coupling between the magnetic and ferroelectric origins are explored in a polycrystalline $DyMnO_3$ sample through, heat capacity and low temperature dielectric constant studies. A low temperature ferroelectric transition has been observed in $DyMnO_3$ polycrystalline sample at around 28K and the results are discussed in the paper.

II. EXPERIMENTAL DETAILS

2.1 Synthesis and Characterization

The sample of multiferroic material with compositional formula $DyMnO_3$, has been prepared by most prominent citrate-gel method. In this method, the primary compounds are pure Dy_2O_3 and freshly prepared $MnCO_3$ taken in a stoichiometric ratio and dissolved in Nitric acid separately. Further, the solutions were shifted into a beaker, placed on a stirrer with hot plate, and mixed for 30 mins. Citric acid has been added in the ratio 1:1 to the solution.

Further, the pH value of the solution was adjusted between 6.5 and 7.0 by adding ammonia solution and allowed it to stir on hot plate until it reaches the one third of the solution. Later, by adding ethylene glycol solution in 1: 1.2 proportion and again heated on a hot plate between 150 - 180^o C for gelation. On further heating, a fluffy porous mass is obtained in the beaker and is grinded. The compound was calcined at 1000^{0}C for 4hrs. The acquired black-colored powder was made into pellets with a diameter 10 mm and thickness 1.5 mm by applying hydraulic pressure of 2 to 3 tons per sq. inch and finally sintered at 1300◦C for 4hrs.

The structural characterization of the pellets was carried out by the powder x-ray diffractometry (XRD), using Bruker AXS D8 Advance diffractometer with Cu-K α source of

wavelength 1.54A°. The XRD data has been analysed by Rietveld refinement using Fullprof software. The specific heat measurements were also carried out by the semi-adiabatic heat pulse method with an absolute accuracy of 0.5% in the presence of 0, 2, and 5 T fields. Finally, the dielectric permittivity was determined using Novo control Alpha-a high frequency analyzer at 1kHz frequency in the temperature range of 4-50K.

III. RESULTS AND DISCUSSIONS

The structural exploration of the sample was characterised by using X-Ray Diffraction and the XRD data were analysed using the Rietveld refinement technique. The XRD results are shown in figure 1(a) and from the figure, it is seen that the sample structure is orthorhombic with *Pnma* space group. The lattice parameters have been determined by using Rietveld analysis and the values are as follows a = 5.83 A°, b =7.38A°, and c = 5.28 A°. The pseudo-Voigt function was used for suitable peak profiles. The experimentally observed and calculated Rietveld refined patterns of $DyMnO_3$ along with difference of both the patterns are shown in figure 1(b). The results are in good accordance with the literature [5]. It was confirmed by the analysis of XRD data that samples are in single phase crystal with lattice parameters values obtained a = 5.83 A°, b =7.38A° and c = 5.28 A° respectively without any detectable impurity.

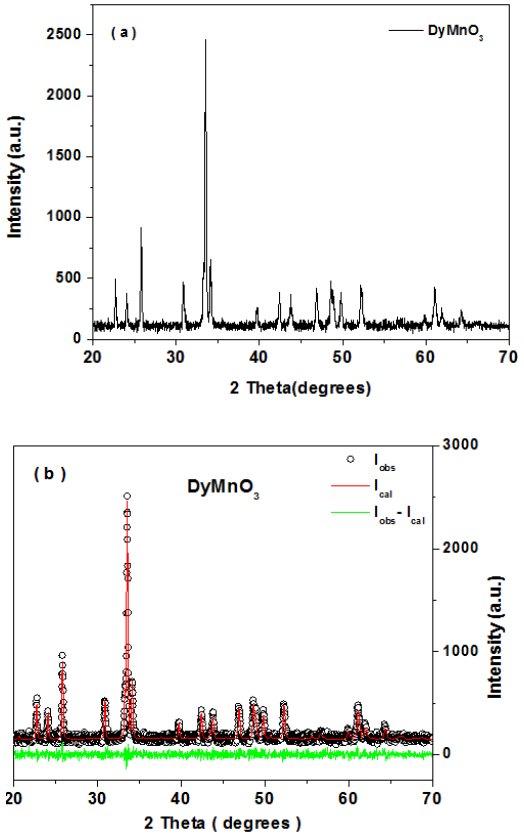

Figure 1: (a) XRD of DyMnO3 sample. (b) Rietveld refinement pattern of DyMnO3 samples.

Figure 2 shows the variation of CP /T with temperature. It can be seen from the figure that sample exhibits three distinct anomalies at 38K, 18K, and 7K. On decreasing the temperature 50K, an anomaly has been observed at 38K which is a consequence of the sinusoidal arrangement of Mn^{3+} ions[9]. At this temperature, Mn^{3+} ions are ordered from disordered state. This is an antiferromagnetic transition from paramagnetic state. On further decreasing the temperature, another anomaly has been ordered at 18K. At this temperature, sinusoidal ordering of Mn^{3+} ions breaks and it converts into spiral ordering. It is attributed to paraelectric to ferroelectric transition where the centre of symmetry breaks. Following these, $DyMnO_3$ exhibit another transition at low temperatures (below ~10 K) and are alike to the Schottky contribution generally observed in rare-earth compounds due to the crystal field effect [10]. Therefore, the broad hump below ~10 K indicates the ordering of rare-earth ion spins. Similar results are observed in literature in single crystalline $TbMnO_3$, $GdMnO_3$ and attributed the same reasons [5, 9].

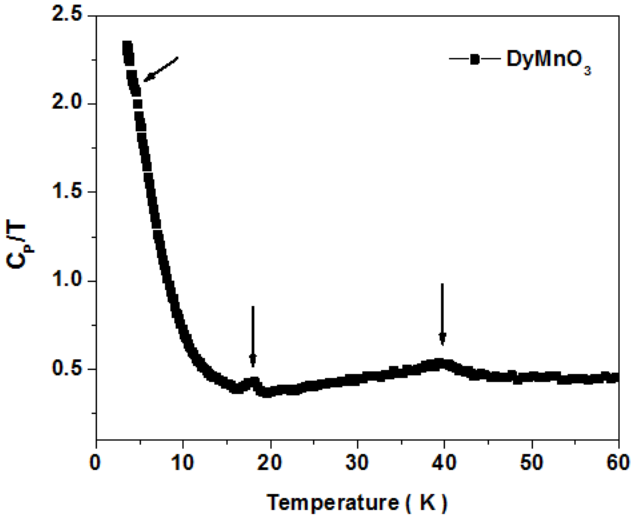

Figure 2: Variation of Cp/T with temperature

Figure-3 shows the graph of dielectric constant versus temperature at 1 kHz frequencies. It has been observed that there is a slight change in dielectric constant values with the frequency. As the temperature decreases from 50K, dielectric constant values are found to increase and an abnormality has been observed at 18 K. It is matching with the irregularities in heat capacity studies. This is a paraelectric to ferroelectric transition at 18K [7]. It is well known that ferroelectricity arises when there is a break in centre of symmetry. At this temperature, a change from sinusoidal ordering of Mn3+ ions is changes to spiral ordering which breaks the symmetry. The break in centre of symmetry leads to the polarization and dielectric constant. This indicates the strong spin-lattice association between the magnetic and ferroelectric orders.

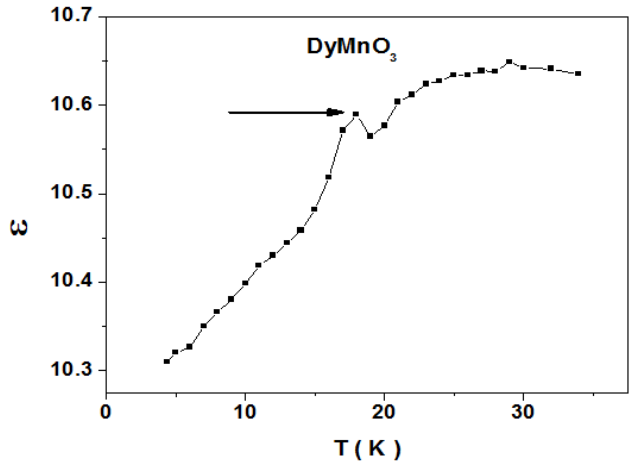

Figure 3: Variation of frequency with temperature

IV. CONCLUSIONS

Polycrystalline $DyMnO_3$ has been prepared by citrate-gel method. X-ray diffraction results revealed the orthorhombic structure of the sample and there are no secondary phases. Heat capacity measurements disclose the multiple transitions in the material at 40K, 18K and below 10K are attributed to the ordering of Mn3+ and Dy3+ ions. Low-temperature dielectric constant studies revealed a ferroelectric transition at 18K. It is well matching with the heat capacity results.

Acknowledgements:

Authors thank Dr. A.M. Awasthi for providing low temperature Dielectric permittivity facility. Authors also thank Dr. R. Rawat and Pallab Bag in heat capacity measurements.

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Smart Highway Electronic Toll Collection Using RFID Technology

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Abstract—Smart highway toll collection system is introduced as a solution of the traffic problems and also to maintain transparency in the toll collection system. The proposed system aims to make a digital toll collection system which can eliminate the delay on toll roads, toll bridges and toll tunnel without cash and without requiring cars to stop.

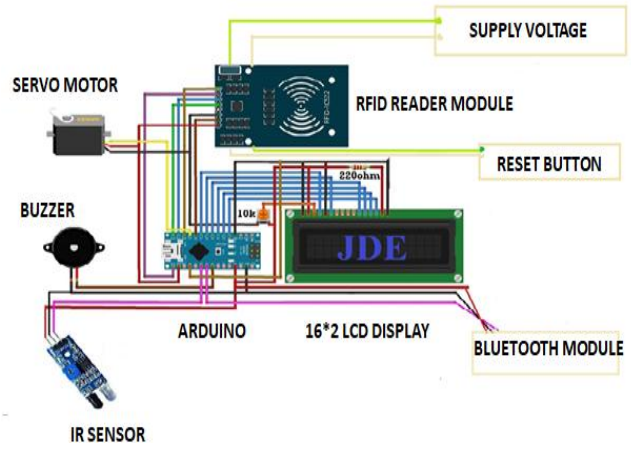
RFID tag contains all the basic information as well as the information related to the amount paid for the TOLL collection. An appropriate amount is deducted from the registered account automatically. In case if one has insufficient balance, his updated balance will be negative. This is an alarming system is used which alert the authority that this vehicle does not have sufficient balance and particular vehicle can be identified; this approach is quite user-friendly and time saving, less fuel consumption and also contributing in saving of money.

Key Words— RFID, Unique ID, Toll Gates, Electronic Tag

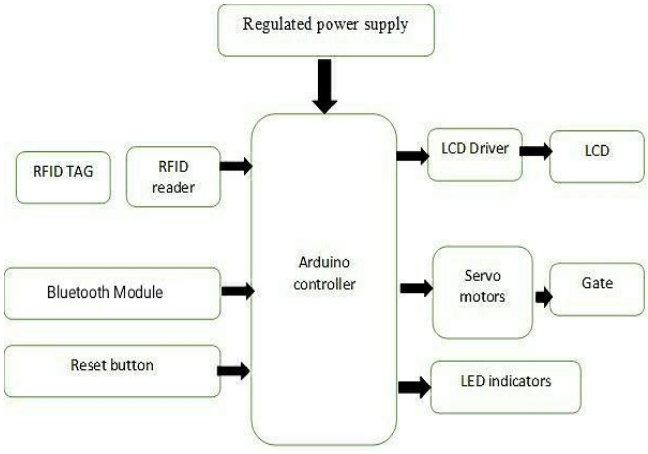
I. INTRODUCTION

In these days traffic problem is a very severe problem in our country. In many countries, every day we have to face traffic jam for several hours which is very annoying at the same time creating a huge trouble in our daily life. Traffic jam mainly causes for reckless driving and also for the rash of the vehicles in the road. For the reduction of traffic problem government has made many bridges, fly over's and bypass roads. People have to give toll when they pass these by any vehicle. Unfortunately, the toll collection system is manual in our country which takes many times to pass the vehicles and creating traffic jam. Here we introducing Electronic toll collection system using RFID technology which will be an automatic system, will not stop the vehicles as well as this system will help to reduce the traffic jam. Here, the payment will be taken from the bank account of the vehicle owner and he will receive a message from the server that the toll payment has been taken. In addition, our system will also help to solve the traffic severe crashes, which is mainly caused by over speeding as here we have used speed breaker to slow down the speed of the vehicles when RFID tag will read the information of the vehicles. The project is used to provide an efficient solution for automatic toll gate control and toll collection for high ways using RFID tag. The project makes use of a atmega328p microcontroller, which acts as a central controlling unit. This module is capable of communicating with the input and the output modules. The user initially has to deposit money in the RFID tag. When RFID reader reads the tag values and money is deducted from the RFID tag. As and when the amount is deducted, the gate opens which is done by the servo motor used for closing and opening of toll gates. LCD is used to display the status of gate and the transaction details. The Arduino Microcontroller is programmed using Embedded C language.

II. 2. DESIGN:



III. BLOCK DIAGRAM



IV. COMPONENTS

1. Regulated Power Supply.
2. Arduino UNO Board
3. RFID reader.

4. RFID tag.
5. Servo motor
6. Reset.
7. Bluetooth module
8. LCD display with driver.
9. LED indicators.
10. Transformer

Table: Equipment Specification.

Name	Capacity	Quantity	Code
Regulator	7805	1	U1
Regulator	7812	1	U3
Capacitor	1000 µf	1	C1
Capacitor	10 µf	1	C2
Ceramic Capacitor	22 pf	2	C3, C4
Diode		4	D1, D2, D3, D4
Push Button		1	
dc motor	100 rpm	2	
LCD	16*2	1	
40 Pin Base		1	U2
16 Pin Base		1	U4
8051(AT89S52)		1	
L293D		1	
Bluetooth	+3.3VDC 50mA	1	X1
LED		1	D5

V. WORKING

In our project, we have a vehicle equipped with RFID tag and computer connected to Transceiver positioned at the Toll station. Whenever the vehicle enters into the coverage area of transceiver, it locates the tag and decodes the code assigned to that particular tag. After receiving the code, it is forwarded to the computer situated at the Toll station. The computer then recognizes the code and automatically access the database and if the vehicle has its valid prepaid account at the toll station, the appropriate toll is deducted from that account and the gate is opened to allow the vehicle to pass. And if the vehicle doesn't have a valid prepaid account or it is not a daily traveller, it will have to pass through a manual check post which will be in another lane. By using the database we can with very less memory requirement.So this reduces ttne time at toll gate and vehicle can pass the toll gate with minimum 10Kilo meters per hour speed without any stop and we can save the fuel consumption .Here we have placed a Bluetooth module to get an alert message to the user to know the deducted amount.

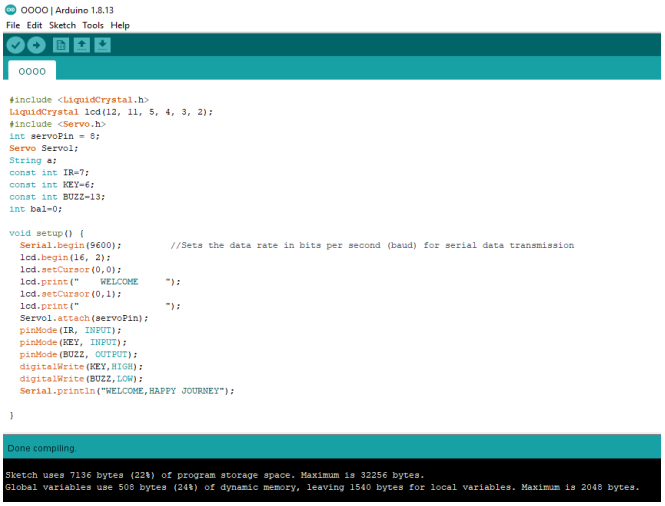


Fig: Code execution in arduino Software

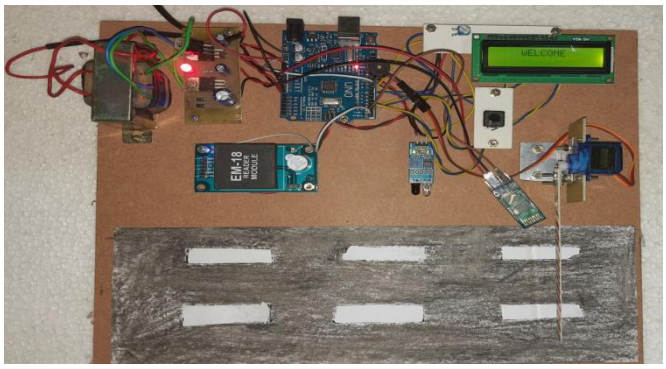


Fig: Intially at Toll Gate

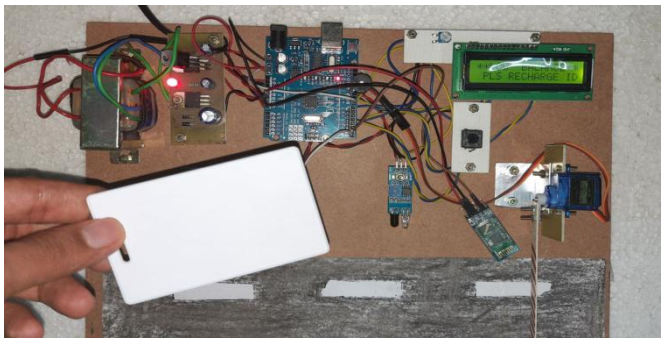


Fig:RFID Reader Reading RFID Tag

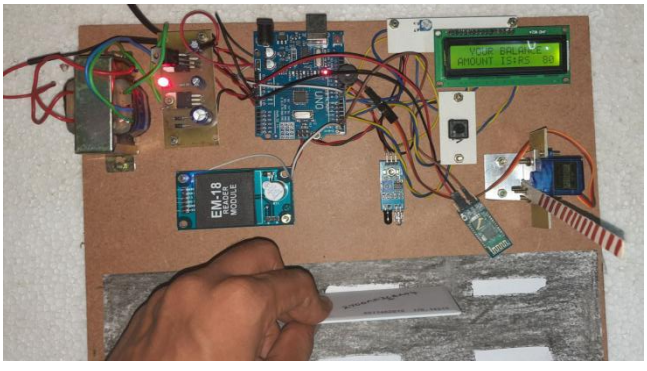


Fig:After reading ,if succesfull, Toll gate is opened

VI. RESULTS

VII. CONCLUSION

Times are changing and even this Manual in mind set of every individual this technology Toll at the Toll station won't be that time of the globe wherever there would be a don't think that its not that far enough benefiting the whole society as well as RFID is a powerful technology, and it is technological advancements of RFID across different market segments. Comparing advantages and limitations travellers and Toll station authorities to and innocuous technology on the surface, its successful, wide-scale deployment. sensor network technologies will help interactions with the people and customers.

Each Tag has different change and seeing a change And we would see that paying across every nook and corner merits of this Toll station we used in India and in terms taxation. the coining years. Continuous and maintenance of devices system is beneficial for daily scowl to be a fairly simple be explored and resolved for RFID and future upcoming manufacturing processes and thewith the people and customers. On the concluding node, we have successfully implemented our project, but still have some advancement to be done.

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Study the Impact of E-Commerce on Indian Economy

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Abstract—The paper uncovers the significance of ecommerce in Indian economy. As we as a whole realize India is among the quickest developing economy of the world, in this manner it is especially critical to have government mediation and tremendous venture inflow in type of Foreign direct interest in substantial economy like India to balance out and increment the development of ecommerce industry in the economy. In India with the digital economy entrance has expanded essentially, as per measurable information web use has expanded to 429.23 million client in India and is relied upon to stretch around 830m by year 2021 ."There has been huge ascent of web based business in India, as India's web economy is 125 billion dollar in 2017. In this paper we will look towards the job of government in ecommerce industry and furthermore look towards the different obstructions of web based business in Indian aspects."In this exploration paper we will speak basically about B2C Ecommerce and its level of total national output in Indian economy.

Key Words— E-Commerce, E-Business, Economy, Growth, India , FDI, GST, GDP

I. INTRODUCTION

Today web based business has turned into an imperative piece of day by day life. Availability to web based business stages isn't a benefit yet rather a need for the vast majority, especially in the urban regions. There are elective web based business stages accessible (rather than the conventional physical stages) for pretty much every part of our lives, beginning from acquiring of ordinary family unit things to online financier." As in 21st century as web has turned out to be most critical and as often as possible and most need gadget, it will doubtlessly race to accomplish more development and deals by means of web. "As per e-Marketer, overall retail Ecommerce deals will reach $1.915 trillion before the finish of 2017. with increment in digital infiltration the whole way across the globe and shoddy and continuous simple accessibly of web, it is inclined to expand the development of ecommerce all over the world, then part of customary individuals are very stressed and strained with change in example of offer through web", with the accessibility of shabby and rapid web with assortment and security alternatives, parcel of individual and firms have associated their business with e-commerce. (As in late world it is exceedingly difficult to develop without being accessible online. Consequently to develop more and win higher benefit it is exceptionally prescribed to have legitimate structure accessibility and simple openness of online destinations, in light of the fact that it not just decides benefit and no. of clients yet additionally decides the positioning and position of enterprise of the firm in general business world.

Likewise in this examination paper I will centered about the development and example of web based business in India and its deals and effect in Indian economy, of every extraordinary kind of online business, my exploration paper confines its investigation to for the most part b2c sorts of business, however it covered different sorts of web based business and its social effect additionally in India by means of offers of web based business in India.

In this way there is huge ascent in offer of retail web based business throughout the years and as indicated by e-Marketer retail internet business deal by 2020 should achieve more than $4trillion. With above figure we can without much of a stretch see how visit and sudden the difference in deals design is world as all the significant economies are moving towards internet business deals.

II. WHAT IS E-COMMERCE?

There is no general definition of electronic commerce , but generally e-commerce is defined as E-commerce (electronic commerce or EC) is the buying and selling of goods and services, or the transmitting of funds or data, over an electronic network, primarily the internet but also all other activities which are associated with any transaction such as:

• Delivery

• Payment facilitation,

• Supply chain and service management, can also be categorized or put under this section of economy.

E-commerce increases the growth of online business. It can be categorized under

1. Online marketing
2. Online advertising
3. Online sales
4. Product delivery
5. Product service
6. Online billing
7. Online payments

Thus, electronic commerce deals with all the work loads related to internet. It also describes the exchange of data between the financing, billing and payment aspects of e-business transactions. Generally e-commerce and e-business are used interchangeably."

DIFFERENT TYPES OF E-COMMERCE

There are different types of e-commerce; we will examine five basic types of e-commerce in this research paper-

BUISNESS – TO-BUISNESS (B2B) – it comprises of all electronic transactions of good or services conducted between 2 companies. This type of e-commerce includes intra system and electronic markets.

BUISNESS TO CUSTOMER (B2C) – This transaction carried out in the retail trade with individual buyers. This typical buyer of any store on the site is a consumer or a buyer

CUSTOMER TO CUSTOMER (C2C) – in this type of e-commerce consumer sells its product directly to consumer

CUSTUMER TO BUISNESS (C2B) – In this classification of e-trade, singular customer of merchandise or administrations pitches their item to association.

BUISNESS TO GOVERNMENT (B2G) – In this web based business segment it bargains of trade among organizations and open segment is recorded.

III. OBJECTIVE OF STUDY

India is one of the largest growing economies of the world. There is heavy use of internet among Indian citizens.

The main basic objective of this research paper are-

1. To analysis the present trends of e-commerce in India

2. Government initiatives and different scheme in growth of e-commerce in India

3. Impact of e-commerce on literacy rate and employment rate in India

IV. RESEARCH METHODOLOGY

Method of Data Collection: Secondary data – various research papers of similar type have been referred to check the format and the type of graphs for analization of data .Other than this, various scholar and data from other certified bank and source are used to collect data which is interpreted further for data analysis

Type Of Research Design: The research is descriptive and exploratory research . Descriptive in the sense that it establishes relationship between literacy rate of the country and given parameter. Exploratory research in the sense that it collects data from various parameters and tends to establish a cause and effect relationship between the parameter.

1. PARAMETER: - Different parameter is used to establish relationship between the indicators. Literacy rate, m-commerce sale, growth of internet, unemployment rate and other such indicators are used to establish clear understanding about indicators.

2. DATA REPRESENTATION:- The data collected is represented in form of Table, graph, pie charts and X-Y graphs.

3. DATA TECHNIQUE – To establish clear understanding and relationship among indicators SPIERMAN RANK CO-RELANTION AND PEARSON CO- RELATION is used in this research paper.

V. SNAPSHOT OF E-COMMERCE INDUSTRY IN INDIA

E-commerce in India is fastest growing economy of the world. Indian E-commerce is growing at an annual rate of 51%, the highest in the world and is expected to jump from $30b in 2016 to $120billion by 2020) (source–assocham–forrester study paper).With $680b in online retail sales in 2016, china is largest E-commerce market globally, followed by United States and then India In India though there were use of e-commerce even before 1990s, but their contributions were significantly negligible. Recently a lot of blue chip PE firms have invested huge money on India e-commerce as there is significantly huge potential and opportunity to success. In India 100 percent FDI is permitted in B2B e-commerce and thus shows the government intention and contribution towards e-commerce industry in India. The growth of e-commerce in India highly dependent n the following sub factors that do have an impact on Indian economy when it comes about e-commerce industry in India" .some of these factors are–

1. Participation of niche companies in online trading

2. Unmatched FDI

3. Uniform GST

India is one of the biggest developing economies of the world. There is substantial utilization of web among Indian natives.

The fundamental essential target of this exploration paper are –

1. To examination the present patterns of online business in India

2. Government activities and diverse plan in development of online business in India

3. Impact of online business on education rate and work rate in India

With the expansion in number of cell phone and great availability of web it is in this manner much required factor to build web based business impact in the Indian economy. The above diagram portrays increment in digital infiltration in India, from 30% in 2014 not out of the ordinary 64% by 2019, Availability of extensive number of electrical apparatuses and its positive impacts has guided towards such an expanding pattern .With the expansion in digital entrance, it in this manner as indicated by (analyst) that we should realize where did the populace, what they did with the increment of digital entrance increases. Along these lines as indicated by analyst reports, Indian digital individuals in Jan 2017, distinctive ordered individuals went under various subsections which by and large affected internet business in India.

VI. CONCLUSION

Through the investigation of research paper we came to know how vital web based business industry right now on the planet is. With setting of India we likewise attempt to locate the upward pattern of development of web based business in India, and furthermore increment in m-begin and digital infiltration in India. Government policies and activities has additionally lead to increment of online business in India over years. As indicated by review after demonetization, job of cashless economy in India has expanded fundamentally, hence the job of web additionally similarly other such government policies have likewise had a noteworthy effect. A ton have been done and a great deal must be done with regards to web based business industry in India. Likewise we think about effect of education rate and joblessness rate on the development of internet business industry in India. Likewise there is noteworthy need to expand the education rate in India and furthermore spread mindfulness among rustic individuals in India about cashless economy and job of web in India in today's world.

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Study of Work Life Balance of Married Working Women: A Review

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Abstract— Many of the women have drowned themselves in the race of earning. In order to succeed, grow and enhance their professional academia they often ruin their social and emotional context, perhaps, it leads to unbalanced work life balance. The literature identifies its effect on various quality life conditions like distraction from work, disturbing the professional and personal life of married working women, job satisfaction, job performance, health issues, stress, familial and social demands of women. In this paper an endeavor has been made to address an over view of various aspects of Work live balance through the review of existing studies.

Design/Approach: Whilst, it is a Qualitative approach of literature review. So many of the sources are referred from numerous journals, articles, research papers, and doctoral thesis and internet sites.

Findings: To wrap up the results based on observations work life balance is persisting because of various reasons like male dominated society, lack of fatherhood rights in men, no sharing of hometasks stress, varied stressors at work and at home etc. But researches also predicted that work lifebalance can be equalized by opting work welfare policies in organizations like stable flow of communication, flexi working hours, motherly support schemes, personality roles, appropriate perception etc..

Key Words— Married working women, Work life balance, Stress, Polymorphous Responsibilities, Familial calls

I. INTRODUCTION

Women of the first centuries were principally confined to their kitchens and people UN agency were utilized worked in factories, farms or search works. Only a few ladies had the access to pedagogy and that they were forced to be at the mercy of their fathers' or husbands' attitudes towards ladies and work. Education has not sceptered them however given them a chance to form a sturdy career. However this has become a troublesome challenge for ladies as they need to perform duties in home still as in workplace. Equalization between their personal and skilled commitments plays a significant role in their life in maintaining a decent and positive physiological, psychological, social and emotional health. Because the range of twin career couples is step by step increasing and also the support of the joint family goes away. Men and ladies workers area unit troubled arduous to manage their skilled and private lives. Ladies professionals realize it troublesome to fulfil demands of the family and society and at a similar time do justice to the stress of their profession at geographic point. This issue becomes even additional pertinent in an exceedingly country like Republic of India wherever most of the familial roles area unit gendered.

Work–life balance may be a thought as well as correct prioritizing between work-career and ambition and lifestyle-Health, leisure, family and non-secular development. Work- life balance isn't regarding the number ofyour time you pay operating vs. not- working. It's additional regarding however you pay some time operating and reposeful, recognizing that what you are doing in one fuel your energy for the opposite. It's central to debates regarding quality of operating lifeand its regard to broader quality of life. It's regarding creating decisions and exerting some management over our lives. Work-life balance is significantly conjointly the highest priority for ladies and also the key to attracting and retentive feminine talent during this more and more difficult setting. because the range of girls within the men continues to grow and so as to draw in and retain feminine workers, employers got to higher take into account the wants of girls staff, significantly in terms of patterns of operating and time without work for (family-related) emergencies. In straightforward words Work-life balance of girls is regarding making and maintaining substantiating and healthy work environments, which can modify workers to possess balance between work and private responsibilities and so strengthen worker loyalty.

II. LITERATURE REVIEW

Akobo, L. A., & Stewart, J. (2020), Current study aimed to unfold WLB by applying several theoretical lenses among women (working) of African origin living in UK. It also tried to fill the gap of current sexual orientation in the work environment that influences work fulfillment and professional needs of them. Theories of "work-family, gender inequality and Theories X and Y" were implied. Using a purposive sampling method, "total 15 semi-structured interviews were conducted with women from Nigeria and Ghana residing in the UK". The interview time varied from 1-1.5 hours, and were held at places convenient to the respondent (home, public places, on phone). It included many facets like face-to-face communication, "phone calls and referrals". Also, data was covered by recordings done by the authors at group discussions that were based on WLB. All interviews were documented (11 were recorded, rest 4 provided written notes). Results displayed 3kindsof WFC: time, behavior and strain-based.

Time-centered were due to shortage of time at both places. Behavior based occurred when an unusual code of conduct was exhibited by the respondent like hostile interaction resulting from "unfair division of household, childcare or wage" labor; it was considered inapt and unfit at the workplace. Strain related clashes happened when "anxiety and fatigue" developed that were provoked due to accumulation and intensification of work–family duties, conceivably distressing an individual's well- being. Findings also revealed the ways adopted by these women in making "work–family choices using networks and services". It was discovered that a lot of participants gave an upper hand to family responsibilities which meant that they were willing to quit job, if necessity so arose. But it also indicated that this was an unjust behavior of their societal norms towards them and that they were overburdened with domestic chores and were held responsible if any wrong doing occurred in the home premises.

DeSimone, K. (2020), the motivation behind this investigation was to expand a comprehension of understanding of women's perceptions regarding obstacles that hinder their road to success in company called S&P 500, keeping family in the husband excluding gender isolation. Data collection was done by semi-structured phone interviews. The company S&P 500 was selected for the present study by the researcher because of its much talked about diversity initiatives. On request of the researcher, 13 participants were chosen and all were pinpointed by the management as high-

potential candidates. They all were thoroughly interviewed, about 1 hour each. All participants were elite professionals, and were subjected to massive job-related travels and meetings. "Interpretive phenomenological analysis" was utilized to obtain the outcomes of the study. Deductions reported that those households where both partners were working and holding high posts of work and responsibility there it really becomes troublesome to fit in both roles simultaneously. So in such cases, one career has to succumb so that the other one may survive. Participants replied it was mostly women who agreed to make this sacrifice. The vexation and exasperation of respondents was very clearly felt on surrendering career of either person "when both partners are highly motivated and have top-talent potential". Women also felt cynical and deceived when they and their "male counterparts are at the same level, who often have a spouse at home to cover family obligations".

Chandel and Shekhawat 2019, discovered in their analysis study that the ever-increasing duties that a ladies should they don't seem tobe solely involved with usual tasks of a married woman however more of an operating ladies too and with all this burden of serious work on their head one major issue that they still suffer and that has been identical of these years is that the fastened perspective of the society that demands that a ladies has to watch out of the family wants altogether things despite of the actual fact that she even have knowledgeable work life. A married operating ladies in our country goes through a great deal of stress owing to the ne'er ending struggle of equalization work life and privatelife. Therefore, among this paper i will be able to analyses however this twin responsibility on married operating ladies adversely impacts them and creates most stress that it tends to effect the body image, mental state further as quality of lifetime of these ladies.

Shirsagar. K 2018, her analysis study was centered on ladies worker Work-Life Balance of service sector particularly lecturers, Banks and Health care sector of Aurangabad Region. A shot was done to check the existence of work-life balance downside among the operating ladies within that space. It absolutely was tried to look at however the factors touching work-life balance influence quality of lifetime of married operating ladies. Supplementary she taken in her analysis study that eighty three.33% of the ladies staff were found terribly spoken language that the Work Life provided to them was worst. It's discovered that they'll be underneath substantial stress thanks to lack of work–life balance. Thanks to longer stretched operating hours their productivity might suffer together with their relationships, health and semi-permanent employability.

Deshmukh. K 2018, in their study created a shot to search out robust challenges sweet- faced by operating ladies in maintaining a balance between personal life and vocation. The varied factors touching the work-life balance of married operating ladies are examined during this study. The tool used forthe study is that the manual on work–life balance of the economic Society. Information were subjected to descriptive statistics and it absolutely was found that the issues sweet- faced by the operating ladies of Pune Maharashtra geographic region state in terms of work-life balance are quite high. The results additionally indicate that the work-life balance of people have an effect on their quality of life.

Rathee and Bhuntel 2018, their study focuses on 3 main insights. Initially on the factors influencing the work life balance of staff in academic organizations. Secondly, it tries to search out whether or not there's a distinction between the influence of those factors on males and females. Thirdly, it studies whether or not occupation (Government and Private) of the staff has any impact on influence of various factors on work life balance. Also, their study suggests that there are a unit scores of hindrances in work life balance that all area unit associated with the factors analyzed during this gift study. for instance, tug of war between time and work, stress, traveling downside, people's perspective towards their jobs, excessive responsibilities reception and geographic point, lack of coordination at geographic point and residential, family's expectations etc. To kind these hindrances of labor life balance there's ought to study work life balance.

Johari et. al 2018, examined the following primary objective of this study is to look at the influence of

autonomy, work and work life balance on job performance among lecturers. A survey was meted out among lecturers publicly colleges within the Northern Region of solid ground Malaysia. Supported the applied mathematics analyses conducted, the findings according that autonomy and work life balance had a major impact on respondents' job performance. Workload, on the opposite hand, had no substantial touching on job performance among college lecturers during this study.

Radhakrishna 2018, conducted a research study at Hyderabad and compared the strain level of married operating ladies in IT sector. He supported in his analysis that several factors have positive and plenty of have negative impact on stress level of ladies. Thanks to that ladies notice it tough to cope up with WLB. Specifically, side like Road Traffic, it offers vast level of stress to operating ladies instead of physiological state or the other variables.

Thevanes and Mangaleswaran 2018, conducted a study so as to fulfil the empirical data gaps. Hence, the target of his study was to check the link between work-life balance and job performance. So as to attain the objectives, primary knowledge were collected from 166 workers of chosen personal banks in Batticaloa region of Sri Lanka and also the structured form was administered to gather the information. Instep with the empirical findings from this study, work-life balance, as a vital part of HRM, it will influence performance.

Alternative conditions being equal, the higher the work-life balance in a very given firm, ends up in improve the duty performance of workers.

Rudra 2017, disclosed in his study the amount of stress to take care of work life balance of the twin career couples, wherever the feminine counterparts are operating within the personal health sector in urban center. Cronbach alpha was used as a responsibility take a look at. Freelance sample t-tests were wont to study the result of gender and family structure on respondents' satisfaction towards WLB. Nowadays, a career isn't a mere want, but rather, a necessity. It's evident that associate understanding, accommodating, and sympathetic approach to the management of twin career stress will improve structure effectiveness by fostering continuing employment and most performance among twin career couples.

Ashtankar 2016, recommended that his study targeted on assessing the impact of work-life balance determined by work-family conflict and family-work conflict on the upbeat of local department workers of Nagpur district. Upbeat was measured by levels of family satisfaction, work satisfaction and psychological distress. This analysis paper is an endeavor to spot the impact of labor life balance on employees upbeat. In their analysis practices they over that additional work-family conflict is experienced by Police dept. workers the less happy they're with their family lives & work life and fewer psychological distress are ascertained. Additional family-work conflict is experienced by the Police dept. workers the less happy they're with their family lives & work life and additionally additional psychological distress are ascertained. Considering the importance of work-life balance within the work, the findings of the study have vital sensible implications to each organization.

Semlali 2016, in her analysis declared that a lot of the married feminine employees ensure that they fulfil role with responsibilities inside their family and at work. However, theperception of their work and family role wasvaried from each other. In fact, quite half married ladies interviewed adhere to cultural stereotype of being ladies World Health Organization will everything reception. During this regard several stressed ladies say that we've the majority classical roles of our family. Current study give 3 main recommendations. Firstly-increase of maternity leave, secondly- work place nurseries and thirdly- telework choices could also be enforced.

Verma .S 2016, through her paper created anendeavor to explore the robust challenges round-faced by operating ladies in maintaining a stability between their personaland business life. The rising responsibilities on the private facade with the technical blessings like advanced mobile phones,notepads, etc. that keeps work life enclosed with personal life additionally creates stress on personal and skilled fronts during this dataage. This affects the person's substantial, emotional and social well-being. the various factors moving the work-life balance of married operating ladies are examine during this study ladies fascinating up work life balance challenge have an effect on women's advancement. The Indian ladies had been homemakers however the ever increasing value of living has created them to travel out and judge on for Careers. Labor union ought to try and improve the conditions for woman's employees in several components as an example maternity leave is definitely provide to ladies. Government ought to place strict rules for these sorts of crimes, additionally conveyance system generally danger for lady and Government ought to place additional review.

Preeti and Yajurvedi 2016, in their analysis study propounded that job life balance is a vital idea. Everybody needs to take care of equilibrium between their work and family life in order that they'll lead a balanced life. This paper studies the impact of Work-Life Balance practices on worker retention and the way they enhance structure performance. The findings show that a Work-Life Balance it's not a quandary to be determined once however a relentless concern to be managed. For organization goals to be achieved through the folks utilized, Work-Life Balance issues should become a vital feature of human resource policy and strategy. We propose organizations got to improve their practices so as to boost structure performance, as well as increased social exchange processes, accumulated value savings, improved productivity and reduced turnover.

Mundada and Tiwari 2015, aims to seek out the extent to that the feminine labor needs to forgo its personal and social life for

fulfilling skilled likewise as family obligations. He conjointly aforesaid that ladies professionalsstruggles to meet demands of the family and at identical time do match to the strain of theirprofession at geographical point. This issue ought to be thought-about in country likeBharat wherever ladies has to be sceptered, thence trying jobs not solely affects feminine employees' ability to harmonize work and family life however conjointly joined with health risks, polygenic disorder and vas diseases, weight gain and depression. In theiranalysis study they realize it cheap to conclude that fashionable organization, particularly banking sector, ought to address the work life balance connected problemsamong their employees specifically ladies and take a holistic approach to style and implement policies to support the employeesto manage their work life balance. Careful designing and private effort square measure the recommendation from those that have found balance in each career and residential life. As per their findings, one respondent summarized, "Plan, place and schedule asexpeditiously as potential... and do not be fearful of exhausting work!" A sentence thatbrings the concept of labor life balance to thepurpose is: "Work to measure. Do not live to figure".

Arathi and Kumar 2015, impart in their studythat their paper aims at analyzing the distinction between level of labor LifeBalance among male and feminine middle level staff and therefore the main reason behind the distinction. And that they terminated in their analysis study that it's essential for girls to balance between their family and work as compared to men. Moreover, the time and efforts ladies ought to pay for his or her family and their work place exploit their physical, psychological, emotional and social elements. Hence, they conjointly support their analysis with providing suggestions that variables like promotions and better financial gain square measure absolutely related with Work Life Balance. Here promotions square measuremotivating issue that provides a way of feat and emotional satisfaction that successively helps within the Work Life Balance of girls staff. It's understood from the thought oflabor Life Balance that fulfilment of social desires and private desires square measure the necessary predictors of WLB. So, if the organizations specialize in Work Life Balance of girls staff by enriching their role effectuality the productivity of the organization likewise because thedevelopment of the workers are going to be ensured.

Das and Panda 2015, says that employment life refers to the link between staff and their operating surroundings. This approach says that folks will perform higher to their best if they're given autonomy in managing their work and life and choices likewise.

So a successful organization ought to specialize in this HRM component thus on get a lot of productive.

Lavanya and Thangawal 2014, created a shotto bring out through their analysis study, the impact of Demographic factors on WLBPs inIT firms. They terminated through their analysis that a Flexi operating approach/ schedule ought to be created a compulsory resolution to the matter of WLB for girls specifically World Health Organization square measure enjoying double roles.

Atheya and Arora 2014, discovered via their paper the impact of stress on the lives of staff, identifies the determinants to employees' work-life balance and conjointly suggests the roles and responsibilities of key parties by providing appropriate ways that to employers for facilitating a more robust WLB choices at the work- place.

Pandey and Jha 2014, aforesaid that teaching is that the key of success of a nation that boosts the economic potential of entire nation resulting in the event of the state. This is often sort of a middleware transformation engine that produces personnel for trade, develop enterpreures and motivates young minds for R&D. This responsibility is on the shoulders of academic staff to know and remodel the energy and information of scholars in economical good} and efficient manner.

Associate degree abundance of analysis studies recommended that the standard of labor life (QWL) is one among the foremost important and economical tools of human resource management. Quality of labor life programs encourage staff, build balance between skilled, personal & social life and ultimately enhances worker job satisfaction.

Ranjan & Prasad 2013, disclosed in their study concerning the railroad wherever railway driver is exposed to a difficult psychosocial work surroundings, which incorporates solitary work, restricted opportunities for social contact and an important responsibility for in operation the train (in terms of each safety and adhering to the timetable). The railway driver's job, i.e. to work the train, is basically ruled by timetables and technical conditions (e.g. sort of train, track area), that restricts the driver' s ability to make a decision for himself however the work is to be done. Railway drivers struggle to meet work and family responsibilities. This struggle is because of long hours, irregular and inflexible work schedules, and significant workloads. Thus, work–family conflict are often a standard work agent for railway drivers. This paper deals with the standard of labor lifetime of Indian railways' drivers and also the factors that cause Associate in nursing imbalance, inflicting high chance of accident. This paper discusses the operating conditions and quality of life to the Indian railway drivers. This paper conjointly in short reviews ideas relevant to shaping work-life balance. This review of literature deals with the Work-Life balance of Associate in Nursing Indian railways' drivers to see the operating conditions Associate in nursing level of their work life balance that has terribly high importance on their total well-being and thus their productivity and whole growth of an Indian railway.

Singh Satinder 2013, through his literature paper identifies impact of WLB on numerous quality life conditions i.e. Job Satisfaction, Work Stress, Career Growth, Turnover, absence, Appreciation and competitive surroundings in context with Work-life Balance and its practices/policies. During this paper, Associate in nursing endeavor has been created to supply a summary of assorted aspects of Work-Life Balance through the review of existing literature.

Raya and Delina 2013, disclosed in their study that non-public factors produce stress on personal and skilled fronts during this data age. This affects the person's physical, emotional and social well- being. Thus, achieving work life balance could be a necessity for operating girls to possess an honest quality of life. Through his analysis paper he created an endeavor to explore the powerful challenges featured by operating girls in maintaining a balance between their personal and business life. The varied factors poignant the work-life balance of married operating girls are examined by him during this study.

Santhi and Sundar 2012, their study explores the aspects prefer to live the amount of satisfaction as perceived by the women- respondent staff on the numerous determinants of labor life balance, to spot thefore most factors that influence the work life balance among numerous classes of girls staff in I.T. business and to live the general work life balance of girls staff no matter cadres. The varied life Programmes enforced by I.T. corporations in urban center reveal that job life Programmes enforced satisfy completely different classes of staff otherwise. In different words the set of things facilitating work life balance is completely different for various teams. The general satisfaction of the respondents across the varied work life equalization parameters points to the actual fact that fifty five per centof the staff area unit extremely glad with this work life initiatives. So the management of I.T. corporations surveyed must decide the explanations for moderate satisfaction and discontentedness prevailing among the remainder of the forty five per cent of staff across the cadre and ask for to deal with the problems of discontentedness among the disgruntled staff.

Anitha and Maheshwari 2012, in their study disclosed that job life balance in today's pastpaced world becomes a Herculean task and presents a significant challenge to each employers and staff. Work life balance is currently progressively changing into the put concentration of study by HRM consultants. Whereas labor market participation has enhanced for girls of all ages, girls still shoulder the most responsibility for organizing and enterprise unpaid caring work. This paper 1st tries to clarify that means and underlying thought of labor life balance and also the later appearance at the varied factors of the work life balance construct. And that they over that WLB could be an issue that has the potential to have an effect on necessary geographic point problems like ratio, stress, job satisfaction, and productivity. The pressures of the work or personal life will cause stress. It's been found that such scenario affects person's health each physiologically and psychologically. Staff area unit the pillars of the organization. Thusorganization ought to provide its attention towards the welfare and wishes of the ladies staff. In order that girls staff will ready to balance their twin role i.e., work moreover as personal life. Therefore, it's necessary forworkers to take care of a healthy balance between work and their personal lives.

Holley and Mohnen 2012, in their study urged that a decent work– life balance ends up in high satisfaction. Our results show numerous perceptions and influences of job conditions on workers, therefore the association between operating hours and work–life balance is extremely necessary for corporations and their human resource policies. Measures that have an effect on jobs absolutely might additionally have an effect on life satisfaction negatively and lead to harmful policies. Results area unit significantly attention- grabbing with relation to versatile operating conditions.

Devi. Chitra 2012, complete in her analysis study the 2 spheres of life are getting additional entangled. The boundary between work life and non-work life in making work life imbalances. thence the organization ought to are available front and supply opportunities like versatile work arrangements, child care, dependent care facilities etc., they need to bear in mind of the actual fact that job life imbalance might lead to the negative life satisfaction and impact worker upbeat.

Edarlin 2012, discovered in her study that girls entrepreneurs has positive also as negative issue effects of labor on family and private desires. Results showed that the positive issue effects of labor on family desires and private desires of the ladies entrepreneurs has smart name within the community whereas negative spillover has to try to with health problems/physical exhaustion/stress thanks to long work hours and employment. High 3 ways opted by girls entrepreneurs partaking in activities to manage stress, locating business at an area close to home and coming up with work and family chores earlier than time.

Roomi and Rehman 2012, complete within their analysis study that augmented participation of ladies in the labor creates challenges for them to balance work and family obligations. the case becomes additional difficult in paternal societies like Islamic Republic of Pakistan thanks to women's unimaginative domestic roles, non- secular prescriptions also as cultural norms and values. This study aims to explore totally different influencing factors on women's work and family roles within the distinctive Pakistani socio- economic and cultural setting. They complete that lack of comfortable time, gender bias, social and cultural norms also as family responsibilities area unit the foremost important challenges girls face to attain balance in a very paternal Muslim society. Strategic coming up with, organizing and relegating area unit the foremost effective ways girls use to deal with competitor roles of labor and family.

Mathew and Panchanantham 2011, careful in their analysis study overload dependent care problems, quality of health, time management and lack of correct social support area unit major factors of unbalanced WLB among girl's entrepreneurs. Further, in their study they urged to predict and validate an acceptable tool for overcoming this downside.

Reddy Krishna et al. 2010, discovered within their study Family- work conflict (FWC) and work-family conflict (WFC) area unit additional possible to exert negative influences in the family domain, leading to lower life satisfaction and bigger internal conflict at intervals the family. Studies have known many variables that influence the amount of WFC and FWC. Variables like the dimensions of family, the age of youngsters, the work hours and also the level of social support impact the expertise of WFC and FWC. They created a trial to check numerous factors that could lead on to WFC and FWC among married girls workers. More they feel the requirement of lacking on the part of organization and organization ought to formulate tips for the management of WFCs at structure level because it is said to job satisfaction and performance of the staff.

Whitehead and Kotze 2003, propounded in their analysis study regarding the woman's ability to balance multiple life-roles is directly associated with her physical and mental well-being, and her career performance and success. This study aims toinfer a theoretical framework for the in-depth understanding of the development of life-balance within the lives of twenty four South African skilled girls. It had been complete that life-balance may be a life-process with arotary nature, and a great tool for achieving personal growth. Life-balance is so not "one, single final experience", however a series of individual experiences evolution over time, that might be higher delineated as "life- balance moments".

III. FACTORS CAUSING WORK LIFE IMBALANCE

From the literature study, it has been founded out that the following factors are responsible for the work life imbalance. They are-

a. Polymorphous Responsibilities Conflict

Each person of existent world has a numerous responsibility and as per these responsibilities they have a number of obligations to execute in their professional and social life. These roles have lot of influences on mortals under different circumstances and conditions. Thus, the conflict which arises due to these heterogeneous roles of employee is known as Polymorphous Responsibilities Conflict. And where there is presence of heterogeneous responsibilities conflict, it results on the imbalance between the work and personal life.

b. Organizational Environment

The place where an employee work is organizational environment. It includes infrastructure, work policies, Co-workers support, superiors and subordinates. All these variables are allied to each other, a change in one variable will have impact on other. Ultimately it will create disturbance on work life imbalance.

c. Mental Issues

Stress can be defined as that state of an individual where he is bound to feel emotional or physical tension. It may result from anything (job pressure, growth in career, health, financial condition) to nothing (thinking about future) but is liable to make one-self frustrated, angry, or nervous. Stress is a body's reaction to a challenge or demand. In short bursts, stress can be positive, such as when it helps a person to avoid danger or meet a deadline. "Stress is the body's reaction to any change that requires an adjustment or response. The body reacts to these changes with physical, mental, and emotional responses". This monster is otherwise a part of normal living; it can occur from environment, a person's body, and his/her thoughts.

d. Familial Calls

The desire/need of family folks shall be the top priority. Whenever they call upon something they shall be contended on time. Secondly the mortal must ensure that work demands do not over shadow familial demands. If it happens so then there are more possibilities of Conflict. As a result, it would lead to work life imbalance of employees.

e. Work Stipulations

Work stipulations are those circumstances that arouse at work station. One of the predictable muddles every employee suffers. Similar to Family demands the work stipulations must be met on time and at best conditions. These demands must be the urgent domain of workman. If they are not accomplished as prescribed then it can create work life imbalances in employees.

f. Problem of Social Support system

It means the problem faced by women in organization as well as in their homes. In short family support to work domain issues and supervisor support to family domain issues. If these are not in synchronization than it will create work life imbalance.

g. Stress, Age and Health

If there is mental and physical exertion then it will lead to stress and imbalance work life balance. Also age is primary factor which reflects efficiency in work. As age decay the work efficiency also diminishes at pacing rate. This all leads to imbalance in work life.

IV. CONCLUSION

Although the concept of work life balance is not a new notion and contrasting research studies have been executed. Still this area is so monumental to research that it attracts the interest of HR practitioners and researchers. This mainly could be attributed to the ever- rising demand of family and work. There is no perfect practice or strategy to over-rule work life balance. But as per studies work life

balance will be an issue which will demand more time, toil, and new practices to balance the wheels of work as well as life. By enlarge research studies are more enough to support that there are many factors up-shot with work life balance of married working women in the atavistic time as well as in new epoch also. Undoubtedly the size of factors affecting the disparity have reduced but it still outlasts. The position of married working women can be improved and results from the studies depict that it can be done only if the married working women is provided an experience of openness, being allowing her to be extrovert, independent, reflective personality and contemplative.

a. Practical Implications

Management practioners need to take steps to implement vigorously holistic policies in organizations. Respondent's perception towards various determinants of WLB hints that provision for promoting WLB among working professional married women is must in employee wellness programme fabricated by organizations. Flexible work culture must be promoted as righteous tool for successful work life Balance strategy

On the other hand, familial calls could be adjusted timely by the other masses of the family, hence making it little than a complex for the married workingwomen to maintain parity.

b. Retrieved Information

Work life balance has been evolved in the life of women's as a custom which as a resultant is onerous. It ultimately oppress the female counterparts leading to destructions. Maintaining an equilibrium in these tough circumstances is equivalent to null and void situation for the ladies. An attempt has been made in order to elucidate the summary of the above mentioned literature review in a tabular form,where in the researcher's contributions have also been proffered.

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Design and Verification of Wishbone Compliant Protocol

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Abstract— Synchronous serial interfaces give practical onboard correspondence between the processor, computerized to simple and simple to advanced converters, memory, and other building hinders present on the chip. Various Integrated Circuit (IC) makers create and deliver parts that are perfect with serial interfaces. The basic serial interfaces incorporate Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I2C), Universal Asynchronous Receiver Transmitter (UART), and Universal Serial Bus (USB). SPI is generally utilized and worthwhile over other serial interfaces because of its highlights of effortlessness, minimal effort, synchronous clock, and nonintruding on rapid information exchange rate. An open source equipment PC transport Wishbone is chosen as the host controller empowering parallel information trade for quicker correspondence. Both the equipment transports utilize a master slave setup which makes the transport interfacing less demanding.

Key Words— SPI (serial peripheral interface); Wishbone; Verilog HDL

I. INTRODUCTION

SPI is the highly used serial communication protocols that is mainly used for the intra-chip high speed data transfers. This is applied to interface among a microcontroller and other peripherals like ADCs, DACs, and EEPROMs. We are using different data rate communication protocols in the field of serial data communication. SPI is considered as small communication protocol. Each and every protocols have their specific purpose and usage. USB, Ethernet and Serial AT Attachment, are meant for "inter-system communications" and data transmit in the whole system, while in serial peripheral interface the communication happens between the integrated circuits for little or middle data transfer rate with peripheral devices [2].

II. SERIAL PERIPHERAL INTERFACE

Serial to Peripheral Interface (SPI) is a hardware communications protocol developed by Motorola for the transmission of data between the microcontroller and the peripherals. This protocol was later adapted by others in the industry. The Serial Peripheral Interface or SPI-bus is a simple four-wire serial communications interface used by many microprocessor/microcontroller peripheral chips that enables the controllers and peripheral devices to exchange the data with each other. Even though it is initially developed for the communication between host processor and peripherals, a connection of two processors using SPI is possible. Both single-master and multi-master protocols are possible in SPI. The SPI Bus is mainly used only on the PCB. The SPI Bus was designed to transfer data between various IC chips, at very high speeds. Most literature review indicates that the interface can only be used for eight or sixteen bits data transfers, but many Motorola microcontrollers allow transfers of any range of blocks between two and sixteen bits at a time. Because of the serial nature of the interface, data transfers of more than sixteen bits at a time can be made easily through control signals. SPI is a protocol that has four significant signal lines (as shown in Fig. 1).

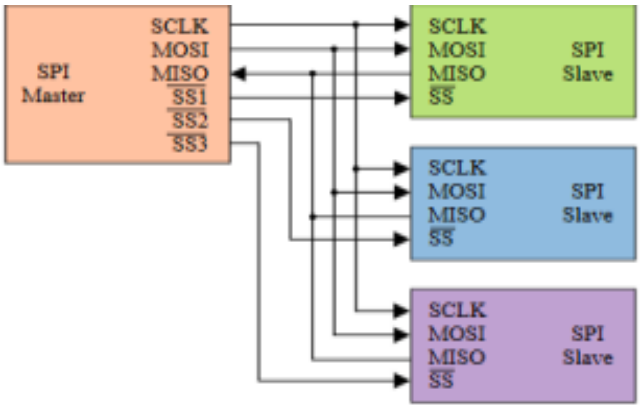


Fig: SPI block diagram

- MOSI - Output data from the master to the inputs of the slaves.
- MISO - Output data from a slave to the input of the master.
- SCLK - Clock driven by the master to slaves, used to synchronize the data bits.
- SS - Select signal driven by the master to individual slaves, used to select the target slave. If there are multiple slaves, then master makes the particular SS line low to which the data has to be transmitted. SPI Master drives the SCLK line and controls the stream of information bits. The Slave Select (SS) line must be low to choose a slave. SPI supports single master communication protocol. This implies one focal master starts every one of the correspondences with the slaves. At the point when the SPI master wishes to send information to a slave as well as

demand data from it, it chooses slave by pulling the relating SS line low and it actuates the time motion at a clock recurrence usable by the master and the slave. Consequently, when there is a need to implement a communication between an integrated circuit such as a microcontroller and a set of peripheral devices, SPI turns into the best decision to move with. SPI has turned into the de facto standard for current computerized hardware frameworks and it will most likely keep on competing later on.

III. WISHBONE INTERFACE

The communication of the SPI master and slave devices with the processor on a chip through the Wishbone bus is shown in Fig. 2.

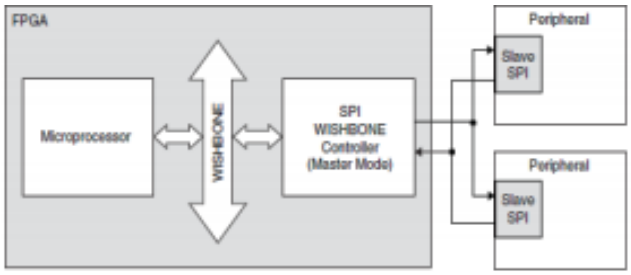


Fig: Processor-SPI Interaction

This SPI WISHBONE controller provides an interface between a microprocessor with a WISHBONE bus and a SPI device. The controller can either act as the SPI Master or SPI Slave device. The selection of the Master or Slave mode is done using parameters in the Verilog HDL code. The design uses a single module [8].

A. SPI DATA TRANSFER MODES: A full-duplex communication is established between the microcontroller or microprocessor and the peripheral devices. The data word or character is simultaneously shifted out from the master to slave and shifted in from the slave to master serially one bit a clock cycle. The data sampling and shifting are synchronized by the SCLK and only after a slave peripheral device is selected by the microcontroller or microprocessor. Two bits in the SPI control register control the clock phase and polarity. There are four modes of operation. As depicted in the table.3 it defines the modes of operation of the data transfer. The phase and polarity should be identical to both the master and slave throughout the transfer. As SPI is synchronous to the serial clock, the data shift occurs on one edge of the serial clock(either positive or negative) and the data capture is on the other edge. Ideally, there are only two data transfer formats based on the clock phase.

TABLE II. APPLICATIONS OF SPI

Device	Application
Sensors	Temperature, Pressure, Touch Screens, controllers, ADCs
Control Devices	CODECs, DACs, Digital Potentiometers
Communications	Ethernet, USB, CAN, USART, IEEE 802.11, IEEE 802.15.4
Memory	Flash, EEPROM, SD card
Clocks	Real Time Clocks

TABLE III. MODES OF OPERATION

Mode	Polarity (CPOL)	Phase (CPHA)	Data Shift	Data Sample
0	0	0	Falling (Negedge)	Rising (Posedge)
1	0	1	Rising (Posedge)	Falling (Negedge)
2	1	0	Rising (Posedge)	Falling (Negedge)
3	1	1	Falling (Negedge)	Rising (Posedge)

IV. METHODOLOGY

The design methodology of the SPI follows the below flow

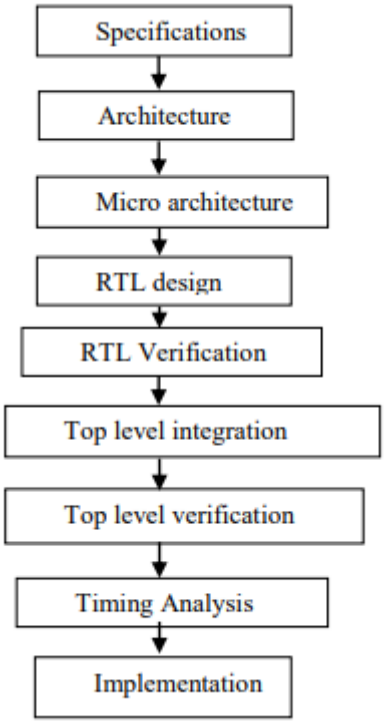
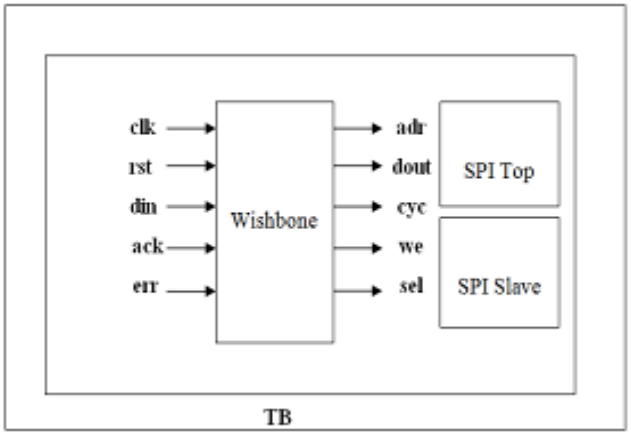


Fig: Flow chart of the VLSI design

V. ARCHITECTURE

The figure below shows the architecture of the complete SPI to be designed. There are three blocks for which RTL design for each block is written and verified. Then the top level integration is followed by top level verification. After which the timing analysis of the integrated architecture is performed.



The Micro-Architecture is shown below is classified into three bocks

- Wishbone
- SPI Master
- Read FIFO
- Write FIFO
- Control Circuits

- FIFO Empty: At the point when the Read Address Register rises to the Write Address Register, the FIFO is named as empty.

- FIFO Full: When the read address LSBs equal the write address LSBs and the extra MSBs are different, the FIFO is full. The control circuit block consists of the three main control registers i.e. SPI Control Register (SPCR), SPI Status and Control Register (SPSCR), SPI Data Register (SPDR).

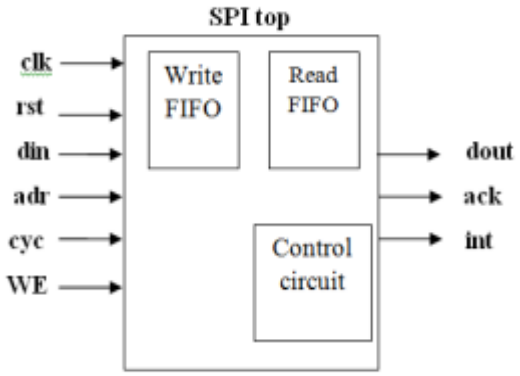


Fig: SPI top module

SPI Slave contains Control Circuits, the below figure shows the SPI slave block. It contains the control circuit block in which the control registers are there.

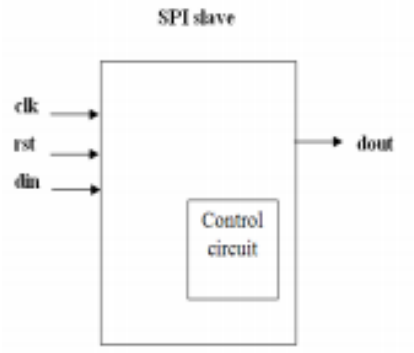


Fig: SPI Slave Mode

VI. CONCLUSION

Our work focuses on the performance analysis of SPI along with the RTL Design work. Design part involves around the specifications and codes written in the Verilog. Serial peripheral interface RTL divided into three blocks i.e. Master, Slave and SPI top module. RTL code written for the complete architecture using the wishbone interface model which open source, work done using XILINX VIVADO Design suite tool which gives simulation and synthesis validation of specification. The complete RTL has been designed for the complete architecture and design summary reports has to recorded.

VII. FUTURE SCOPE

The development of verification environment can be extended to the verification other Wishbone-compliant peripherals that support additional communication protocols.

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Impact on Project Manager Role and Team Structure due to Changing Software Engineering Methodologies

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Abstract— Project management methods have been developed from industry practices and international standards to ensure a higher rate of success for information technology projects. These methods have been widely used in various IT organizations. In IT industry, the entire work is often "projectized" and team structure is also designed to support execution of projects. Research has shown that the successful execution of projects is depended on the project management practices rather than technical issues. This paper deals with the impact of Agile and DevOps on project manager role and team structure. Agile processes have essential applications in the areas of software project management. Specifically, the objective of agile processes is to fulfill the customer requirements at timely manner and also with lower defect rate. It is also evident from the previous researches that, Agile and DevOps methodologies have impact on shared responsibility, automation and feedback which organizes team structure. In addition to these, this paper also provides insight into the skill set needed to adapt Agile and DevOps methodologies.

Key Words— Agile, DevOps, Project manager Role, Team Structure

I. INTRODUCTION

Nowadays, business environment is more dynamic and changes frequently in terms of software & product development. Agile methodologies are implemented and used widely around the world (Rasnacis and Berzisa, 2017). More and more software teams are focusing towards the agile development and this is to increase the efficiency of their projects and to meet the customers' competitive requirements. Agile methodology was developed to deal with the issue, where the traditional model fails in project development and also it provides various opportunities to the projects throughout the development lifecycle. Agile development methodology is an iterative methodology in which customer fulfillment is at top priority as the customer has direct contribution in assessing the software (Boehm and Turner, 2003). Agile and DevOps methodologies add values to the project and also help to deliver the projects accurately and in right time. Agile and DevOps provides excellent feedback which will help to deliver the software system most successfully. Agile and DevOps enables collaboration in workplace and allows team to make decisions together effectively and quickly. DevOps brings efficiency and agilty in the software development process.

II. 2. LITERATURE REVIEW

2.1 Project Management Roles and Team structure

IT Project team roles

The Project Management committee/board is made up of the positions of Project Executive, Senior Manager representing the interests of the Company and end Users /Suppliers/Developers, respectively. The Executive is responsible for the project as a whole and must ensure the project's return on investment while balancing the business, customer and supplier requirements. The customer representatives acting as proxy representative for the end users and will track the project in order to ensure that the output follows, in terms of quality, the targets outlined in the business case.

Project Manager

On behalf of the Management, the Project Manager runs the project on daily basis. The Project Manager is responsible for ensuring that the project deliverables meet the required and predetermined quality standards within the cost and time constraints.

Team Manager

This role is only applicable in larger projects, where team members are divided into sub-teams of specialists, each of which is headed by a team manager. The team manager, in turn, takes the direction of the Project Manager.

Team

Team members are responsible for execution of the project and consists of specialist like Architects, developers and testers.

Project Assurance/Quality Services

Assurance provides independent monitoring of all aspects of the project and covers the interests of all concerned. Project Assurance is responsible for identifying, reporting and escalating any potential issues arise as soon as (or preferably before) they arise.

2.2 Agile Methodology - An Overview

Agile is a methodology in which an association engages its people to work where, when and how they choose with greatest adaptability and least requirements to optimise their execution and convey "best in class" delivery mechanism and customer administration. It utilizes communication and information technology to empower individuals to work in ways, which best suit, their requirements without the traditional limitations of where and when errands must be performed. It depends on the

idea that work is an action people do, as opposed to a spot people go. With the technology accessible to current business, there are various tools to enable people to work in new and distinctive ways, to meet customer needs, diminish costs, increment profitability and improve manageability. Agile is a transformational tool to enable associations to work more astute by dispensing with all barriers to working proficiently (The Agile Organization, 2013).

The "Agile Manifesto" provides a good overview of the intent of Agile Methods ("Manifesto for Agile Software Development," 2001). The following values express the tenor of the principles employed:

i.) individuals and interactions over process and tools

ii.) working code over comprehensive documentation

iii.) customer collaboration over contract negotiation

iv.) responding to change over following a plan

Highsmith ((2004has proposed five periods of the agile project management approach: Envision (characterize vision, project degree, and project association), Speculate (create display characterized by the item qualities and time requirements, and cycle plan for vision usage), Explore (convey tried parts in brief time and constantly scan for an approach to lessen project hazard and vulnerability), Adapt (check expectations, current circumstance, and team conduct to adjust if vital) and (close project, make exercises learned, and celebrate).

Agile development methodology is an umbrella term that describes several agile methods such as Scrum, XP, ASD, Crystal, FDD, and DSDM.

DIFFERENT AGILE METHODOLOGIES

Agile is a framework and there are number of specific methods within the agile movement The different flavours of agile are:

Extreme Programming (XP): It is also known as XP, extreme programming is a type of software development intended to improve quality and responsiveness to evolving customer requirements. The key points of XP include feedback, assuming simplicity and embracing change.

Feature-driven development (FDD): This iterative and incremental software development process blends industry best practices into one approach. There are five basic activities in FDD: develop overall model, build feature list, plan by feature, design and build by feature.

Adaptive system development (ASD): Adaptive system development defines the idea in which projects should always be in a state of continuous adaptive state. ASD has a cycle of three repeating series: speculate, collaborate and learn.

Dynamic Systems Development Method (DSDM):This agile project delivery framework is used for developing software and non-IT solutions. It addresses the common failures of IT projects like going over budget, missing deadlines, and lack of user involvement [7]. The eight principles of DSDM are: focus on the business need, deliver on time, collaborate, never compromise quality, build incrementally from firm foundations, develop iteratively, communicate continuously and clearly and demonstrate control.

Crystal Clear: Crystal clear is part of the crystal family of methodologies. It can be used with teams of 6-8 developers and it focuses on the people and not on processes or artefacts. Crystal clear requires the following: frequent delivery of usable code to users, reflective improvement and osmotic communication preferably by being co-located.

SCRUM: Scrum is one of the most popular ways to implement agile. It is an iterative software model that follows a set of roles, responsibilities, and meetings that never change. Sprints usually lasting one to two weeks, allow the team to deliver software on a regular basis. Scrum is a repetitive and progressive agile software development framework for managing software projects or application development. Its focus is on "a versatile, holistic product development strategy where a development team works as a unit to achieve a standard goal" as against a "traditional, sequential approach"[5].

Scrum Roles

These are the essential roles for scrum success. A scrum team has a slightly different composition than a traditional software development project, with three specific roles: product owner, scrum master and the development team [5]. And because scrum teams are cross-functional, "the development team" includes testers, designers, and engineers in addition to developers.

PRODUCT OWNER

- The product owner represents the stakeholders and is the voice of the customer.
- Accountable for ensuring value to the business.
- Writes (or the team) customer-centric items (user stories), prioritizes them, and adds them to the product backlog.
- Scrum teams should have one, may also be a member of the development team.
- Not be combined with that of the scrum master.

DEVELOPMENT TEAM

- Responsible for delivering potentially shippable product increments at the end of each sprint.
- Made up of 3–9 people with cross-functional skills who do the actual work (analyze, design, develop, test, technical communication, document, etc.).
- Self-organizing, even though they may interface with project management organizations (PMOs).

Lehman et al (2011) stated that, Agile software processes is an iterative and incremental based development, where necessities are alterable as indicated by customer needs. It helps in versatile arranging, iterative advancement and time boxing. It is a system that advances anticipated associations all through the development cycle. The software development activities like planning, analysis, structure, coding, testing and support which should be performed by the interest of the customer. The development activities rely upon the different applications to pick the particular model (Ahmed et al, 2010).

2.3 DevOps Methodology - An Overview

The Operations endeavor is to ensure nonstop client service by giving a steady and dependable working condition. On the other, the Development objective is to keep enhancing and releasing new enhancements in the production or in existing services by agile way of working. These targets present a test: how to deploy latest changes rapidly and every now and again, without undermining the unwavering quality and steadiness of the working condition. The DevOps approach is to unite Development and Operations to address this challenge. The approach gained resonance with the IT people team and was expanded after some time to include the effectiveness of the delivery chain, just as the quality of the output in terms of enhancements or services.

DevOps presents an answer for the challenge that associations face in discharging enhancements or service updates into complex working conditions without causing administration interruption. This is not a new challenge. In any case, the need to discover answers for the challenge has strengthened as agile advancement practices and complex versatile foundation setups have gone to the fore throughout the most recent decade (Ahmed and Capretz, 2011).

DevOps was supposed to be solution to improve cooperation between Development and Operations teams to meet this challenge (Kim et all, 2016). While the standard DevOps execution is conducive in conditions where agile software project management procedures are utilized (Highsmith, 2010), it has been demonstrated that DevOps practices can likewise be effectively implemented in controlled ventures (Fitzgerald et al, 2013). Smeds et al, 2015 in the paper has summarized the challenges the organizations face while implementing DevOps.

DevOps helps in designing an automated framework through which the information and data is passed by the system and overall efficiency is improved.

2.4 Need of Agile & DevOps

The software industry is moving rapidly towards agile methodology to ensure the quality, efficiency, and scalability of the produced software products as it offers alternatives to the traditional techniques of project management. The agile strategy also aims to tackle the problem of unpredictability in industry. Scrum is the agile framework most widely used for projects that have frequent change of requirements. Agile as methodology for has been around for last 2 decades while concept of DevOps is recently gaining momentum. DevOps has been classified as “on the rise” with the respect to the Gartner Hype cycle for Application development in 2013.

Project Management (PM) methodology much remain in tune and updated to cater to requirement for developing software products which became progressively complex and with the demand to launch them in short time. From the traditional technique’s progression has been to towards Agile methodology (2001), after which, in 2009, another major step was recorded by presenting the idea of DevOps (Development Operations). Because of the advantages that DevOps could convey to the ventures as far as proficiency and agility in software project management (Menzel and Macaulay, (2015). DevOps is placed on the top of the 2015 Gartner's Hype Cycle for application services. Nonetheless, toward the finish of 2016, DevOps is yet thought as an expansion of Agile approach, rising up to the need to approve and quickly delivering software enhancements/releases.

2.5 Impact on the Project Manager Role and Team structure

Autonomous agile teams offer potential advantages over traditional software teams. Nonetheless, team execution is mind boggling, and an autonomous agile team's execution depends not just in the team's ability in overseeing and executing its work and more dependent on the team relationship setting. Further, autonomy affects team adequacy when assignment relationship is high and a negative impact when assignment relationship is low. Albeit most examinations report constructive outcomes from autonomous teams, some present a progressively mixed assessment; they can be hard to execute and there is a chance of failure when utilized in wrong circumstances or without adequate authority and backing. The genuine execution of an autonomous agile team depends not just on the capability of the team itself in overseeing and executing its work yet additionally on the hierarchical setting given by management (Hoda and Noble, 2017).

Autonomous teams are not made basically by urging popularity-based beliefs, by tearing down hierarchical chains of command, or by founding one-individual one-vote basic leadership processes. Further, teams regularly don't have the sufficient resources and experience to manage daily issues while maintaining a strategic distance from unnecessary worry for the people. Managers cannot mentor teams for independence. Standards are the casual tenets that control the team and direct team individuals' conduct (Forsyth, 2018). If standards are left to defined by individuals, they will frequently not bolster strategic thinking that is fundamental for autonomous teams.

III. RESEARCH APPROACH

There is a need to establish and determine the specific research philosophy that the research scholar intends to pursue. This is very important in research and it has been

emphasized by (Alvesson & Sköldberg, 2017). They have also clearly stated that there is a need to choose one best representative research philosophy for the research which is very significant.

Rationale for the study:

(Walliman, 2005) has stated that research conducted has to be purposive, to find out a particular aspect, which is clearly stated and data collection and analysis is done systematically. This study would evaluate and investigate in to the dimensions of Agile, DevOps project management practices in Indian IT companies. It is also found that as research studies have not been done on these dimensions, there is a rationale to do this study which would provide new thinking, approaches, solutions and strategies for Indian IT companies and project management procedures.

Rationale of the topic and academic justification:

(Brady, 2015) has given the various methods which must be used for rational choice and selection of topic. Delphi technique was used extensively with professionals, academicians and research scholars of repute.

The past research works which have been done was analysed using the digital libraries of various universities all over the world. Brainstorming sessions were conducted with other research scholars and guide to gain more insights and perspectives.

The global market size for business software and services was estimated at USD 322.91 billion in 2018 and is projected to grow from 2019 to 2025 at a CAGR of 10.7 per cent. The Indian IT industry has been major contributor to growth of the nation with $ 84 billion USD worth of export and employment to 10 million people. In the contemporary world economy India is the second-largest exporter of IT. Exports dominate the Indian IT industry and constitute about 77% of the industry's total revenue. According to NASSCOM (“India IT-BPM Overview | NASSCOM,”), the sector aggregated revenues of US$ 115 billion (Non BPM part) in 2016, with export revenue standing at US$ 84 billion. The IT sector grew at 10.5%, ER&D and product development grew at 12.5% over the previous year

The Software industry in India is well established and has contributed significantly to growth of the economy and employment opportunities in India. We have analyzed that IT/Software projects are vital for any industry and project management is vital to the successful execution of the project. In IT industry the project manager role and team skills were established based on the Waterfall software development approach. The established IT project management practice and the team structure have been established over decades and are aligned with waterfall development methodology. Recent emergence of Agile and DevOps practices have challenged the existing Project management practices, roles and team skills. The changes due to adoption of Agile and DevOps practices on the project manager role and team structure need to be studied. There is gap in terms of studying the impact of Agile & DevOps for Indian companies in terms of project manager role and team skills.

Problem statement:

The study is an investigation in to the agile DevOps and its impact on project manager role and team structure in Indian IT companies. Senior management and collaboration with development team and operations team, scrum master role in projects which has not been investigated.

The role of scrum master and contributions on agile DevOps and its impact on project management practices and team structure has not been analysed or evaluated before. So this research is an attempt to provide solutions to these problems which are prevalent.

3.1 Data Collection and Sampling

Sample choice and decisions:

(Becker, 2008) has differentiated the two concepts population and sample. Population would mean the total number of living persons in the region and sample would be a representation of the total population. As it is impossible to collect information from the entire population due to time and cost factors, usually a sample representation of the total sample is chosen for research study.

(Barnett, 2002) has categorically stated that sampling is the best way to collect data as it is more authentic and representative in nature than population. So he suggests that for researches to be conducted it is more appropriate to collect sample rather than looking at or analysing the population as such.

The importance of sampling and defining the research population is very important. In this research managers would be contacted in Indian IT companies who have been taken as the major group of population to be studied.

In probability sampling we do find simple, systematic, cluster and stratified sampling methods. In non-probability sampling we do find quota, snowball and convenience sampling.

In this study 176 managers would be contacted for collecting data using convenience sampling. The researcher has the ultimate final decision to choose the sample based on the requirements.

3.1.1 Questionnaire Design

The Questionnaire was divided into 2 segments. The first segment was on the demographic profile of the respondents and also to identify if the respondents had worked in Agile & DevOps methodologies. The purpose was to compare the response and evaluate if the changes had made an impact on traditional project manager role and team skills

Table 1 : Proposed Questions mapped to Project Manager Role & Team Skills

S.No	Questions	Data Type	Response				
1	Organization	Text					
2	Number of Employees	Integer	0-1000	1000- 5000	5000-10000	>10000	
3	Department /Role	Text	Project Manager	Master/Team Member	Business Analyst	Management	Developer/Tester
4	Total Experience in IT projects in Years	Text	0-5	5-10 years	10-20 years	> 20 Years	
5	Have you worked/associated with Projects using Agile ?	Integer	Yes	No			
6	Have you worked/associated with Projects using DevOps?	Integer	Yes	No			
7	What % of applicable projects in your organization are implementing DevOps/Agile	Text	0-20%	20-50%	> 50%		
8	Years of Experience working on Agile/Devops practices	Text	No Experience	0-5 years	5-10 years	> 10 years	
	Skills needed for Project Manager, Team Skill set						
27	Is the Senior Management involved in improving the collobration between Devlopment team and Operations team	Likart Scale	1.Strongly disagree	2. Disagree	3. Neither agree nor disagree	4. Agree	5. Strongly agree
28	How would you describe the role of Scrum Masters on your projects		Scrum Masters Role	Dedicated Scrum Master Role	addition to Scrum Master	Project Manager will	
29	As an project team member, do you agree the role of Scrum master is different from traditional Project Manager?	Likart Scale	1.Strongly disagree	2. Disagree	3. Neither agree nor disagree	4. Agree	5. Strongly agree
30	Are the practices of Scrum leading to "Servant Leader and Facilitator" rather than "Manager and Controller" kind of leadership ?	Likart Scale	1.Strongly disagree	2. Disagree	3. Neither agree nor disagree	4. Agree	5. Strongly agree
31	Is the Function of project management is being reorganized into roles like scrum masters and product owners	Likart Scale	1.Strongly disagree	2. Disagree	3. Neither agree nor disagree	4. Agree	5. Strongly agree
32	Skill Set preferred for the team	Text	High Coding Skills	Testing Skills	Generalist (Communication, Technical, Business Analyst)	Tool Integration, CI/CD tools usage	Requirement Analysis & Design

3.1.2 Identification of IT companies for the survey

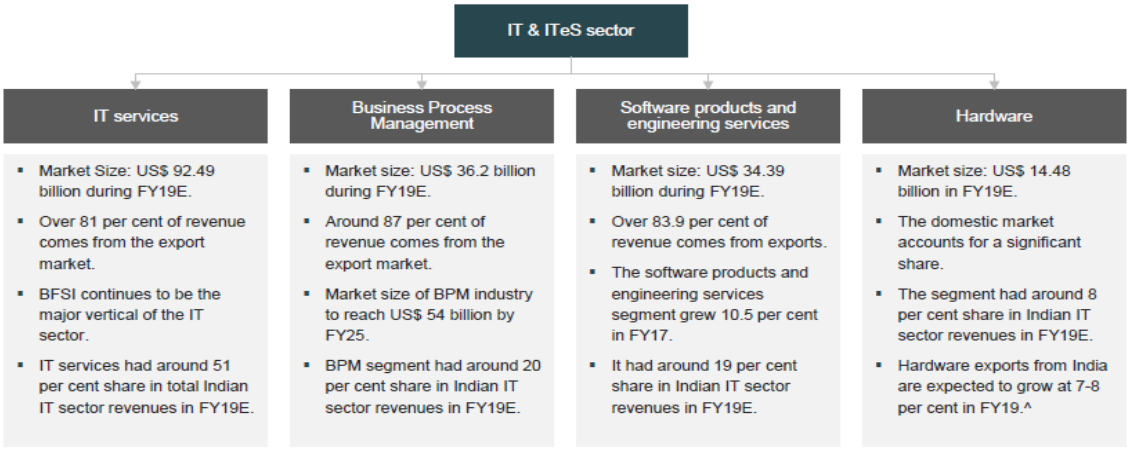
The first source was ET 500 from where we could pick Indian IT companies listed in India. We had to identify another source since many MNC's do not report data in India. DNB publishes top 500 companies in India and has separate section on Software & BPM. It has list of 21 Top Software companies in Top 500. DataQuest (DQ) was another magazine from where data for many IT companies was identified.

Various Segments on India 's IT sector

- **IT services**
- Business process Management
- **Software products and engineering services**
- Hardware

Software products and IT services were identified as targeted area since these companies would have software development practices and project structure in place.

Table 2 : Segments of Indian IT sector



Source: *NASSCOM, TechSciResearch , News sources*

India 's IT sector Size

The Indian IT sector is dominated by large players and top 11 occupying almost 50% of the revenue. Another Top 10 companies would cater to 20-25% of the revenue. So the plan was to target Top 50 companies we would be able to target approximately 85% to 90% of the revenue and team strength

Table 3 : Indian IT sector Revenue and Headcount segment

Category	Number of players	Percentage of total export revenue	Percentage of total employees	Work Focus
Large	11	47-50%	~35-38%	▪ Fully integrated players offering complete range of services ▪ Large scale operations and infrastructure ▪ Presence in over 60 countries
Medium	120-150	32-35%	~28-30%	▪ Mid tier Indian and MNC firms offering services in multiple verticals ▪ Dedicated captive centres ▪ Near shore and offshore presence in more than 30-35 countries
Emerging	~1,000-1,200	9-10%	~15-20%	▪ Players offering niche IT-BPM services ▪ Dedicated captives offering niche services ▪ Expanding focus towards sub Fortune 500/1,000 firms
Small	~15,000	9-10%	~15-18%	▪ Small players focussing on specific niches in either services or verticals ▪ Includes Indian providers and small niche captives

Source: *NASSCOM*

The companies identified were also mapped to prime activities and companies engaged in software development , product development were mapped and targeted for survey. The large companies will have identified roles and

Table 4: Identification of IT companies for the Survey (Top 50 by Size & applicability)

S.No	Company	Headcount	Revenue (In Crs)	Remarks	Survey
1	TCS	448000	126745		Yes
2	Infosys	242371	73762		Yes
3	Cognizant	292000	97814		Yes
4	Wipro	175000	56986		Yes
5	HCL Technologies Limited	117000	51695		Yes
6	IBM	140000	35880		Yes
7	TechM	117000	32189		Yes
8	HP India	20000	16400		Yes
9	Cisco India	10000	13351		Yes
10	Capgemini	120000	12800		Yes
11	Microsoft India	8000	10,600		Yes
12	Larsen & Toubro Infotech Ltd	31000	7732		Yes
13	APC by Schneider Electric India		6848	UPS, BackUP, Data Centre software	No
14	Mphsais Limted	21997	6707		Yes
15	Vakrangee Limited	1706	6505		Yes
16	Mindtree limited	16470	5653		Yes
17	Oracle financial services software Limited	8818	4618		Yes
18	Cyient Limited		4070	Engineering design, Geospatial, CAD/CAM	No
19	Hexaware Technologies Limited	19000	3990		Yes
20	HCL Limited		3959	Primarily Hardware	No
21	L&T technology services limited	22000	3940		Yes
22	Birla Soft	9995	3701		Yes
23	Zensar Technologies limited	10000	3175		Yes
24	Persistent Systems limited	10600	3152		Yes
25	NIIT technologies Limited	9500	3030		Yes
26	CSC India		2961	Not In ET	Yes

27	KPIT Technologies limited		2910	Not In ET 500, 2018	Yes
28	Rolta India Limited	2700	2888		Yes
29	Sonata Software		2500		Yes
30	Polaris Consulting & Services Limited		1530	Not In ET	Yes
31	Hinduja Global Solutons Limited		1624	Primarily BPO	No
32	Tata Elxsi limited		1249	Not In ET	Yes
33	eClerx Services Limited		1190	Primarily BPO, Not In ET	No
34	Syntel India		5586	Not listed In India	Yes
35	Accenture			Not Listed	Yes
36	Aricent Technologies Limited			Not Listed	Yes
37	Ericsson			Primarily telecom but good software development	Yes
38	Genpact			Primarily BPO	No
39	Ingram Micro India		24823	Distribution and IT supply chain management	No
40	Redingtion India		18700	Primarily Hardware	No
41	Dell India		16905	Primarily Hardware	No
42	Lenovo India		9075	Primarily Hardware	No
43	Intel India		7905	Primarily Hardware	No
44	Savex Computer		5905	Primarily Hardware	No
45	Acer India		3692	Primarily Hardware	No
46	Samsung India		3995	Primarily Hardware	No
47	IRIS computer		2573	IT distributon	No
48	Rashi Peripheral		2984	Primarily Hardware	No
49	Compuage Infocom		2129	Primarily Hardware	No
50	CMC India		2513	Part of TCS	No

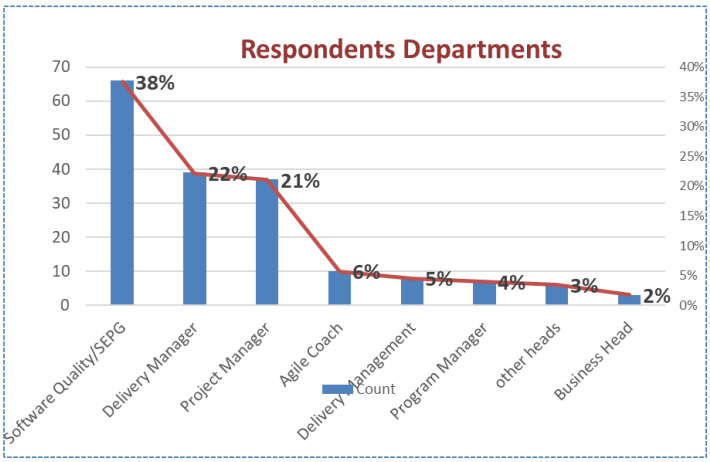
IV. FINDINGS AND DISCUSSION

Once the companies were identified, the survey was launched on Survey Monkey. We had response from 176 respondents with the response frequency of 317

4.1 Demographic analysis

Table 5 : Role wise distribution of the respondents

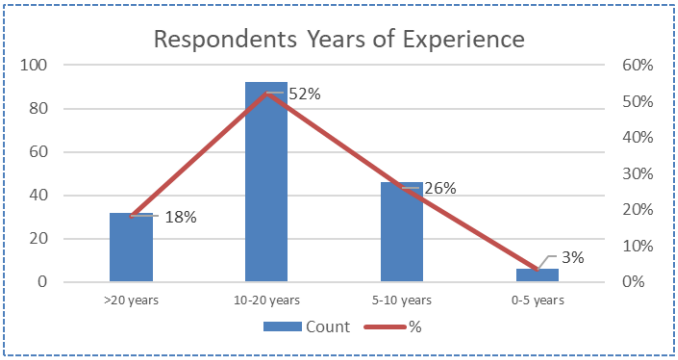
Department	Count	%
Software Quality/SEPG	66	38%
Delivery Manager	39	22%
Project Manager	37	21%
Agile Coach	10	6%
Delivery Management	8	5%
Program Manager	7	4%
other heads	6	3%
Business Head	3	2%
Grand Total	**176**	



From above it is found that the 38% of the respondents are software quality /SPEG executives, 22% of the respondents are delivery managers and 21% of the respondents are project managers. 5% and 6 % of the respondents are from delivery management department, program managers, agile coach and other heads. Only 2% of the respondents are Business Heads or higher authorities.

Table 6: Respondents Experience in IT projects & Agile/DevOps

Years Of Experience	Count
>20 years	32
10-20	92
5-10	46
0-5	6
Grand Total	176



From above it is found that 52% of the respondents are having 10-20 years of experience as total industrial (IT) experience.27% of the respondents are having 5 to 10 years of experience and 18 % of the respondents are having above 20 years of experience. only 3% of the respondents are having 0-5 years of experience

Table 7: Respondents' organization details

Name of Organization	Frequency	Percent
Infosys	22	7.0
Aricent Technologies Limited	19	6.0
Tech Mahindra	15	4.8
Wipro	14	4.4
NIIT technologies Limited	14	4.4
Cognizant	13	4.1
Persistent Systems limited	13	4.1
TCS	12	3.8
HCL	12	3.8
Birla Soft	12	3.8
Ericsson Inc	12	3.8
HP India	11	3.5
Rolta India Limited	11	3.5
CGI	10	3.2
Mind tree limited	10	3.2
Syntel India	10	3.2
Hexaware Technologies Limited	10	3.2
Polaris Consulting & Services Limited	10	3.2
Larsen & Toubro InfoTech Ltd	9	2.9
Mphsais Limited	9	2.9
Zensar Technologies limited	9	2.9
Tata Elxsi	9	2.9
Capgemini	8	2.5
Accenture	8	2.5
IBM	7	2.2
CSC India	7	2.2
KPIT	7	2.2
Sonata Software	6	1.9
Deloitte	4	1.3
No response/confidentiality	1	.3
Icare	1	.3
Total	315	100.0

4.2 Descriptive Analysis

Table 8: Descriptive Analysis on Project Manager Skill & Team Skill

	N	Min	Max	Mean	Std. Deviation
Are the practices of Scrum leading to "Servant Leader and Facilitator" rather than "Manager and Controller" kind of leadership	315	2	5	3.94	.852
As a project team member, do you agree the role of Scrum master is different from traditional Project Manager?	315	1	5	3.74	1.297
Is the Senior Management involved in improving the collaboration between Development team and Operations team	315	1	5	3.56	.870
Is the Function of project management is being reorganized into roles like scrum masters and product owners	315	1	5	3.55	.951
Valid N (listwise)	315				

From table 8 it is found that both agile and non-agile group respondents are agreed that the practices of Scrum will lead to "Servant Leader and Facilitator" rather than "Manager and Controller" kind of leadership. Also agreed that the role of Scrum master is different from traditional Project Manager and they are opined that there is a need of separate scrum master for their projects. The Senior Management involvement is good for improving the collaboration between Development team and Operations team and the function of project management is being reorganized into roles like scrum masters and product owners.

Table 9: Description of scrum master role

How would you describe the role of Scrum Masters on your projects?	Frequency	Percent
Dedicated Scrum Master Role	81	50
Project Manager in addition to Scrum Master	75	46
Traditional Project Manager will act as role of Scrum Master	6	4
Total	162	100

From table 9 it is found that 50% of the agile respondents are described role of scrum master as dedicated role in their project.46% of the respondents stated that Project Manager in addition to Scrum Master is required for their project. Only 4% of the respondents are opined that Traditional Project Manager will act as role of Scrum Master.

Table 10: Cross tabulation of Agile/Non Agile group with skill preference for team

		Skill Set preferred for the team				Total
		Specific Coding/Testing Skills	Generalist (Communication, Technical, Business Analyst)	Tool Integration, CI/CD tools usage	Requirement Analysis & Design	
Agile	Count	23	88	45	6	162
	%	14.2%	54.3%	27.8%	3.7%	100.0%
Non-Agile	Count	40	51	49	13	153
	%	26.1%	33.3%	32.0%	8.5%	100.0%
	Count	63	139	94	19	315
	%	20.0%	44.1%	29.8%	6.0%	100.0%

From table 10 it is found that both agile and non-agile group respondents ranked high for general skill set like Communication skill, Technical skill and Business Analyst skill mandatory for team .The next ranking for tool integration skill and CI/CD tools usage skill are given by both the group.

4.3 Hypothesis Analysis

H1N: There is no difference in Senior Management involvement in improving the collaboration of development team and Operations team between Agile/devops and non-agile projects

H1A: There is a difference in Senior Management involvement in improving the collaboration of development team & Operations team between Agile/devops and non-agile projects.

Table 11: Chi-Square Test - Senior Management involvement in improving the collaboration of development team & Operations team

Agile :Senior Management involvement in improving the collaboration of development team and Operations team			
	Observed N	Expected N	Residual
strongly disagree	2	27.6	-25.6
Disagree	17	27.6	-10.6
Neither agree nor disagree	25	27.6	-2.6
Agree	71	27.6	43.4
Strongly agree	23	27.6	-4.6
Total	138		

Non-Agile :Senior Management involvement in improving the collaboration of development team and Operations team			
	Observed N	Expected N	Residual
strongly disagree	20	27.6	-7.6
Disagree	22	27.6	-5.6
Neither agree nor disagree	19	27.6	-8.6
Agree	66	27.6	38.4
Strongly agree	11	27.6	-16.6
Total	138		

Test Statistics		
	Agile :Senior Management involvement in improving the collaboration of development team and Operations team	Non-Agile :Senior Management involvement in improving the collaboration of development team and Operations team
Chi-Square	97.072[a]	69.319[a]
df	4	4
Asymp. Sig.	.000	.000
a. 0 cells (0.0%) have expected frequencies less than 5. The minimum expected cell frequency is 27.6.		

From table 11 it is found that the Senior Management involvement in improving the collaboration of development team and Operations team take places highly on agile projects.

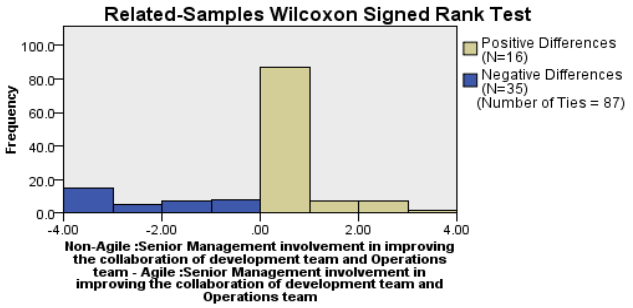
Table 12: Hypothesis-13 test summary

Hypothesis Test Summary

	Null Hypothesis	Test	Sig.	Decision
1	The median of differences between Agile :Senior Management involvement in improving the collaboration of development team and Operations team and Non-Agile :Senior Management involvement in improving the collaboration of development team and Operations team equals 0.	Related-Samples Wilcoxon Signed Rank Test	.000	Reject the null hypothesis.

Asymptotic significances are displayed. The significance level is .05.

Figure 1: Wilcoxon signed rank test for hypothesis 13



Total N	138
Test Statistic	279.500
Standard Error	105.724
Standardized Test Statistic	-3.627
Asymptotic Sig. (2-sided test)	.000

From table 12 and figure 1 shows the hypothesis test result that the null hypothesis is rejected therefore there is a difference in Senior Management involvement in improving the collaboration of development team & Operations team between Agile/devops and non-agile projects.

H2N: There is no difference in reorganization of project management function into roles like scrum masters and product owners between Agile/devops and non-agile projects

H2A: There is a difference in reorganization of project management function into roles like scrum masters and product owners between Agile/devops and non-agile projects.

Table 13: Chi-Square Test - reorganization of project management function into roles like scrum masters and product owners

Agile :reorganization of project management function into roles like scrum masters and product owners			
	Observed N	Expected N	Residual
strongly disagree	2	27.6	-25.6
Disagree	23	27.6	-4.6
Neither agree nor disagree	30	27.6	2.4
Agree	68	27.6	40.4
Strongly agree	15	27.6	-12.6
Total	138		
Non-Agile :reorganization of project management function into roles like scrum masters and product owners			
	Observed N	Expected N	Residual
Disagree	29	34.5	-5.5
Neither agree nor disagree	9	34.5	-25.5
Agree	86	34.5	51.5
Strongly agree	14	34.5	-20.5
Total	138		

Test Statistics

	Agile :reorganization of project management function into roles like scrum masters and product owners	Non-Agile :reorganization of project management function into roles like scrum masters and product owners
Chi-Square	89.609[a]	108.783[b]
df	4	3
Asymp. Sig.	.000	.000

a. 0 cells (0.0%) have expected frequencies less than 5. The minimum expected cell frequency is 27.6.

b. 0 cells (0.0%) have expected frequencies less than 5. The minimum expected cell frequency is 34.5.

From table 13 it is found that in both agile and non-agile projects reorganization of project management function into roles like scrum masters and product owners take places

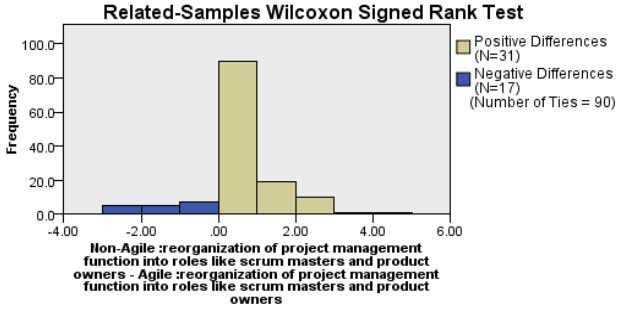
Table 14: Hypothesis-14 test summary

Hypothesis Test Summary

	Null Hypothesis	Test	Sig.	Decision
1	The median of differences between Agile :reorganization of project management function into roles like scrum masters and product owners and Non-Agile :reorganization of project management function into roles like scrum masters and product owners equals 0.	Related-Samples Wilcoxon Signed Rank Test	.289	Retain the null hypothesis.

Asymptotic significances are displayed. The significance level is .05.

Figure 14: Wilcoxon signed rank test for hypothesis 14



Total N	138
Test Statistic	689.000
Standard Error	95.216
Standardized Test Statistic	1.061
Asymptotic Sig. (2-sided test)	.289

From table 14 and figure 2 shows the hypothesis test result that the null hypothesis is accepted therefore there is no difference in reorganization of project management function into roles like scrum masters and product owners between Agile/devops and non-agile projects

H3N: There is no difference in perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role between Agile/devops and non-agile projects

H3A: There is a difference in perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role between Agile/devops and non-agile projects

Table 15: Chi-Square Test - perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role

Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role

	Observed N	Expected N	Residual
strongly disagree	20	27.6	-7.6
Disagree	6	27.6	-21.6
Neither agree nor disagree	12	27.6	-15.6
Agree	50	27.6	22.4
Strongly agree	50	27.6	22.4
Total	138		

Non-Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role

	Observed N	Expected N	Residual
strongly disagree	18	27.6	-9.6
Disagree	5	27.6	-22.6
Neither agree nor disagree	22	27.6	-5.6
Agree	53	27.6	25.4
Strongly agree	40	27.6	12.4
Total	138		

Test Statistics

	Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role	Non-Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role
Chi-Square	64.174[a]	51.928[a]
df	4	4
Asymp. Sig.	.000	.000

a. 0 cells (0.0%) have expected frequencies less than 5. The minimum expected cell frequency is 27.6.

From table 15 it is found that project team member in both agile and non-agile project agreed that Scrum master's role differed from traditional Project Manager's role

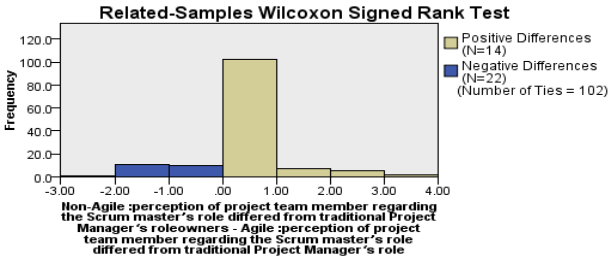
Table 16: Hypothesis-15 test summary

Hypothesis Test Summary

	Null Hypothesis	Test	Sig.	Decision
1	The median of differences between Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role and Non-Agile :perception of project team member regarding the Scrum master's role differed from traditional Project Manager's roleowners equals 0.	Related-Samples Wilcoxon Signed Rank Test	.243	Retain the null hypothesis.

Asymptotic significances are displayed. The significance level is .05.

Figure 3: Wilcoxon signed rank test for hypothesis 15



Total N	138
Test Statistic	260.500
Standard Error	62.161
Standardized Test Statistic	-1.166
Asymptotic Sig. (2-sided test)	.243

From table 16 and figure 3 shows the hypothesis test result that the null hypothesis is accepted therefore there is no difference in perception of project team member regarding the Scrum master's role differed from traditional Project Manager's role between Agile/devops and non-agile projects.

H4N: There is no difference in perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller between Agile/devops and non-agile projects

H4A: There is a difference in perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller between Agile/devops and non-agile projects

Table 17: Chi-Square Test - perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller

Agile :perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller			
	Observed N	Expected N	Residual
Disagree	12	34.5	-22.5
Neither agree nor disagree	11	34.5	-23.5
Agree	74	34.5	39.5
Strongly agree	41	34.5	6.5
Total	138		
Non-Agile :perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller			
	Observed N	Expected N	Residual
Disagree	14	34.5	-20.5
Neither agree nor disagree	18	34.5	-16.5
Agree	86	34.5	51.5
Strongly agree	20	34.5	-14.5
Total	138		

Test Statistics

	Agile :perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller	Non-Agile :perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller
Chi-Square	77.130[a]	103.043[a]
Df	3	3
Asymp. Sig.	.000	.000

a. 0 cells (0.0%) have expected frequencies less than 5. The minimum expected cell frequency is 34.5.

From table 17 it is found that the project team members are highly agreed that the scrum leadership would leads to Servant Leader and Facilitator" rather than "Manager and Controller while working in agile project.

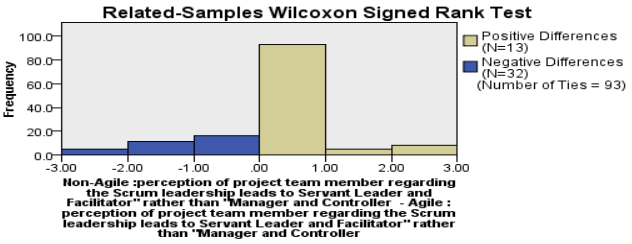
Table 18: Hypothesis-16 test summary

Hypothesis Test Summary

	Null Hypothesis	Test	Sig.	Decision
1	The median of differences between Agile :perception of project team member regarding the Scrum leadership leads to Servant Leade and Facilitator" rather than "Manager and Controller and Non-Agile :perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller equals 0.	Related-Samples Wilcoxon Signed Rank Test	.013	Reject the null hypothesis.

Asymptotic significances are displayed. The significance level is .05.

Figure 4: Wilcoxon signed rank test for hypothesis 16



Total N	138
Test Statistic	303.000
Standard Error	86.667
Standardized Test Statistic	-2.475
Asymptotic Sig. (2-sided test)	.013

From table 18 and figure 4 shows the hypothesis test result that the null hypothesis is rejected therefore there is a difference in perception of project team member regarding the Scrum leadership leads to Servant Leader and Facilitator" rather than "Manager and Controller between Agile/devops and non-agile projects.

V. CONCLUSION, RECOMMENDATIONS AND FUTURE WORK

The present study has reviewed about the impact of Agile and DevOps methodologies on Project Management Practices and Team structure. It is evident from the review that the impact of Agile and DevOps methodologies can produce significant effect on the project manager role and team structure. This paper provides better insights about how Agile and DevOps creates significant impact on the project management practices and team structure. Hence this research provides new insights for the future researchers to understand the Agile and DevOps and how it significant impacts on the industry. This research has both theoretical as well as practical implications.

The following are the finding for sectors that wish to implement Agile and DevOps methodologies for their software development process:

- There is a difference in Senior Management involvement in improving the collaboration of development team & Operations team between Agile/devops and non-agile projects. Senior Management involvement in improving the collaboration of development team and operations team take places highly on agile projects.
- Respondents working in both agile and non-agile projects opined that reorganization of project management function into roles like scrum masters and product owners are needed. The business need to changing the characteristics of Project Manager role and is more inclined to Scrum master values.

- Project team members are highly agreed that the scrum leadership would leads to Servant Leader and Facilitator" rather than "Manager and Controller while working in agile project.
- The focus is to have general skill set like Communication skill, Technical and Business Analyst skills apart from the technical skills. The next ranking is for tool integration skill and CI/CD tools usage.

Senior Management involvement

The traditional concept of management has always been vertical but the senior management in Agile should be a horizontal they have to align with the functional area of the team members.(McKnight, 2017) and also they need to focus more on why & what to influence the employees' mind-set, behaviour of groups, teams and departments.(ZHU, 2015)

Scrum leadership

Scrum leadership will guide the team with what is wrong with the way they currently doing work, and how a simple set of principles, applied in exactly the right sequence, can accelerate double the productivity and quality in half the time.(Sutherland, 2014)

In future, the work can be extended by conducting and validating the study in the proposed area and it can be achieved by conducting on different sample size and data.

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Design and Implementation of a Prototype for Prevention of Covid-19 Spread

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Abstract— Major travel hubs like airports, railway stations, and bus stations are some of the points on which the security measures of public authorities are aimed when infectious diseases such as the Corona virus (2019-nCoV, COVID-19, SARS-CoV-2) cause global problems. In this paper, the user stimulate a room where the necessary precautions have been taken. Here a laser diode and a receiver is used to detect a person's entrance, and if a person is being detected at the entrance, the person's temperature is checked. If the temperature of the person is normal body temperature only then the person is allowed to enter else the entry is denied. Also, a predetermined number of people are allowed to stay in the room. In this paper, the users can set and also monitor the temperature of the person entering, and the number of people actively attending the room. In this paper an Arduino based prototype is designed and implemented to detect the covid -19 patients and notify them with a buzzer and also there is only limited number of people allowed inside a room by opening and closing the gate and if a person exit the room the count of people in the room will be decreased automatically.

Key Words— Arduino, Temperature sensor, Relay, Covid-19, Sanitization, IR sensor

I. INTRODUCTION

COVID 19 has made a huge impact on the society and its economy. The new restriction has been imposed in the number of users allowed in a particular room either in offices, shops, etc. to maintain social distancing. In addition, regular temperature check at entrances of malls and offices is made mandatory. Fever is one of the most important symptoms [**1**] of COVID-19, but due to the contagious effect, its measurement can become a serious problem, so it is important to perform the temperature detection of patients very quickly and possibly without any contact. On the other hand, both epidemiological and laboratory studies have revealed that ambient temperature could affect the survival and spread of Coronavirus [**2**] so there is a need of continuous monitoring of temperature, regarding both ambient and body temperature. To implement this method of monitoring, time and energy consumption of the person to check every person entering is more. To reduce the time and energy consumed and to allow a smooth process the idea for this prototype was implemented. As per the guidelines, the gathering of people in a particular place is reduced to half of the normal scenario.

The additional monitoring of ambient temperature can be strongly helpful to improve the accuracy in the detection of human body temperature, the measurement of which can be affected by the environmental humidity. Furthermore, recent studies have confirmed the effects of environmental temperature and humidity values in the increased risk of COVID-19 transmission [**3**].

II. LITERATURE SURVEY

In the paper by Nenad Petrović and Đorđe Kocić has fostered a moderate IoT-based arrangement meaning to build a COVID-19 indoor security which covering a few significant viewpoints like contactless temperature detecting, veil location, social separating check. The contactless temperature detecting subsystem depends on Arduino Uno utilizing an infrared sensor or warm camera, while cover identification and social separating check are performed by utilizing PC vision methods on camera-prepared Raspberry Pi. According to the outcomes, the arrangement is usable for some certain execution impediments. In future progressions, they are attempting to foster different profound learning and PC vision systems for object location on Raspberry Pi to accomplish higher frame rate. Besides, they will broaden this arrangement with climate detecting components for versatile structure cooling and ventilation airborne insurance to lessen the spread of Covid inside, particularly during summer. At last, a definitive objective of them is to coordinate the framework introduced in this paper with the structure for productive asset arranging during the pandemic emergency to empower proficient security faculty planning and cover allotment, along with hazard appraisal dependent on measurements about regarding the wellbeing rules and air quality.

This paper portrays a hearty self-ruling sterilization passage to clean outer surfaces of the Coronavirus infection, for example, garments and open body segments out in the open places like air terminals, office edifices, schools, and shopping centres. To make the passage viable and profoundly proficient, it has been furnished with two chambers with three sanitization measures. Because of the different cycles, the chance of killing the infection is very high and higher than different arrangements accessible now for this reason. Chamber 1 showers the arrangement of a sanitizer on the individual entering. This arrangement can be either a weaken arrangement of a supported substance or any Ayurvedic/home grown sanitizer. When the individual

enters chamber 2, he/she is presented to hot air at 70 °C alongside far-bright C beams (207–222 nm). The two chambers work self-sufficiently by distinguishing an individual in a chamber utilizing ultrasonic sensors. This proposed burrow is created under industry-the scholarly community cooperation together by Technopark@iitk and ALIMCO under the ambit of the Service of HR Improvement and the Service of Social Equity and Strengthening, individually. This paper is alluded to as the 'Techno Progressed Sterilization Passage' (TADT). As per the outcomes, in the primary chamber, the individual is sanitized by the splashing of the ionized fog of an endorsed sanitizer answer for 20 s. The electrostatic spouts utilized in the chamber produce super fine drops of size < 30 microns permitting negligible utilization of a sanitizer. In the subsequent chamber, the individual is presented to hot air for around 20s and a protected frequency of far-UVC radiations for 15s at the same time. Every one of these cycles are performed self-sufficiently, where the presence of an individual is distinguished utilizing ultrasonic sensors. This 'Techno Progressed Sanitization Passage's effectively evolved under industry-the scholarly community joint effort at IIT Kanpur. This work can be stretched out to versatile sterilization burrows for vehicles/bikes and lightweight chambers at air terminals.

The objective of the project proposed is to stimulate a room where the necessary precaution has been taken such as temperature detection, sanitization and limited room count is maintained. The steps to be followed to implement the objective are:

The design and layout of the project which consists of the planning the flow of project, choosing the prefect hardware components for the prototype and their position to be placed on the prototype

1 Write C++ code for the following modules such as temperature, opening and closing of gate, sanitization kit, count inside the room and buzzer.

2 Compiling and verifying the code to check whether the code written is error free and all the programmed modules function as planned.

3 Dumping the code into Arduino Uno board and check for result for wireless temperature sensor, buzzer, infrared sensor, sanitizer circuit and the gate.

4 Simulation of result after dumping the code and practically check the working of the prototype and verify the results.

III. IMPLEMENTATION AND DESIGN

As covid-19 has changed a lot of things in our daily lives, such as maintaining social distance, washing or sanitising hands every time someone goes out. It even had a large impact on the world economy. However it would take some ample time to irradigate the virus completely by wearing mask, maintaining social distance and getting vaccined and practicing the pattern that WHO released can eventually prevent the virus spread.

The steps involved in the working of the prototype are as follows. This prototype is placed near the gate, door, or at the entrance of any public places.

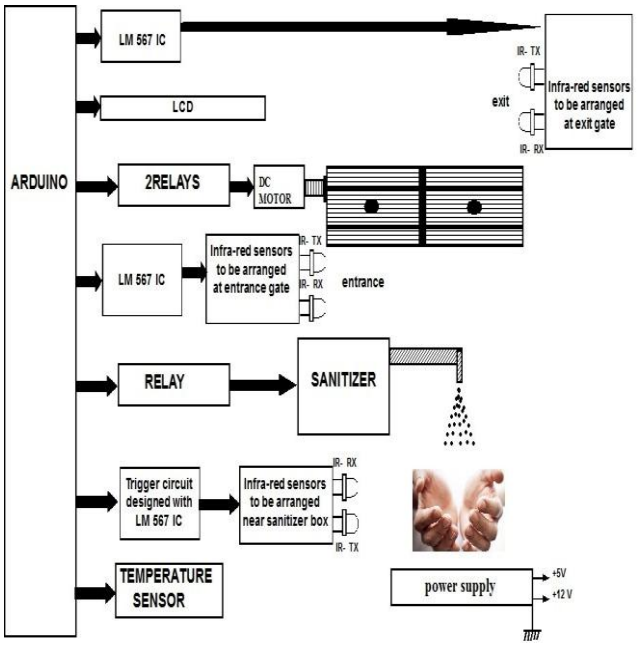

Fig.3.1 Block diagram of Prototype for Prevention of Covid19 Spread.

When a person tries to enter, an interrupt is sensed by the Infrared Sensors placed at the entrance. This indicates the entry of a person willing to enter inside the room. A Temperature Sensor is placed right next to the Infrared Sensors. The prototype model detects the entry and also the temperature of the person entering. These sensors sense the temperature of the person entering the room. If the temperature is below the temperature set in the prototype, the person is allowed into the room as the person entering has a normal body temperature the gates open and entry is allowed. The sanitizer sprinkler is provided near the entrance so that he/she is getting self- sanitized. When the person enters the room, the count of the number of persons available in the room is increased by one. If the temperature is above the temperature set, then the entry for the person is denied and the buzzer goes 'ON' indicating that the person's body temperature is above the temperature set. The model is designed in such a way that the number of people present inside the simulated room can be monitored, and hence the capacity of the room is made limited. So only a limited number of people are allowed into the room. An LED display is used to display the temperature of the person as well as the number of people present in the room.

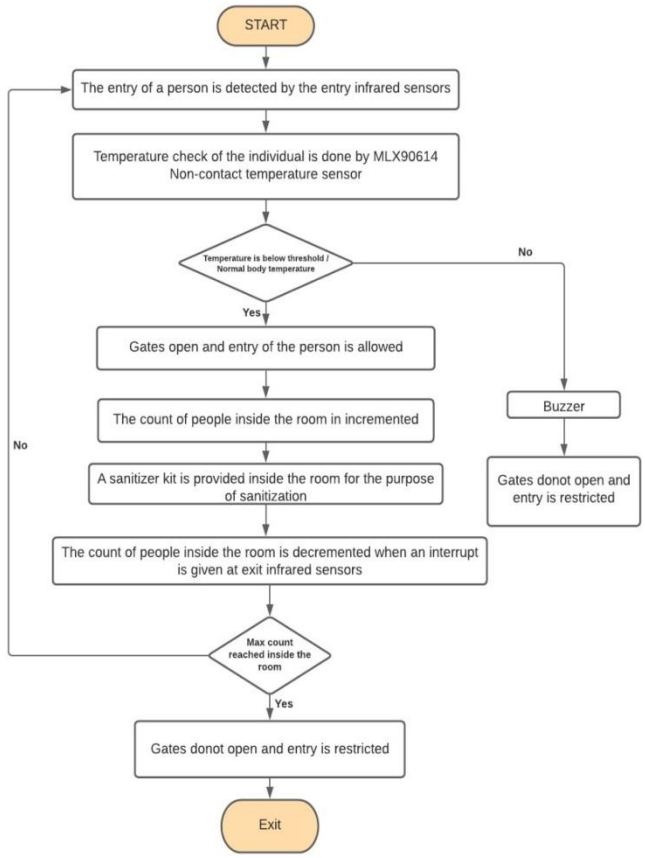

Fig 3.2 flow chart for project

Another set of Infrared sensors are placed at the exit of the room to count the number of people exiting the room. When someone exits, the count of people available in the room is decreased by a count 1 which is displayed on the LCD. If the temperature is above the threshold or if the temperature of the person entering the room is high, the gates do not open and entry is restricted. A buzzer is placed in the prototype model to indicate a warning of high temperature. A Sanitizer sprinkler is kept near the entrance of the room so that immediately after the person enters and interrupts the IR sensors the sanitizer sprinkler, sprinkles the sanitizer liquid. And also the number of entries inside the room are limited to avoid suffocation.

The above-mentioned process continues until the maximum count set is reached. Once the maximum count is reached, even if a person with normal body temperature tries to enter inside the room is restricted and the gates do not open. As mentioned earlier, to reduce the count of people inside the room someone should exit. So whenever a person exits out an interrupt is given to the IR sensors at the exit door and the count is reduced to 9. Now there is a possibility of another person to enter and hence he is allowed.

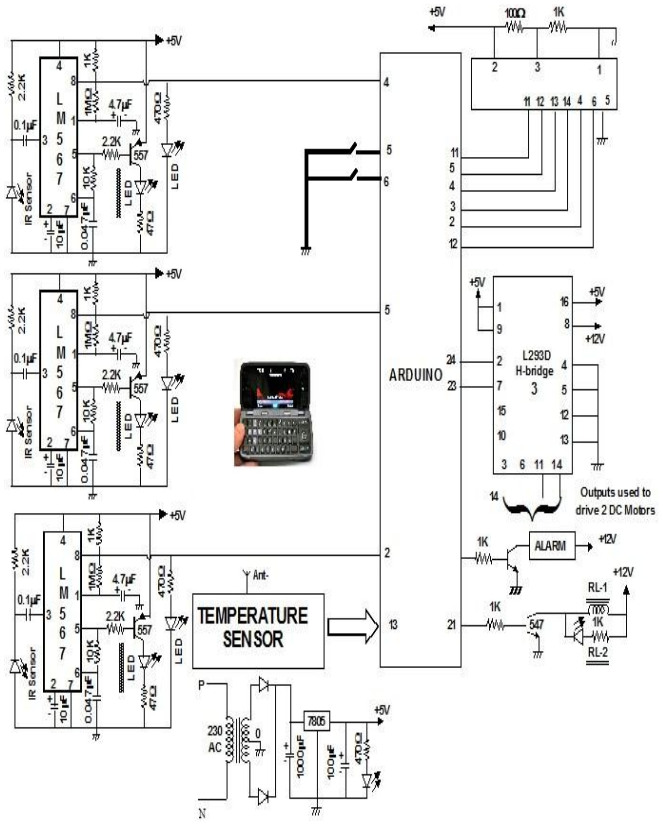

Fig 3.3 Schematic diagram

- Vin: - Input voltage to Arduino when using an external power source.
- 5V: - Regulated power supply used to power microcontroller and other components on the board.
- 3.3V: - 3.3V supply generated by on-board voltage regulator. Maximum current draw is 50mA.
- GND: - ground pin.

Analog pins:

- A0: Analog pin is connected to Temperature sensor.
- A2: Analog pin is connected to Infrared Sensor.

Data Pins

- Pin D6: It is connected to Entry Count.
- Pin D7: It is connected to Exit count.
- Pin D8: It is connected to Relay1.
- Pin D9: It is connected to Relay 2.
- Pin D10: It is connected to Sanitizer.
- Pin D13: It is connected to Buzzer.
- Pin D2-pin D5: These are connected to LCD (Liquid crystal display) D0- D3.
- Pin D11: It is connected to Enable pin of LCD.
- Pin D12: It is connected to Register select of LCD

IV. RESULTS

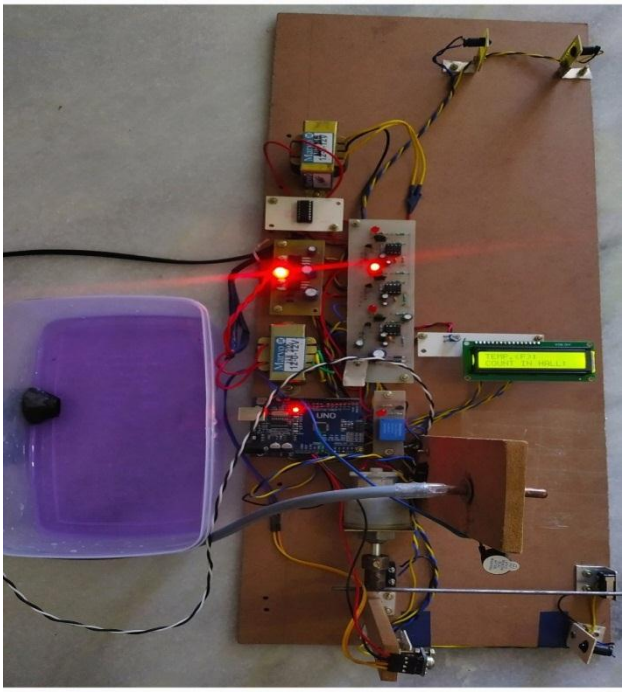

Fig 4.1 Prototype Model Top View

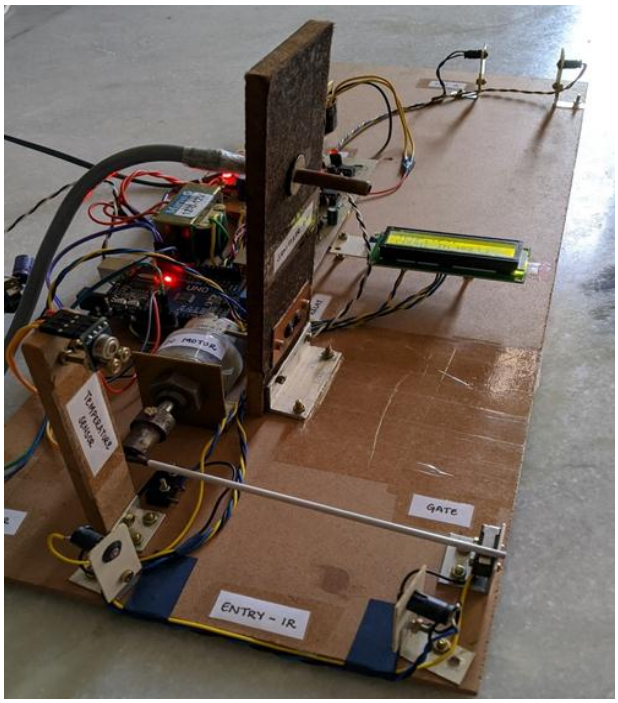

Fig 4.2 Prototype model Front View

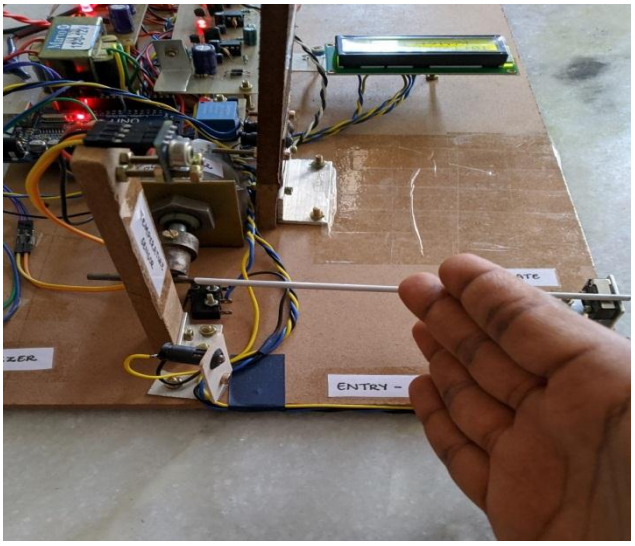

Fig 4.3 When IR sensor detects a person at the entrance of the room.

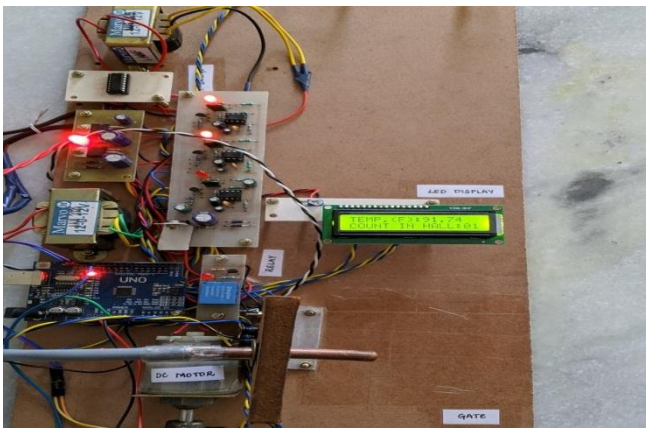

Fig 4.4 Temperature of the person entering and count of persons present in the room are displayed on LCD

In this model the count is set and limited to 10, so only ten individuals are allowed into room as shown in the pictures below in fig 4. 5. when the count reached the maximum limit set, a person is not allowed into the room as the gate will not be opened.

Fig 4.5 showing the person's count displayed as 10 in number

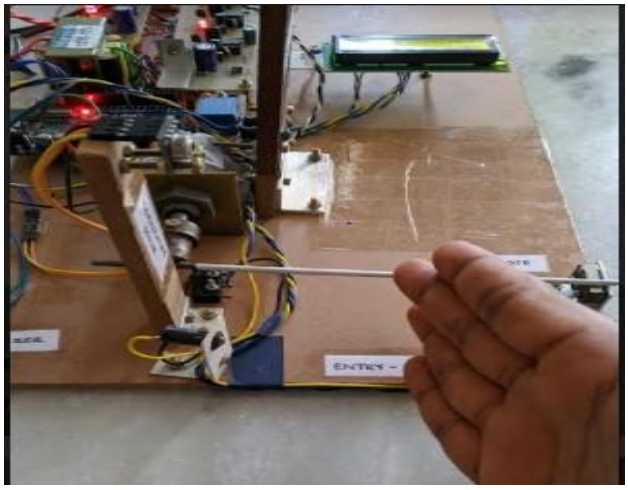

Fig 4.6 Displays the gate closure when a person wants to enter when the limit reaches the maximum count set.

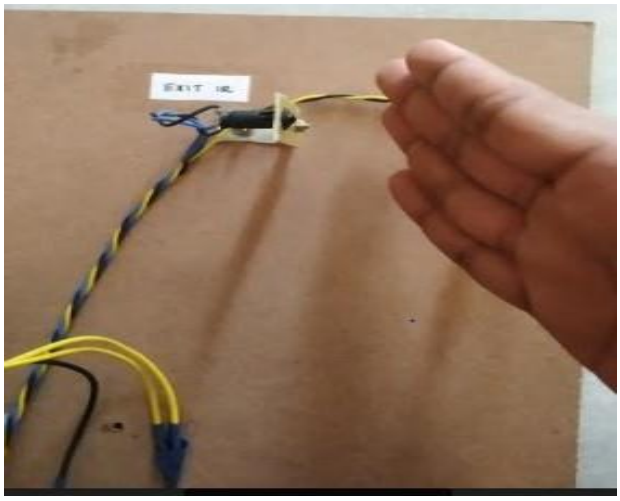

Fig 4.7 when a person exits from exit entrance the IR sensors are interrupted and the count of persons available is decreased by one.

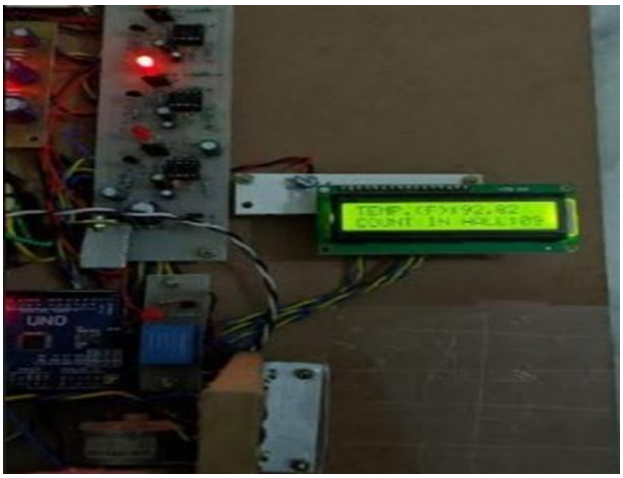

Fig 4.8 The count of persons in the room is displayed as count 9 on LCD

IV. CONCLUSION

This paper demonstrates developing a COVID-19 symptom monitoring system taking into account the importance of social distance in managing and reducing the probability of COVID-19 disease from continuously spreading which can cause the healthcare system to collapse due to high number of patients.

Hence, an Arduino based prototype is designed and implemented to detect the covid -19 patients and notify them with a buzzer and also there is only limited number of people allowed inside a room by opening and closing the gate and if a person exit the room the count of people in the room will be decreased automatically.

V. FUTURE SCOPE

We have restricted this project till temperature measuring, sanitizing, counting the number persons and also only particular number people can be allowed in the room. Because of the high cost we couldn't done the checking of the pulse rate .so for this project this is the future scope or else we have implemented this project using Arduino software they can use different software as well

VI. ACKNOLEDGEMENT

The authors acknowledge the help provided by Geethanjali college of engineering and technology, Hyderabad for using their facilities and for enabling the authors to carry out the experiments with ease.

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15th-16th July, 2021 – Virtual Conference

VHDL Implementation of Asynchronous GRAY Code Counter Using Reversible Logic Gates

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Abstract— Reversable logic gates has become one of the most promising research areas in the past few decades and has found its applications in several technologies due to its less heat dissipation and low power consumption.
A Gray code is an encoding of integers as sequences of bits with the property that represents the adjacent integers differ in exactly one binary position. There are different types of Gray codes binary reflected, balanced, antipodal, maximum gap etc. On the other hand, counters have a primary function of producing a specified output sequence and are thus sometimes referred to as pattern generators. this paper represents the design purpose of reversable Gray code counters for binary reflected, balanced, and antipodal Gray codes which are the most frequently used once in the design and technology.

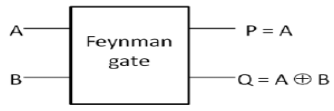
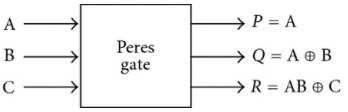
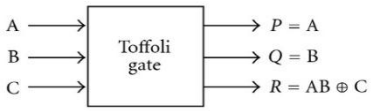
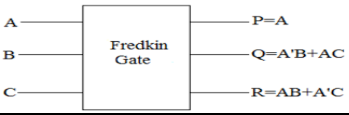
Key Words— Reversible logic gates, Gray code counters: Binary reflected, Balanced and Antipodal

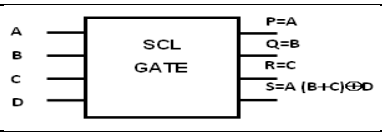
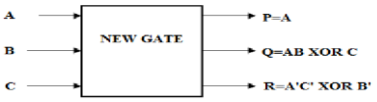
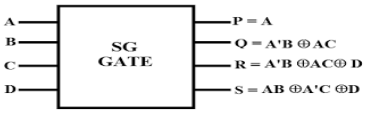
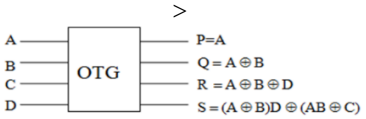
I. INTRODUCTION

Most digital circuits are designed as synchronous circuits. Yet, asynchronous circuits may offer some advantages, including lower power consumption and no clock skew. The asynchronous circuits face problems such as difficult design process and lack of design tools. Some issues are raised regarding performance advantage and power reduction of asynchronous circuits in comparison with synchronous circuits. Despite the development of asynchronous circuits, some factors make synchronous circuits predominate. Nevertheless, asynchronous circuits are used in research area [1]. On the other hand, Reversible circuits are those circuits that do not lose information. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Synthesis of reversible logic circuit differs from the combinational one in many ways. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly for each input pattern there should be unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible circuit design includes only the gates that are the number of gates, quantum cost and the number of garbage outputs [7]. According to Landauer's principle [10], the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant, T is the absolute temperature. In 1973, Bennett [13], showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits.

II. REVERSABLE LOGIC GATES:

A reversable logic gate is a memory-less logic element that realizes an injective logical function. The important reversible logic gates and a brief overview of some areas under.

Gate	Schematic representation	Inputs	Outputs
Feynman gate		A	P, Q
Peres Gate		A, B, C	P, Q, R
Toffoli Gate		A, B, C	A, B, C
Fredkin Gate		A, B, C	P, Q, R

SCL Gate		A, B, C, D	P, Q, R
TR Gate		A, B, C	P, Q, R
New Gate		A, B, C	P, Q, R
URG Gate		A, B, C	P, Q, R
Sayem Gate		A, B, C, D	P, Q, R, S
OTG Gate		A, B, C, D	P, Q, R, S

III. TYPES OF GRAY CODE COUNTERS

A Gray Code is an encoding of integers as sequences of bits with the property that the representations of adjacent integers differ in exactly one binary position. Some of the widely cited Gray codes are.

Binary Reflected Gray Code Counter: It is the most common form of Gray code and vastly superior in communications protocols. The sequence is shown in Table 1. But generally, this is not the optimal code for use as output for mechanical actuators where it is preferred to have a coding system that provides more uniformity. Two measures of uniformity are the transition counts and the gap of the code.

Uniformly Balanced Gray Code Counter: Gray codes with the additional property that the number of bit changes is more uniformly distributed among the bit positions. The sequence of UBGC in the lexicographical order is tabulated in table 1. below

Antipodal Gray Code Counter: An n-bit Antipodal Gray Codes have the additional property that the binary complement of any code string appears exactly n steps away in the list. Thus, the spatial frequency of the antipodal Gray code-pattern is similar along frames. The code is as shown in Table 1.

TABLE 1: DIFFERENT TYPES OF GRAY CODES

Binary reflected Gray code		Uniformly balance Gray code		Antipodal Gray codes	
0000	1100	0000	1010	0000	0110
0001	1101	0001	1011	0001	0100
0011	1111	0011	1001	0011	0101
0010	1110	0010	1101	0010	0111
0110	0101	0110	0101	0110	0011
0111	1011	0111	0100	0111	1011
0101	1001	0101	0110	0101	1001
0100	1000	0100	0010	0100	0001

IV. GRAY CODE COUNTERS USING REVERSABLE LOGIC GATES

The Reversable logic implementation of Binary Reflected, Uniformly Balanced and Antipodal Gray code counters are as follows.

Binary Reflected Gray Code Counter: It is the most common form of Gray code and vastly superior in communications protocols. The sequence is shown in Table 1. But generally, this is not the optimal code for use as output for mechanical actuators where it is preferred to have a coding system that provides more uniformity. Two measures of uniformity are the transition counts and the gap of the code.

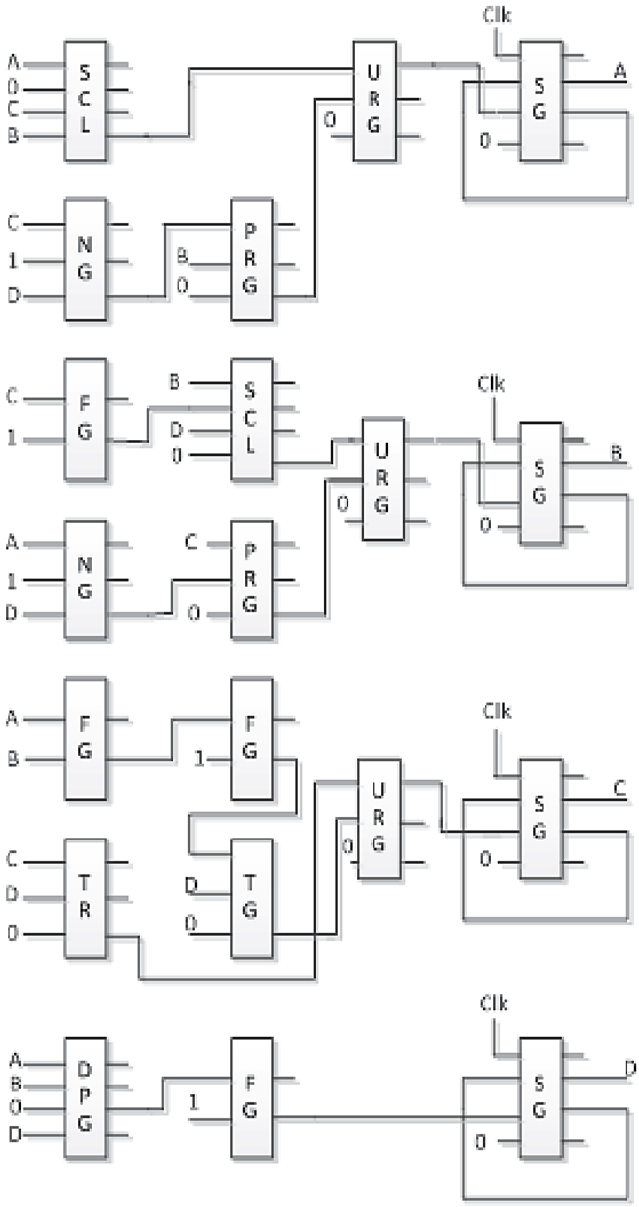


FIGURE.1 BINARY REFLECTED GRAY CODE COUNTER

Uniformly Balanced Gray Code Counter: Gray codes with the interesting property that the number of state transitions per bit is more uniformly distributed among the bit positions. For 4-bit UBGC each bit changes state exactly four times. The sequence of UBGC in the lexicographical order is tabulated in Table 1

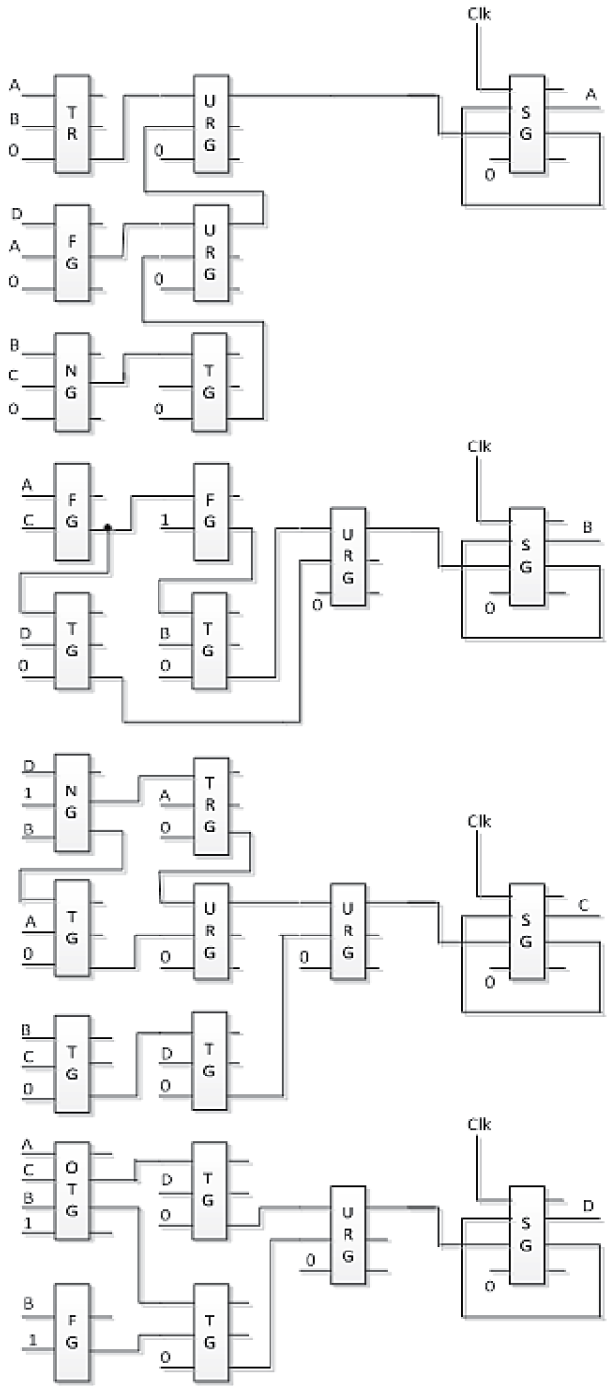


FIGURE.2 UNIFORMLY BALANCED GRAY CODE COUNTER

Antipodal Gray Code Counter: An n-bit Antipodal Gray Codes have the additional property that the binary complement of any code string appears exactly n steps away in the list. Thus, the spatial frequency of the antipodal Gray code-pattern is similar along frames. The code is as shown in Table 1.

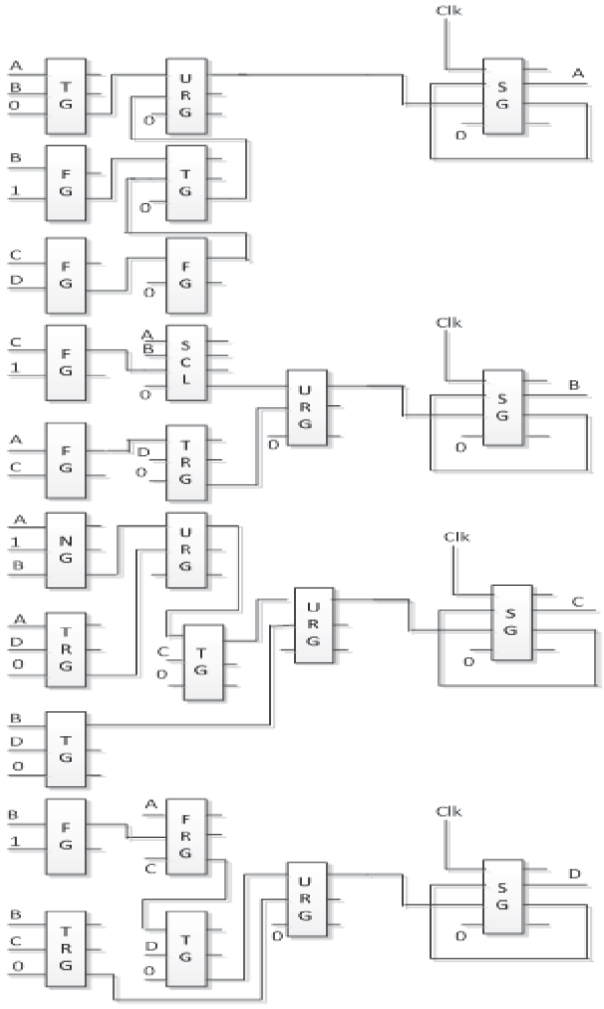


FIGURE.3 ANTIPODAL GRAY CODE COUNTER

V. CONCLUSION

Gray Code counters are unit distance counters since it has only one bit change. Gray code counters can be used for asynchronous circuits to lower power consumption. They reduce the digital noise as compared to the normal counters. They also find application in data path synchronization. They are widely used to facilitate error correction in digital communication such as digital terrestrial television and some cable TV systems. This paper gives a comparative study of Gray code variants namely Binary reflected code counter, uniformly balanced code counter and Antipodal Gray code counter.

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FPGA Implementation of Multibit Flip-Flop Using Mesochrnous Technique

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Abstract— More relaxed clocking techniques such as mesochronous clocking replace completely sync clocking to enhance system composability and simplify timing closure. Under this regime, the modules on two ends of the mesokronous interface get the same clock signal, which works at the same clock frequency, but an unknown phase relationship might occur on the margins of the arrival clock signals. Clock synchronisation is required if data is sent across modules. In this short we introduce a unique mesochron first-input dual-clock first-output buffer (FIFO), which can manage clock synchronisation and temporary data storage, syncing data implicitly through explicit flow control synchronisation alone. Even if the transmitter and receiver are separated by a lengthy connection whereby delay cannot fit inside the intended operating frequency, the suggested system can function well. In such cases, the suggested mesochronous FIFO may be modified to accommodate delays with multi-cycle connections modularly and with little changes to the baseline design. The novel architecture is shown to produce a much-reduced cost implementation compared to prior state-of-the-art mesochronous FIFO architectures.

I. INTRODUCTION

The main development architecture in the field of rapid computer interfaces is Multiprocessor System-on-Chips (MPSoC). The evolution of new technologies has brought forth the necessity for MPSoC. However, the computer overhead and energy requirements have resulted in its optimization required for such a sophisticated design. The designers are dealing with this problem in two ways, by adapting the design to the application limit[1] and by scaling the operation to a restricted voltage / frequency operation[2,3]. Whereas adaptation is an optimum technique, the overall design is substantially high [4]. The design technique comprises monitoring the communications protocol and signal interface between different components [5] in the processor unit while optimising the overhead power and processing. The variety of the design units and the components utilised in this design are also a key restriction in the MPSoC optimization process[6]. The optimization restrictions also limit the operating frequency and system performance[7] in certain applications. This is why the design approach is described with an internal clock allocation updating process[8] and a FIFO-based technique for synchronisation across many units in sub unit activities. Here each core unit is linked to synchronise data exchange across various core units[9]. Each of the IP core processor blocks employs a FIFO dual clock design. However, if all IP blocks are using a dual-clock FIFO design for one common purpose, the resource is more at risk than the provision, because the configuration of all IP interfaces must be conservative, as the speed and throughput of each IP core is different[10]. For example, the buffering of this synchronisation parameter should be modified for a worst-case scenario based on the comparison between source and receiver frequency [11]. Furthermore, the descriptive existence of frequency ratio information (such as the interconnection of a chip operates at a quicker rate than the interconnected IP units) together with performance restriction information can lead to twin high impact specializations[12]. Therefore, the FIFO dual clock design has a wide area and power conservation at last. Different uses are given in [12-17]. Since the designs do not employ clocks, the synchronisation process is difficult to accept between two clock variations[18]. The delay factor in the clock system is ignored while synchronising the various core units. This restricts the synchronisation in this way. Recent advancements show that the delay factor in MPSoC architecture is minimised. The lag due to resource allocation is not overcome at the time of the processing. Here each instruction process has a delay in processing the clock; clock delays must be assigned and the transition to that assignment results in the system processing delays. A novel latency monitoring technique is given in this article by providing the enhanced clock library function. This technique minimises the interchange of data and the delay in instruction and overcomes the overhead latency during instruction. This document is described in 6 sections to present the paper. Section 2 outlines the MPSoC design approach to library coding. Section 3 describes the recommended technique for library code for Mesochronous operations to measure latency. Section 4 showed the results of the simulation for the strategy devised and the conclusion offered in section 5.

II. DISTRIBUTION OPERATION IN VA-MPSOC

CoreVA-MPSoC shows the target application for an integrated and energy-efficient hierarchical interconnect architecture. In this CPU cluster, multiple core CPUs in the cluster that share a comparable address space in the core are connected nicely. Every CPU may read and write local data

from other CPUs through a bus-based interconnection at its original design. The CPU is connected to a cluster interconnection using a FIFO buffer to prevent cycles of penalty operations. The topology of the standard data bus width is specified when the processing unit is designed. For example, Advanced Bus Architecture Microcontroller (AMBA) utilises an AXI4 Interconnect Standard 32 bit or 64 bit data bus width. For particular addresses, AXI4 defines address and data transmission. In addition, distinct channels for reading and writing enable simultaneous read/write (R/W) bus requests. Steps can be added for the connection registration to simplify the compensation for space and route time, increasing the frequency to a maximum of MPSoC clocks. Here, the architecture does not allow the best read requests as it does not work for all cores in the sequence of execution. The CPU boasts the lowest 4-clock operating cycle CPU latency. For Share Bus implementing a total of five intermediaries (1 per channel) are required and for each operation (read/write) two intermediaries are required for crossbar linkages. The Network Interface (NI) interface is formed during the two CPUs connection via the Network-on-Chip (NoC) interface. Each CPU cluster is placed in a 2D structure via a separate X and Y coordinate index. For all cluster memory and units, a common address space is employed in the cluster. NI bridge-based communication during the interchange of CPU clusters and packets via interconnections with routers. As such, it offers the flow control capable of decreasing the operating duration of the CPU for this contact in the CPU core. In order to do so, packet data is saved and retrieved from all local memory of the CPU directly. CPUs therefore take use of local memory access delays. NI also functions as a DMA controller through the distribution of parallel data to the CPU. NI is connected to the cluster in the original setup through a master and a slave port. Packets may be routed to various R/W separation channels. Where the AXI master port of NI can be sent whilst writing data at the same time.

In the exchange of schedules for different CPU interfaces an effective communication strategy is necessary. CoreVA-MPSOC[19] employs a communications paradigm with a single communication channel integration. This method offers more scalability and efficiency than common memory ideas, which can interrupt memory accesses. In general, one job reads and writes on one or more output channels from one or more input channels. Each channel controls the data storage of one or more R/W. Synchronization is regulated by granularity of buffer size. When a channel's buffer requests, the CPU doesn't acquire enough data or no free basic buffer may be written.

However, since data is received via a channel, any memory location in that buffer is accessed by random application. Moreover, no additional synchronisation is required. When the work has been completed, the CPU communicates with the other units in order to exchange the status and reuse the registry. The pooling of resources therefore minimises the overhead. The allocation delay is nonetheless significant. The delay due to resource allocation and sync is also significant, as time delay computation is restricted to the data interface between various CPU units utilising the NoC interface. The NoC operates as a bus arbitrator as a data exchange routing bus. This exchange shows a substantial delay that leads to a reduction in processing speed. Therefore, the time limit, which is focused on in this article, must be decreased. A novel delay mapping technique employing the time stamp library is presented to produce a quicker clock allocation during the syncing procedure.

III. MESOCHRONOUS CLOCK VIRTUALIZATION IN MPSOC (VR-MPSOC)

A virtual delay calculation unit is provided in the suggested method to the virtualisation of the MPSoC operation. This suggested technique changes the current MPSoC design for each core unit with a library unit; for each operating instruction of the processor unit, the library Unit is specified by a pre-computed delay parameter. The instructions for a multi-core processing unit are referenced in this design approach where instructions are classified as 1, 2 or 3 byte instructions. Every operation is conducted here as a direct addressing operation or a direct addressing operation or two indirect addressing operations. The clock delay is calculated for each of these types. The time calculation is calculated as an aggregate delay of the physical delay due to the manufacture of the device and the total delay in the set-up and the time for data is maintained. Each delay is calculated for each type of instruction and set as a library for each core unit. This delay input procedure is conducted throughout the design process as the processing instructions of a design processor are constant and the delay parameter is constant for each instruction. Each instruction is processed to complete delay computing and a matching delay in the library function is set for each instruction. Each library is stored in the core unit as a synchronisation table. This library unit is mapped with the processing instructions during operational stage and the delay is mapped to the arbiter unit. The arbiter is specified at the MPSoCNoC interface that performs the bus arbitration procedure. Each bus line is allocated on the basis of the core bus request from the core unit. In this method of allocation, the delay of the mapped instructions is applied for each allocation. This minimises the extra calculation delay and reduces latency in MPSoC operation. The suggested approach's latency parameter is the accumulated delay owing to clock allocation and calculation delay. In each execution of the instructions, the data or instruction takes an instruction/data buffering time to synchronise the process. Each unit is processed for a delay value according to the instruction type. As the added latency corresponds to the entire delay from allocation to calculation, and the time delay for the clock to sync and the delay is high. In addition to the processing delay, the bus allocation and the data exchange also observes a route delay. Where attempts are made to decrease the road delay by appropriate architectural floor layout, the delay is substantial during operation. The main element of switching and calculation is eliminated by the

library unit to overcome this delay. This is a virtual implementation of a time stamp unit that returns the appropriate delay value during operation. This leads to virtual MPSoC design being developed called 'Vr-MPSoC' units. The technique proposed is described in the following algorithm.

Algorithm (Clock switch virtualization)

Process Initialize:

Step 1: *define the cluster of CPU*

Step 2: *allocate the arbiter for data and instruction*

Step 3: *allocate the operation instruction for each CPU*

Process read:

Step 1: *generate a read offset signal to library latency*

Step 2: *recover the time stamp for each instruction*

Step 3: *record the delay to offset library*

Processes execute:

Step 1: *Read instruction*

Step 2: *Decode instruction type*

Step 3: *Read offset value*

Step 4: *Allocate to data and instruction register*

Step 5: *Read data*

Step 6: *Execute instruction*

Step 7: *Write back*

End

The operational block diagram for the proposed approach is presented in Fig. 1 below.

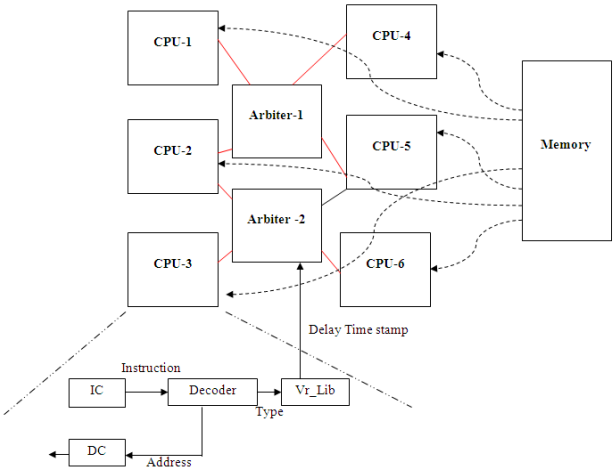


Fig. 1: System Architecture for the proposed MPSoC interface

The processor unit is handled in two operational phases, in which the update phase Phase-1 is performed when each of the decoded commands is mapped to the library unit. The arbiter is assigned a delay stamp for each type of instruction decoded, which internally assigns the delay value dependent on the clock cycle during execution. The procedure of computation and allocation is removed and the arbitration process is carried out on the basis of the scalar time delay value. This leads to a low system latency.

IV. SIMULATION RESULTS

This suggested work is validated in three stages of simulation, whereby the operational functionality of the proposed method is assessed for the scheduling of the proposed task. The allocation and operating overhead delay is calculated. The suggested technique is validated at the second level of implementation using the Xilinx ISE synthesiser for the FPGA device. This result shows the processing speed, area, latency and system performance. The final portion of the simulation result is analysed for the various instructional densities.

A) Operational verification functional

For time monitoring, the HDL description of the simulated particular job was generated in the Aldec tool. The created design is focused at Xilinix FPGA devices in order to implement the proposed method. Measurements are assessed for power, latency, throughput, and area. The results are shown below. Fig. 2 shows the set of instructions utilised to validate the proposed work. This technique works differently by using the instruction buffer set in the core CPU as the instruction cache. The processing instructions for each core unit are used to buffer the data collected from the main memory.

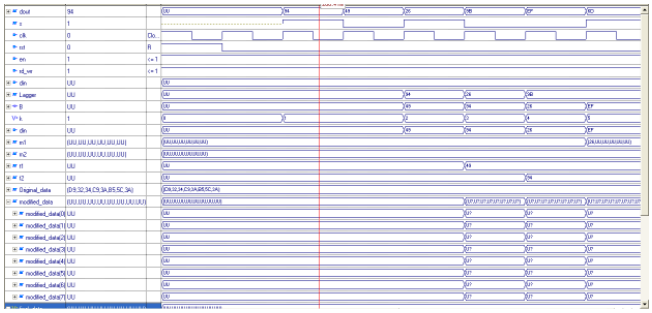


Fig. 2: Operational instruction used for testing

In the test process, each of the instruction is passed to the arbiter unit, where the instructions are mapped with the delay constraint as illustrated in Fig. 3.

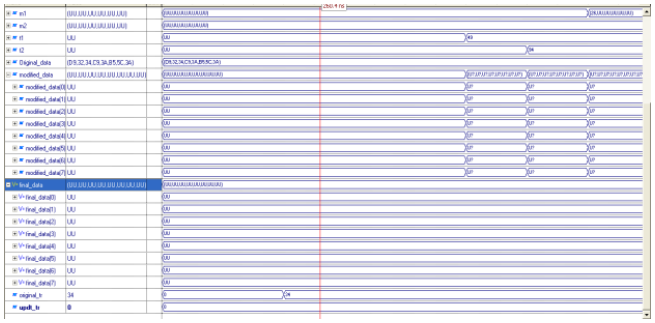


Fig. 3: Mapped instruction of delay metric at arbiter unit

The mapped clock pulse results in the creation of a new data, which is decoded in the arbiter as a delay instruction. Each register is assigned with the input and output clock delay value in the processing unit during execution. The mapped clock pulse results in a new data generated for each instruction and decoded as a delay instruction placed on the arbiter. Each processor unit is immediately allocated during processing when conducting an execution reading. The delay mapping and allocation procedure is shown in Fig. 4.

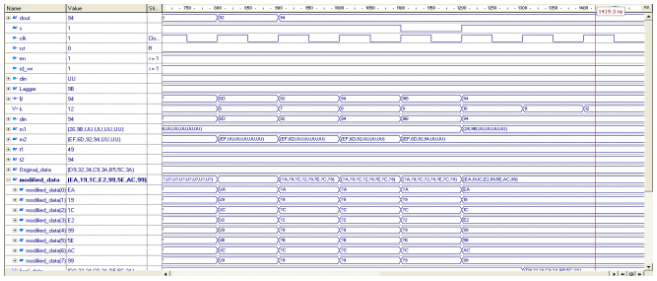


Fig. 4: Delay instruction allocation at arbiter unit

In the process of instruction execution for a 4 set of instruction, the latency for the proposed approach is observed to be 49 compared to 54 for VA-MPSoC design. The observation is illustrated in Fig. 5 below.

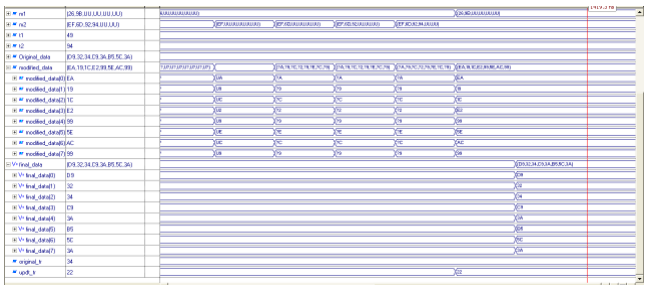


Fig. 5: Latency measurement for the developed system

B) Implementation result

The implementation of the developed approach is targeted to Xilinx FPGA device for a Spartan family. The implementation report obtained is presented in Fig. 6.

TRB Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	113	88,192	1%	
Number of 4 input LUTs	123	88,192	1%	
Logic Distribution				
Number of occupied Slices	134	44,096	1%	
Number of Slices containing only related logic	134	134	100%	
Number of Slices containing unrelated logic	0	134	0%	
Total Number of 4 input LUTs	261	88,192	1%	
Number used as logic	123			
Number used as a route-thru	138			
Number of bonded IOBs	34	1,164	2%	
IOB Flip Flops	14			
Number of PPC405s	0	2	0%	
Number of GCLKs	1	16	6%	
Number of GTs	0	20	0%	
Number of GT10s	0	0	0%	
Total equivalent gate count for design	2,633			
Additional JTAG gate count for IOBs	1,632			

Synthesis Report

Fig.6: Report of Xilinx FPGA implementation for the developed system

A Power Analysis of the implemented design is computed using X-power analyzer of Xilinx tool. A power rating of 181mW of power rating is obtained.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		181

Vccint 1.50V:	85	128
Vccaux 2.50V:	20	50
Vcco25 2.50V:	2	4

Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0

Quiescent Vccint 1.50V:	85	128
Quiescent Vccaux 2.50V:	20	50
Quiescent Vcco25 2.50V:	2	4

Fig. 7: X-power report for developed system

The timing report for the developed system illustrated a maximum operating frequency of 129.98MHz with a time period of 7.6ns. The device has a setup delay of 2.9ns and a hold delay of 3.6ns. The placement of the logical design with routing and area coverage is observed using Xilinx-route and place operation. The Interconnection

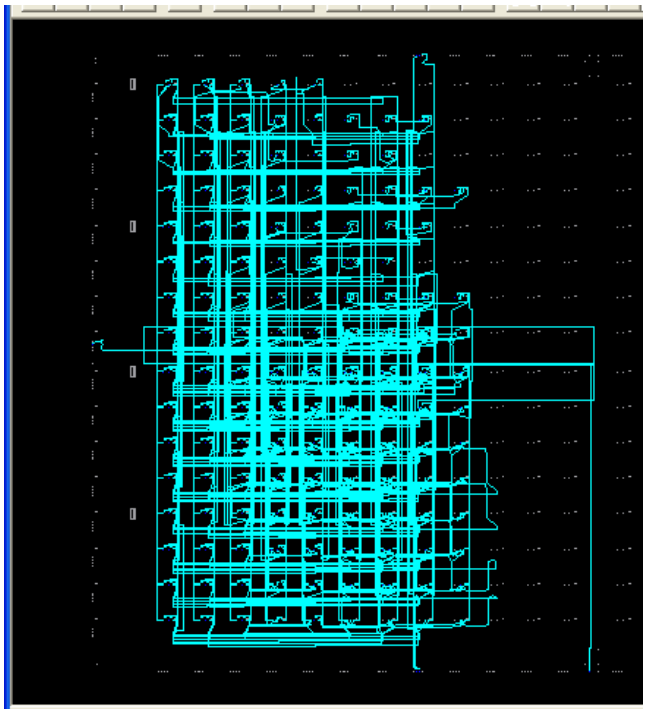


Fig. 8: Logical interconnect of CLB in targeted FPGA device

The logical placement of CLB unit is shown in Fig. 9.

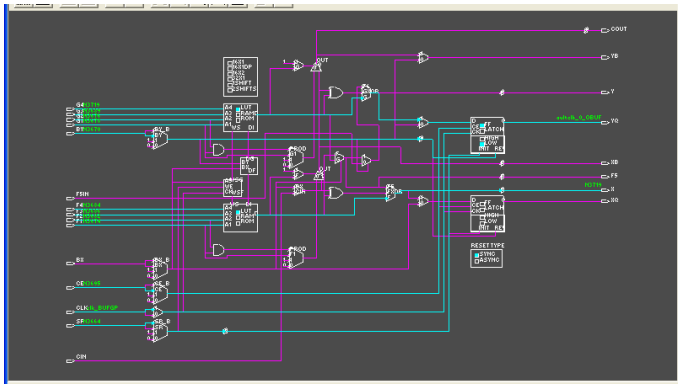


Fig. 9: Logical Placement of CLB unit

The pin layout for the targeted design is shown in Fig. 10. This implementation has dedicated lines of 12 IO lines with Vcc and ground pins as seen in Fig. 10.

The blue encircled are the allocated line here,

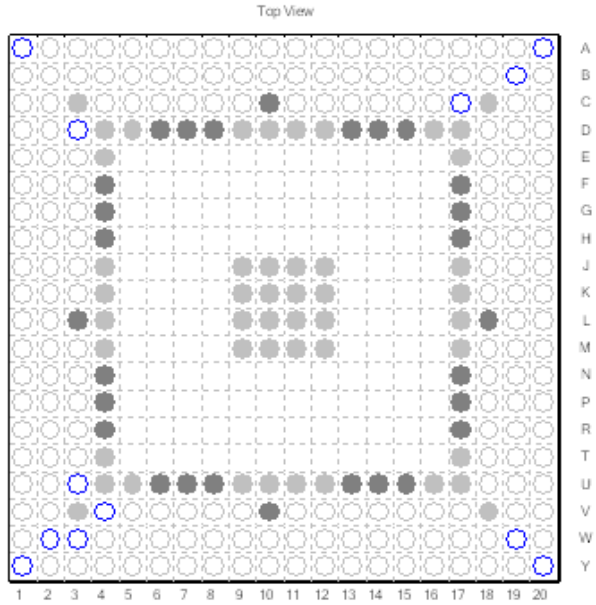


Fig. 10: Pin layout of the implemented design for the targeted FPGA

C) Analysis of developed approach

In the validation of operation performance power measure is critical. The power consumed in a processor unit is defined by,

(1)

Where is the capacitance, is the voltage, and is the operating frequency for a set of instruction executed. Here the power is defined as a function of device parameter and the operating frequency of the processing unit. Here, more the operation frequency is more the unit is enabling giving more dissipation of power. However, for reduced computations the operational iteration are reduced which leads to less number of operational cycles and hence reducing the power consumption. The analysis of the power utilization is presented in table 1 below.

Table 1: Observation for power utilization

Instruction density	Power (*mW*)	
	VA-MPSoC [19]	Vr-MPSoC
4	131.5	114.2
5	274.5	182.8
7	321.4	281.3
9	388.7	311.4
12	451.6	411.3

The comparison of power utilization for different instruction density is shown in Fig. 11

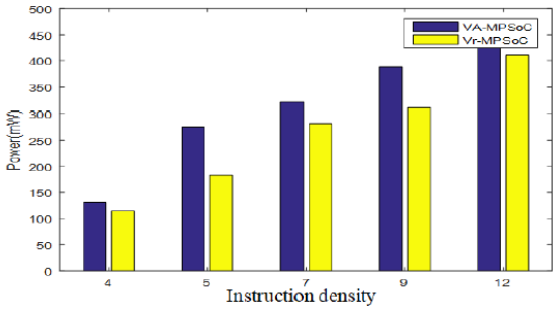


Fig. 11: Comparison of power utilization for different instruction density

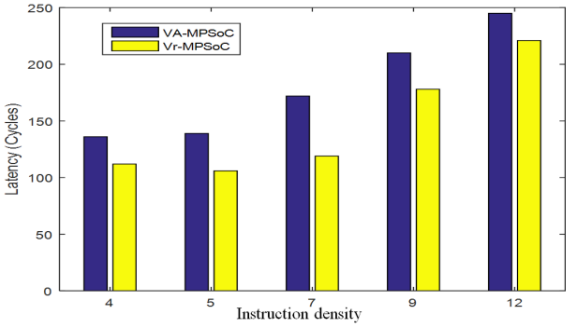
The power consumption is proportionately high for wide selection of instructional systems, however owing to low time computing cycles, the consumption is comparably smaller in the Vr-MPSoC architecture.

Latency is the number of calculation cycles used in a procedure. Table 2 below summarises the observed delay of the technique proposed.

Table 2: Latency observation for the developed approach

Instruction density	Latency (Cycles)	
	VA-MPSoC [19]	Vr-MPSoC
4	136	112
5	139	106
7	172	119
9	210	178
12	245	221

The comparison of latency for different instruction density is shown in Fig. 12



The system performance for a device design is validated by the efficiency of number of processing block per cycle

which is termed as throughput. The throughput of a digital system is defined by,

$$THR = \frac{Fmax \times Bsize}{LAT} \qquad (2)$$

Where, and LAT are the maximum operating frequency, block size and latency measured.

Table 3: Throughput observation

Instruction density	Throughput	
	VA-MPSoC [19]	Vr-MPSoC
4	196.4	212.3
5	226.1	272.7
7	270.2	321.1
9	321.4	342.4
12	387.1	396.2

The comparison of the processing throughput for different instruction density is shown in Fig. 13

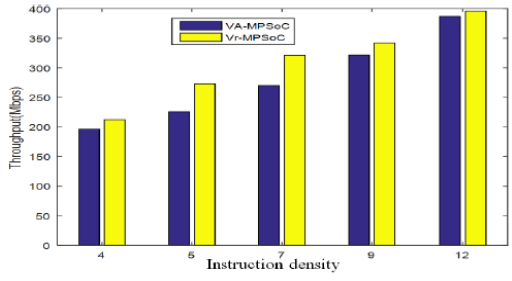


Fig. 13: Comparison of the processing throughput for different instruction density

V. CONCLUSION

This study introduced a novel technique to the mapping of chip multiprocessor system architecture (MPSoC). The distributed computing offers the benefit of quicker operation, but its functional performance is constrained by delays in resource allocation. In order to achieve optimum operating performance in spreading processing units, a novel clock time allocation virtualization with library mapping is introduced in the MPSoC architecture. The above technique significantly improves latency reduction and hence decreases electricity usage. This performance shows an increase in the system processing performance.

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Realization of Speed Optimized VLSI Architecture of Multistage Linear Feedback Shift Register Counters Decoding Logic

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Abstract— When compared to standard binary counters, it has been discovered that linear-feedback shift register counters are ideally suited to applications needing huge arrays of counters that can improve both area of the design and performance. However, decoding the count order into binary necessitates a lot of processing, making system-on-chip designs impossible. A counter made up of many LFSR stagesis presented in this study using carry look ahead adder for high frequency applications that keep the advantages of a one-stage LFSR while only requiring decoding Circuitry that scales logarithmically with the number of stages instead of exponentially with the number of bits like other circuitry does.

I. INTRODUCTION

Recent improvements in applications like single-photon microscopy identification have made the use of a large number of arrayed counters is requiredin a compact space.Time-of-flight (TOF) cameras are among themrun inside and outside and require counters to tally clock cycles, as well as photon-checking photon counters are cameras that count the number of photonsin a span.

Because each camera pixel has a distinctive counter, reducing the amount of space in these applications, the amount of energy spent by the counter is crucial for increasing the number of pixels in the cameras.Although linear feedback shift

registers (LFSRs) are commonly used as pseudorandom number generators, they can also be used for other purposes, they have likewise been ended up being a viable method to make synchronous counters and are undeniably fit to huge displayed frameworks because of the shift register's sequential understanding technique.In Single-photon detection arrays and CMOS pixel design, LFSR counters have been used.

An LFSR's clock speed is independent of the counter's amount of bits, and except for zero states, all states in the state space are traversed.Because the count order of the LFSR is pseudorandom, to transform the LFSR state to binary order, more processing is required.The LFSR sequence must be decoded into binary, the direct lookup table (LUT) methodology, as well as the iteration technique, and a tradeoff technique for time and memory are all compared.

The iteration method repeats the count sequence of the LFSR indefinitely, comparing each to the counter value. On average, this needs around 2n1 comparisons for an n-bit LFSRthe direct LUT technique, on the other hand, uses a n LUT to directly decode the LFSR state.2(N/2) LFSR count values are stored in a table, iterate the LFSR sequence until the count value matches one of the table values, the time-memory tradeoff technique proposed in integrates both methods.

To get the decoded value, subtract the number of iterations from the stored value.For usage with ring generator event counts in, a logarithms-based approach was introduced and developed.

Decoding for further processing is required for large array applications, so transform each cell in the array to binary order, and this decoding must be done on the chip for system-on-chip architectures. Because multiple conversions must be performed, the decoding logic must be integrable and fast to meet this need.However, with the size of the LFSR, in terms of time or area, all of the aforementioned approaches develop exponentially.There are various instances of arrayed designs for single-photon detection applications that would be impossible to accomplish with LFSR counters that don't require exorbitantly large integrated LUTs.

This project is designed with a new counter architecture based on numerous LFSR stages that can be decrypted using logic that grows logarithmically, rather than exponentially, as counter size increases. While a simple concatenation of LFSR counters, like binary ripple counters, would result in a large performance loss, this study presents a strategy for distributing the ripple signal in time and compensating for it in a generalized decoding logic scheme.For the rest of this paper, an n-bit LFSR will be referred to as an n-LFSR.

II. LETERATURE SURVEY

For the last four decades, astounding advances in Silicon devices and circuits, as well as very dependable mass manufacturing techniques, have sparked extraordinary revolutions in electronics, to the point that electronics is increasingly pervading many facets of our lives. V Modern

electronic systems' complexity and competitiveness necessitate optimization across various disciplines.

*For high-performance systems, joint optimization of device, circuit, packaging, and test is becoming increasingly crucial.In complex systems, design for manufacturing and testing is becoming more important, but it is also becoming more difficult.*Vornicu,

R. Carmona-Galán, and A. Rodrguez-Vázquez presented "A single photon image sensor with a CMOS 0.18 m 6464 pixel and pixel 11 b time to digital converter," when compared to conventional binary counters, counters with linear-feedback shift registers (LFSRs) have been found to be well suited to a variety of applicationsrequire a huge number of counters and improving space and performance.

However, decoding the count order into binary necessitates a lot of processing, making system-on-chip designs impossible.This study proposes a counter made up of several advantages of a single-stage LFSR stage are preservedwhile only requiring decoding circuitry that grows logarithmically rather than exponentially considering the amount of bits and the number of phases as other techniques do.

III. REGISTER COUNTERS WITH REDUCED DECODING LOGIC USING MULTISTAGE LINEAR FEEDBACK SHIFT

A) Multistage LFSR Counter

Figure 1 depicts the counter's overall design scheme. An enable signal controls M a set of n-LFSR blocks that are all the same.The enable signal is asserted when the (m 1)thn-LFSR experiences a needed state change, leading the n-LFSR to advance one state in the mth state.This allows you to traverse the whole M n bit state space.In large arrayed designs, the counter can also be employed as a high-speed serial readout chain.

The LFSR's feedback and ripple-carry blocks are avoided, and this is accomplished with minimal additional circuitry.The multistage counter technique divides dividing the counter into M separate segments, allowing a n bit LUT to decode each n-LFSR individually rather than a (Mn) bit LUT.For small n, a LUT can be easily implemented on a chips

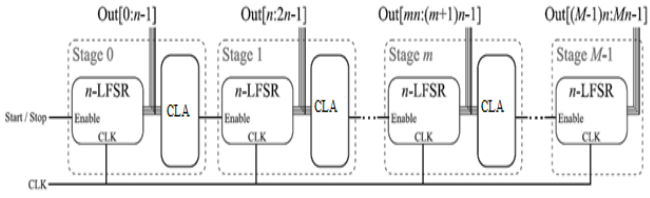

Fig. 1.The multistage LFSR counter is depicted as a block diagram.

B) Carry Look Ahead Adder

In computerized logic, a fast adder, now and then known as a carry look-ahead adder (CLA), is a kind of adder. A carry look aheadadder the time it takes to distinguish adder bits, which improves execution. It's not equivalent to the ripplecarry adder (RCA), it figures the convey bit close by the total bits and requires each progression to stand by until the past adder bit is resolved prior to computing its own total bit and carry bits.

The carry look ahead adderbefore the aggregate, the adder figures at least one carry bits, which limits the time it takes to compute the bigger worth bits of the adders outcome.

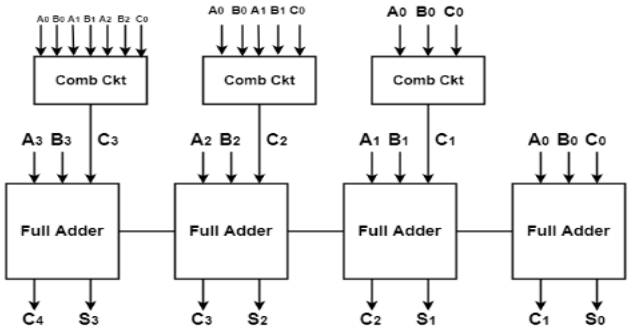

Fig 2:carry look ahead adder with 4 bits

C) LFSR Block snip

Lost LFSR states will result in large blocks of counter states being missing from the counter state space because the counter is triggered once for each stage during each period of the preceding stage.As a result, an n-LFSR be constructed for maximum length.Because an n-maximum LFSR's sequence length is only 2n 1, further logic is required to include the missing state in the count sequence.When the 0x000...1 condition is recognized, as demonstrated in Figure 2, a NOR and XOR function can be employed to stop the feedback mechanism.

This logic extends the length of the individual component LFSRs' sequences to 2n allowing the counter to cover each and every state in the space of 2Mn states.This permits a multistage counter that can be utilized in a variety of applications where all states must be covered, self-starting counters, where regular LFSRs are ineffective. Dotted components in an n-LFSR block with logic for sequence extension.A single logic block is used to implement the complete feedback block.

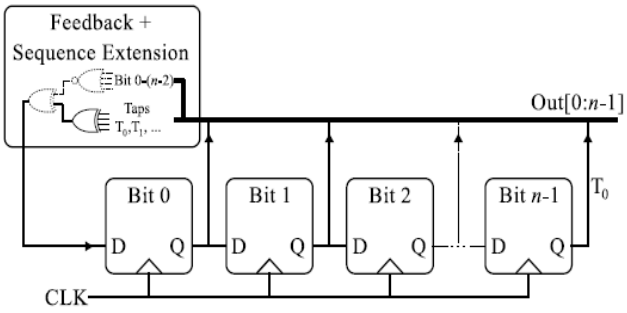

Fig 3: Structure of a proposed multistage

Fibonacci and Galois LFSRs, as well as ring generators, are examples of many-to-one and one-to-many LFSRs are all examples of LFSR feedback.Figure (a) shows ring generators and these are widely seen to be the best approach to design an LFSR, there are subloops formed by the shift register forming a ring and the taps within the ring.

The sequence-extension is a term that refers to the process of extendingon the other hand, necessitates additional logic in the LFSR, which rules the basic way Instead, for logic minimization utilizing a 4bit conventional LFSR, LFSRs with a many-to-one ratio Fig (b),as shown in Figure 3, the feedback logic and the sequence-extension logic are merged into a single logic block..

Allows for a multistage counter for greater flexibility in n-LFSR size selection, compact single-tap LFSRs are preferred.A many-to-one LFSR with a single tap and the accompanying ring generator are topologically indistinguishable.The decoding logic must process the highlighted states further.

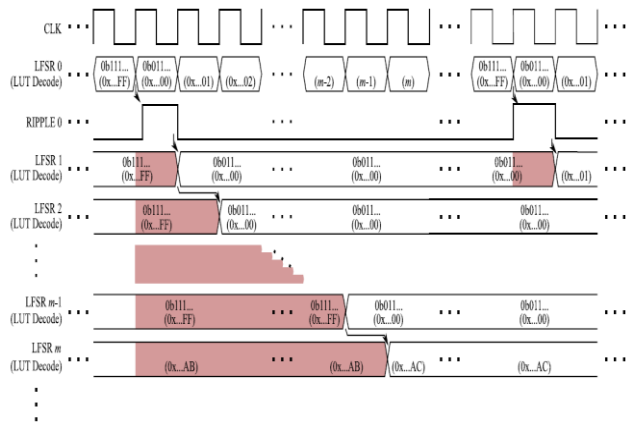

Fig. 4.The multistage LFSR counter's operation is depicted in a timing diagram. The carry look ahead logic is depicted with arrows.

D). Decoding Logic

On the output of the multistage LFSR counter array, the decoding logic functions as a post processing step.Each LFSR value is passed through a LUT as it is read from the array. The LUT corrects most states to binary order, as seen in Fig. 4.To fix the problems produced by the delayed transition, however, more logic is required.Initial and overflow errors are the two sorts of LUT decoding problems that might occur.Before the mth stage switches, the counter is suspended on the clock cycle, the states at the top of the scale of the triangle of transitional errorproduce initial errors.

The number of cycles in a clocksince the commencement of theedge of transition is also thevalue of the previous phases has been decoded.Because the mth step takes m clock cycles to reach the ripple, these faults can be identified if the previous stages' decoded values are equal to m1.When there is an error in the previous stage and the current stage is equivalent to 0x...FF, overflow errors occur.These faults suggest that a prior step should have resulted in a ripple event sooner in the clock cycle.

Figure 5 depicts the logic decoding that discovers and corrects these problems.Each stage's error detection is based on the preceding stage's decoded value, hence each step is evaluated in order.If the following step detects an incorrect circumstance, the invalid register is set for the next stage, causing the fault to be corrected on the following clock cycle. Because the inaccuracies are always a fraction of a percent below the actual value,the next stage is incorrect, as it either adds a LUT or outputs one. On the off chance that the current stage is an error and furthermore 0x... FF, an overflow error will occur in the next step.When the incrementer carryout is ANDed in the next stage an invalid register is discovered.

By comparing previously decoded stages and putting them in latches, them to a stage counter that keeps track of the number of stages that is currently in use, initial errors can be discovered.The next stage will have an initial mistake if the stage is currently the same as the value previously decoded the counter simply has to count up to a certain number.

M, hence,y = _log2(M)_ bits are required.As a result, only a y-bit comparison between the prior state of decoding and the counter is required, and Z = y/nstages must be stored.

To confirm that the comparison is legitimate, to verify that all other bits in the previously decoded value are zero, the zeros register is employed.The zero point of the counter is in an erroneous state (0x....00). If all of the counter phases have been resetto zero, the first count values will be wrongly decoded.However, because it is not an error if the end state (0b1111...) is reached. condition, after one clock cycle, the counter will properly transition to zeroif it is reset to this state instead.

The final count value will be a one-time occurrence, but if necessary, this can be adjusted by increasing the final count amount by one.The time it takes to decode the count value is proportional to M and n. Each stage of the counter takes one clock cycle to decode, as a result, to decode the complete count value, M clock cycles are required.The decoding circuitry's critical path differs depending on the implementation, but it may involve for huge n, the LUT, the incrementer, and the comparison to the stage counter all perform poorly.

As a result, for bigger n values, the maximum clock rate will be lower, however for a counter of the same size but with a larger n value, more stages will be required, decoding the counter with fewer clock cycles.The logic decoding can be implemented as a pipeline in the readout chain if the array is read out serially. The entire array reading will be delayed by M clock cycles, individual counter values will be read out with a decoded value.

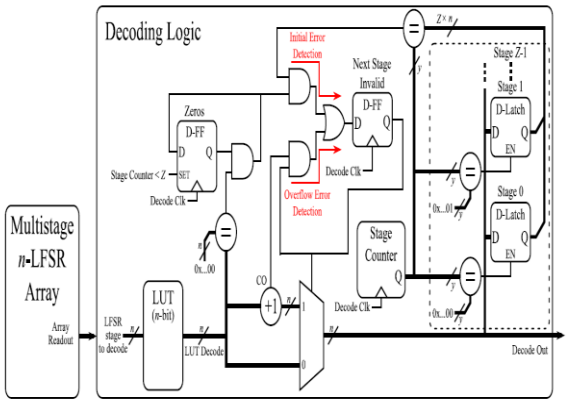

Fig.5. Logic for decoding the binary representation of the LFSR counter state order with multiple stages. Each stage is decoded one at a time in the correct order.

IV. RESULTS

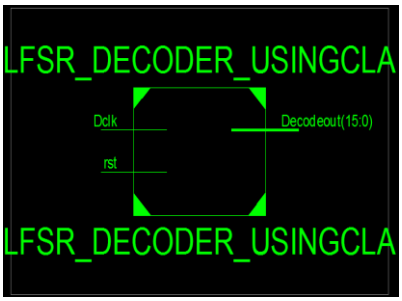

Fig 6: RTL schematic of proposed design using carry look ahead adder

RTL Schematic: The RTL schematic, also known as the register transfer level, denotes the architecture's blue print and is used to compare the designed architecture to the ideal architecture that we are working on.The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e, verilog,vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing. The figure represented below shows the RTL schematic diagram of the designed architecture

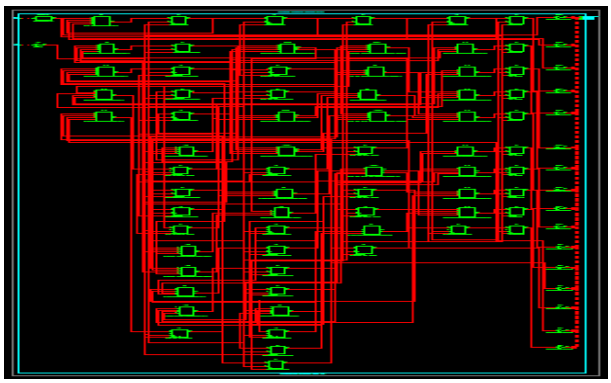

Fig7: View technology Schematic view using carry look ahead adder

TECHNOLOGY SCHEMATIC:-The architecture is represented in the LUT format by the technology schematic, the LUT is an area parameter that is used in VLSI to estimate the architecture design.The LUT is a square unit, and the FPGA's LUTs mirror the code's memory allocation.

Fig8 : simulated wave forms of proposed design using carry look ahead adder

The simulation is the method that is used to verify the system's functionality, whereas the schematic is used to verify the connections and blocks. Switching from implantation to simulation on the tool's home screen opens the simulation window, and the simulation window limits the output to wave forms. It has the flexibility of provisos in this case.

Parameter	LFSR DECODER USING CSLA	LFSR DECODER USING CLA
Frequency (M Hz)	175.841	238.555

Table 1: frequency comparison table

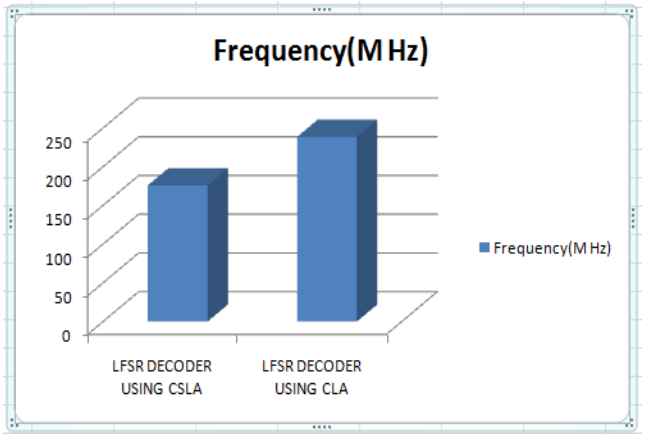

Fig9: frequency comparison bar graph

V. CONCLUSION

This study describes a generalized design and realistic implementation of LFSR counters with many stages and logic decoding in VLSI technology.The proposed counter is made up of a large look ahead adder and many smaller LFSR stages are activated by the previous stage's state

transition.Instead of the LUT to scale to the counter's size, for any number of stages, this architecture allows the decoding circuitry to be implemented on a fixed sized LUT.

Traditional LFSR decoding systems demand rather than scaling exponentially witexponentially as the number of bits increases h the number of bits, decoding logic scales linearly.A considerable amount of upsides of LFSR counters are held in the multistage LFSR counter, for instance, great execution paying little heed to the quantity of bits in the counter for an unassuming measure of additional logic.The suggested multistage LFSR, which can give LFSR counters with both performance and frequency benefits, any functionthat necessitates the use of a set of event counters will profit from this.

VI. FUTURE SCOPE

In future multistage linear feedback shift registers have wide rangeof applications,these lfsrs will be useful at built in self-testmethodologies (BIST).this kind array structures will be useful large number of bit designs. It will be extend up to 32bit,64bitand so on. these random numbers designs will be used in applications of counterbased designs.multistage linear feedback shift registers will be used in one time password (OTP) generations also..

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Quantile Regression Model for Handling Outliers in Time Series Data

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Abstract— Time Series forecasting comprises techniques for predicting future values based on previously observed values . Prediction results of time series data might be compromised due to outliers in the dataset. Handling outliers is very essential in real scenario in order to provide accurate prediction results. In this paper, we have compared experimentally well-known linear regression technique with quantile regression technique in order to check the capability of outlier handling. The results of experiments proved that quantile regression model excels for handling outliers.

Key Words—Quantile Regression, Linear Regression, Time Series Data, Linear Relationship, Normal Distribution

I. INTRODUCTION

Linear regression technique is widely used in literature for Time series data analysis. It is most simplistic and impressive when relationship between dependent and independent variables is highly known. However, this technique is based on several assumptions:

- It is for linear relationship. It assumes there exists a linear relationship between the dependent variable and independent variables. This technique calculates the best fit that defines relationship between the dependent and independent variables.
- It assumes that linear combination of the variables also has a Normal distribution in nature. It is also known as multivariate normality.
- This assumption exists in multiple regression techniques. Regression technique suffers from little or no Multi collinearity problem. It is states of very high inter correlations or inter-associations among the independent variables. In the regression, it might be possible that no inter-association exist among multiple variables.
- No auto-correlation in regression technique. Auto-correlation is very crucial in time series data analysis. Autocorrelation states the degree of correlation amid the values of the similar variables across diverse observations in the data.
- In regression techniques, noise or random disturbance is the same across all values of independent variables.
- It is based on central tendency value so outliers affect the results of these kind of models.

Quantile regression is an expedient alternative to linear regression that deals with:

- Study of distributional relationships of variables.
- Heteroscedasticity effectively.
- Censored variables.
- Outliers effectively.
- Predicting a certain quantile by minimizing quantile loss.

Machine Learning techniques gaining popularity these days for diverse kind of applications. Time Series Data Analysis is suitable application for Machine Learning. Accurate and unbiased estimation of time series data is not feasible with linear models hence to achieve such kind of results; machine learning techniques play a vital role. Basically, there are four main types of machine learning algorithms exist in literature: Supervised, Unsupervised, Semi-Supervised and Reinforcement Learning. Supervised and Unsupervised both techniques are relevant for time series data analysis. Support Vector Machines, Logistic Regression, Naïve Byes, Decision Trees, K-nearest neighbor, Neural Network are popular machine learning algorithms supervised algorithms that are vital for time series data analysis. Clustering, Anomaly Detection and Neural Network are familiar unsupervised learning algorithms suitable for time series data analysis.

The section-2 of paper will describe related work based on traditional statistical models and quantile regression model. The section-3 will describe the mathematical model of quantile regression. The section-4 will depict the significance of outlier in time series data. The section-5 will discuss the time series dataset used for the experimentation purpose. The section-6 will discuss about experiments and result discussion. At last, the paper will provide the conclusion of the proposed research.

II. RELATED WORK

Literature survey is divided on traditional statistical models and quantile regression based models in context to time series data analysis.

2.1 Traditional statistical models for Time series data analysis

Time is central dimension in many applications. Temporal data not only deals great prospect and benefit, but it also comes with its peculiar set of real-world complications and matters [4,5]. In the book published in 2000, authors [2] depicted the importance of regression analysis in several use cases of time series related data. Time series data of different use cases fit in linear regression model effectively. Simple linear regression plays a vital and dominant role in time series data analysis. In 2010, in the paper [1] authors described the importance of linear regression method for the analysis of medical data. The purpose of this statistical model was to describe relationships between two variables or among several variables. In [3] authors, described tools for assessing quality and reliability of regression estimates. Authors also discussed the presence and intensity of collinear relations among the regression data. Regression analysis is very vital for the time series data analysis, however it suffers from various drawbacks: normal distribution of data, linear relationship only, no multi collinearity, no auto-correlation and based on central tendency values.

Autoregressive Models [8] are another vital category for time series data analysis. These models use linear combination of past values in order to make forecast. They are incredible flexible and modeled a many different types of time series patterns. Autoregressive Integrated Moving Average (ARIMA) model [6,7] is the most popular in this category. However, it is based on two main assumptions (i) Linear time series is required and (ii) Normal Distribution of the data. The most important variant of this model is SARIMA [9]. SARIMA stands for Seasonal Autoregressive Integrated Moving Average. The salient feature of this model is its flexibility for diverse time series in simpler way. However, it required pre-assumption of linear form.

Non-linear stochastic models [6,10,11] are the solutions to overcome the limitations of Autoregressive Models. Several hybrid approaches have been proposed in the literature to deal with the time series data analysis using Artificial Neural Networks [6,12,13]. However, several limitations such as censored variables and outlier dealing are the main concern of the research.

2.2 Quantile Regression Model for Time series data analysis

Quantile regression [14] has received progressively attention in current eons and applied to varied domains. It has numerous advantages over traditional statistical methods. It has been widely applied to independent data and time-to-event data. The scope of the paper is to time-to-event data. Quantile Regression is best to measure the differences of covariates effects at different quantiles of duration time [15]. Various studies have been carried out using QR model for time-to-event data. The authors in [16] have developed a recursively reweighted estimator of the regression quantile process which is direct generalization of the Kaplan-Meier estimator. In [17] authors explored the quantile regression model for interrelated failure data. The authors in [18] developed a new quantile regression approach for survival data subject to conditionally independent censoring. In [19], authors have developed a universal hypothetical and inferential framework for the new counting process model, which amalgamates with an existing method for censored quantile regression. In [20] authors have used quantile regression method for the recurrent gap time data for health domain. They have designed estimation technique that can be straightforwardly applied in present software for univariate censored quantile regression. In [21], the authors have developed the validation procedure for the predictive censored quantile regression model. The performance of procedure was carried out using simulation and authors concluded that censored quantile regression model permits more sensitive analysis to time to event data. In the book [22], authors provided twelve outstanding empirical contributions in economics and stated that quantile regression provides an ensemble of techniques for estimating families of conditional quantile models, thus offering a more complete view of the stochastic relationship among variables. Other interesting applications of Quantile Regression related to clinical, biomedical and health care areas are described in [23,24,25,26].

2.3 Discussion based on Related Work

Based on related work, authors have derived several conclusions:

- Quantile regression is gaining popularity for estimating the quantiles of a distribution conditional on the values of covariates.
- It is the robust technique for dealing with outliers
- It gives a more complete picture of the conditional distribution than a single estimate of the center like traditional regression techniques.
- Quantile regression methods offer a mechanism for estimating models for the conditional median function, and the full range of other conditional quantile functions.
- Quantile regression is capable of providing a more complete statistical analysis of the stochastic relationships among random variables.
- In several machine learning projects, predictions are subject to high uncertainty. The decisions of such projects are driven by output of machine learning project and potential prediction error. The Quantile regression loss function is the solution to tackle such problems by replacing single value prediction by prediction interval.

III. QUNATILE REGRESSION MODEL

Let R be a random variable with cumulative distribution function FR(r) = P(R ≤ r). The n[th] quantile of R is represented by :

$$Q_R(n) = F_R^{-1}(n) \ \inf\{ r : F_R(y) \geq n\} \quad (1)$$

Where r ϵ (0,1)

Specific Quantile is achieved by minimizing the expected loss of R – x with respect any value of x.

$$\min A(pr(R-x) = min\{ (r-1) \int_{-\infty}^{x} (r-x) dF_R(r) + r \int_{x}^{\infty} (r-x) dF_R(r)\} \quad (2)$$

Simplify the above equation-2 and, new equation-3 will be derived

$$0 = (1-r) \int_{-\infty}^{qr} dF_R(r) - r \int_{qr}^{\infty} dF_R(r) \quad (3)$$

More simplification of equation-3 gives the result as equation-4

$$0 = F_R(qr) - r \quad (4)$$

Finally, the equation-4 is simplified as equation-5

$$F_R(qr) = r \quad (5)$$

IV. SIGNIFICANCE OF OUTLIER IN TIME SERIES DATA

Usual time series data comprises of low and high points as selection of data is arbitrarily. Outlier detection and management is crucial as it finds data that are substantially divergent and inconsistent with the majority of the data in dataset [27]. If it is not detected and managed properly in time series data, then the results of forecasting might be compromised. In principle, it is a mapping function that is expressed as equation (6).

$$f(p) \rightarrow q \quad (6)$$

The mapping function determines the score of outlier based on the value p. If the value of p is beyond the threshold value, then it is considered as an outlier. Outlier detection and management is vital for time series data set as in most of series majority of data resides in particular range but few data points are either very low or very high. If authors consider all the data, then the forecasting results might be affected.

V. TIME SERIES DATASET

In this proposed research time series dataset of Covid-19 cases in India is taken as for the experimentation purpose. The data set is taken from the trusted site https://www.covid19india.org. They are using state bulletins and official handles of Chief Minister or Health Ministry to update their data. The data of 239 days are collected from 30[th] January-2020 to 24[th] Septemebr-2020. The structure of the dataset is depicted in Table-1.

Table -1 Structure of Time Series Dataset

Date	Daily Confirmed	Total Confirmed	Daily Recovered	Total Recovered	Daily Deceased	Total Deceased
4-Mar	22	28	0	3	0	0
5-Mar	2	30	0	3	0	0
6-Mar	1	31	0	3	0	0
7-Mar	3	34	0	3	0	0
8-Mar	5	39	0	3	0	0
9-Mar	9	48	0	3	0	0
10-Mar	15	63	1	4	0	0
11-Mar	8	71	0	4	0	0
12-Mar	10	81	0	4	1	1
13-Mar	10	91	6	10	0	1
14-Mar	11	102	0	10	1	2
15-Mar	10	112	3	13	0	2
16-Mar	14	126	1	14	0	2
17-Mar	20	146	1	15	1	3
18-Mar	25	171	0	15	0	3
19-Mar	27	198	5	20	1	4
20-Mar	58	256	3	23	0	4
21-Mar	78	334	0	23	0	4

VI. EXPERIMENTS AND RESULT DISCUSSION

R programming language is used for the experimentation purpose as it provides excellent statistical and machine learning capabilities. Total Deceased are predicted using independent variables Date, Daily Confirmed and Daily Recovered. The quantile regression approach is compared with well-known linear regression model. Table-2 described the summary of dependent variable i.e Total Deceased.

Table-2 Summary of Dependent Variable

Minimum Value	1st Quartile	2nd Quartile	3rd Quartile	Mean	Maximum Value
0	34	4710	33148	19789	91733

Table-3 described the summary of independent variables i.e Daily Confirmed and Daily Recovered

Table-3 Summary of Independent Variable

Independent Variable	Minimum Value	1st Quartile	2nd Quartile	3rd Quartile	Mean	Maximum Value
Daily Confirmed	0	170	7254	49282	24335	97860
Daily Recovered	0	18	3789	33840	19887	102070

The well-known linear regression model is applied on the data set by considering Total Deceased variable as dependent variable and Date, Daily Confirmed and Daily Recovered variables as Independent variables. The Table-4 described the residuals of linear regression model.

Table-4 Residuals of Linear Regression Model

Minimum Value	1st Quartile	2nd Quartile	3rd Quartile	Maximum Value
-11251.0	-326.0	-289.6	780.4	15313.3

The Table-5 depicted the coefficients values of Intercept and independent variables on the basis of linear regression model.

Table-5 Coefficients of Linear Regression Model

Aspect	Estimated Value	Standard Error	t value
Intercept	289.63230	232.41439	1.246
X1	0.25642	0.03133	8.185
X2	0.66673	0.03503	19.033

The result of Table-5 provided estimated value of coefficients intercepts and independent variables. Only one value is derived by considering all the data means it considered all the data and result is generated based on the central tendency value of the data set. Suppose, certain data is not in the range and authors want to generate the results by eliminating those data then it is not possible in the linear regression. In another word, linear regression is based on central tendency value and it does not deal with outliers.

Quantile regression model deals with different quantiles. With the help of this model, authors are able to generate estimated value of different coefficients on the basis of different quantiles. The Table-6 described the estimated value of coefficients based on 19 standard quantiles.

Table-6 Coefficients of Quantile Regression Model

Quantile	Intercept Value	X1	X2
0.05	-134.92543	0.36010	0.40052
0.10	-114.35035	0.37664	0.40286
0.15	-22.50236	0.26308	0.57148
0.20	-9.40376	0.23774	0.62671
0.25	-4.37631	0.24928	0.63706
0.30	-3.12299	0.27544	0.61412
0.35	-1.80406	0.28041	0.61742
0.40	-2.79754	0.31084	0.60335
0.45	-0.58178	0.33351	0.58178
0.50	-0.23749	0.33590	0.58074
0.55	0.00000	0.36865	0.55126
0.60	0.00000	0.38109	0.54006
0.65	0.00000	0.38600	0.54111
0.70	0.00000	0.37733	0.56888
0.75	0.00000	0.38452	0.57810
0.80	0.00000	0.40218	0.57236
0.85	0.00000	0.44396	0.54187
0.90	0.00000	0.50553	0.49694
0.95	0.00000	0.62147	0.42006

It gives a more complete picture of the conditional distribution than a single estimate of the center like linear regression techniques. If certain data is very small or big and not in the range, authors can eliminate them in the Quantile Regression. In our dataset, for the initial few days, the data is not significant and if authors considered them for any prediction then the accuracy of the results might be compromised. Handling outliers is vital for any real time prediction so traditional technique like linear regression is not fitted every times. Results showed that Quantile Regression is vital for handling outliers. The Figure-1 shows the confidence interval of coefficients in the case of quantile regression model. The red lines described the magnitude of linear regression model. For every coefficient, the magnitude of red lines is very narrow while actual data is dispersed among different quantiles so quantile regression model provides more insights about the data in terms of prediction.

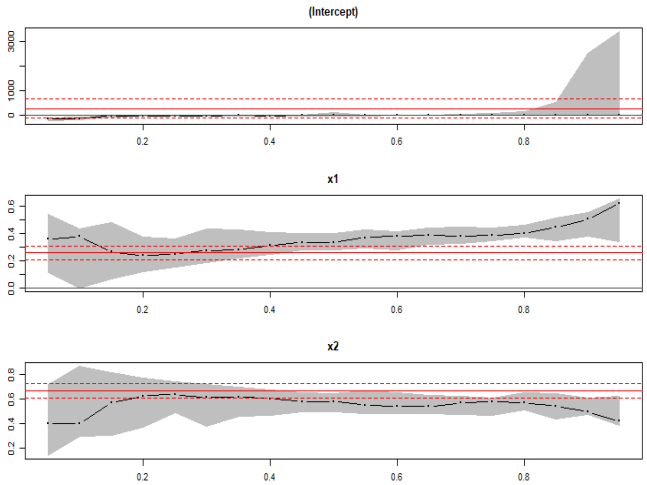

Figure-1 Confidence Interval of Coefficients in Quantile Regression

VII. CONCLUSIONS

Linear regression technique is widely used for time series data analysis. Linear regression is simplest technique for implementation. The results of linear regression are based on only one central value. Linear regression provides efficient results when data are normally distributed. However, when dataset consists of outliers then the results of linear regression based techniques might be compromised. In this research, authors have identified limitations of linear regression based on experiments. Authors did experiments on 239 days' corona cases in India and applied linear regression and quantile regression techniques on same data. Linear regression technique gave one value of coefficients i.e Intercept and X1,X2 values and considered all the data even though several data having 0 values. Quantile regression provided different values of coefficients based on the percentile applied. Based on the results of initial percentiles such as 0.05 and 0.10, the intercept values are very less and if authors considered them for the prediction then the overall accuracy of the model might be compromised. Based on the proposed research, authors have concluded that outlier handling is very vital in the prediction of any real scenario and quantile regression model is suitable in such scenarios.

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Design of Reconfigurable Architecture Using Reverse Carry Propagate Adder for Energy Efficient DSP Applications

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Abstract— Now a days Hardware acceleration was proven to be an highly promising implementation technique for the digital signal processing (DSP) domain. Rather than selecting a monolithic application-specific integrated circuit design approach, In this abstract, we provide a novel accelerator architecture consisting of flexible computational units that helps the execution of a huge amount of operation templates available in DSP kernels. Adders plays a vital role in many digital signal processing applications and An well organised Reverse carry propagate adder (RCPA) is shown in this paper. In this RCPA structure, the carry signal propagates from the high significant bit (MSB) to the less important bit (LSB) in a reverse way; thus the Carry signal is more appropriate when compared to the production. In this case of delay variance, this propagation technique improves stability. And also we use combination of hybrid structure in the n bit adder design were by using accurate high speed adder like Brent–Kung adder to add first half of n bit adder i.e. most significant half. Using Brent–Kung adder we can increase the adder speed and least half of the adder design is implemented by using Reverse Carry Propagate Adder (RCPA). The structure of Hybrid adders are studied and compared with that of conventional approximate adders using Xilinx ISE 14.7 software with Verilog HDL coding.

Key Words— Approximate adder, Brent–Kung adder (BKA), Digital signal processing (DSP), Reverse carry propagate adder (RCPA)

I. INTRODUCTION

Adder blocks are the important components in arithmetic units of DSP systems, are power hungry and usually form hot-spot locations in the die. These provide the motivations for realizing this kind of component using the approximate computing approach. General purpose processors and instruction sets for DSP's include at least one type of addition. Some instructions such as subtraction and multiplication includes addition in their operations, and their underlying hardware is similar or identical to addition hardware. Often, In design an adder or multiple adders will be in the crucial path , hence the design performance will be usually restricted by the performance of its multiple adders or adders. When looking at remaining attributes of a chip, such as power or area, the designer will find that the hardware used for addition will be a more contributor to these areas. Therefore it is beneficial to choose the correct adder to implement in a design because of the many other factors it affects the overall chip. The use of high speed processing is increasing as a result of expanding applications such as signal and computer processing. Arithmetic operations with higher throughput are the important factor to achieve the desired performance in many image processing and real-time signal applications.

Digital signal Processing (DSP) is finding its way into many applications , and due to its demand it has taken place into a huge number of a commercial processors . Digital signal processors (DSP) have various architectures and features when compared to general purpose processors, The whole processor performance is determined by the gain performance of these features. Previous researches on approximate adders have taken two general approaches of focusing on error probability reductions and error weight. To reduce power consumption and to increase speed are the key goals to design a digital processing units, mainly the portable systems. Usually, an increase in the speed results in more power Consumption for exact processing units. Another approaches to improve both the speed and power is to sacrifice the computation exactness.

The approach, which is approximate computing, It is used for the applications where few errors maybe tolerated. One of the approach is based on a hybrid structure adder where two different parts, approximate least significant bits (LSBs) and exact MSBs are utilized. The error appears in the input carry of the exact most significant bit (MSB) part and the summation in the LSB part. This limits the error weight of the carry input of the MSB part. Since usually most of the activities occur in the LSB part. In the second approach, pure approximate adder structures are used. For these adders, decreasing the power and delay and also to reduce the error probability of the summation are the key design criteria.

In this paper, we will study on the hybrid adders where the use of the approximate reverse carry propagate full-adder (RCPFA) is suggested. The approximate adder propagates the carry input in a reverse way, i.e., from the high significant bit to low significant bit to form the carry out. In this type of adder, which is called as reverse carry propagate adder (RCPA), the propagation can be done by using a forecast signal acting as an output signal. By using the reverse carry propagation, the carry weight will be decreased as it propagates. The MSB half is added by using

parallel prefix adder as it can improve the speed of operation. The Lower part i.e LSB half will be added by using the approximate reverse carry propagate adder.

II. LITERATURE SURVEY

When compared to all the exact adder structures, the Ripple carry adder (RCA) has the worst power and area utilizations. Despite, It suffers from a huge delay. To increase the energy efficiency and speed of this adder, some previous works have sacrificed the accuracy.

An approximate RCA structure which is known as error tolerant adder Structure (EAS) has been presented. The structure of EAS is shown in Fig.

In this design, the input operands are seperated into 2 parts called exact computation part and inexact computation part. In the exact part is the MSB part, the conventional FAs with a zero input carry for the each part are used wherease the inexact part is the LSB part which consists of a carry-free addition part.

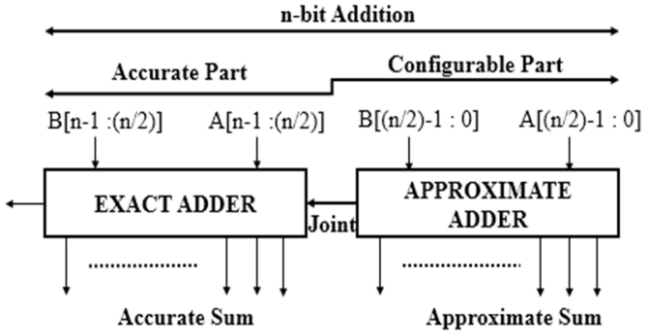

Fig.1 Error tolerant adder structure

To design an adder using carry propagation will have more delay so by avoiding the carry propagation while designing an adder will results in the better adder performance so we choose an reverse carry propagate adder in which the carry is propagated in reverse manner.

The conventional FA is the most important building block of the reverse carry propagate adders has 3 inputs with the equal weight. Moreover, For a summation result it has 2 outputs with the equal weight as similar to the inputs and a output carry with double the weight. The carry propagation delay (tCP*)* is one of the important timing factor in an FA because of the fact that it used to find the critical path delay of multi bit adders (and multipliers). A small short-delay violation can lead to a large amount of error owing to the reason that the error occurs on the MSBs of the summation.

This is the result of the propagation and generation of the input carry of the MSBs through less significant bit FAs. Due to this reason, if the order of the carry propagation is reversed, one can see the decrease in the amount of error due to the timing violation.

1. Reverse Carry Propagate Full-Adder Cell

Each exact FA generates its sum and carry output signals using

$$2Ci+1 + S_i = A_i + B_i + C_i \quad (1)$$

Where Ai (Bi) is the i^{th} bit of the input A(B), Ci(Ci + 1)is the carry in (output), and *Si* is the i^{th} bit of the sum.

Based on this equation, the output signals in the i^{th} bit position relay on the i^{th} bits of the inputs *A* and *B* and the carry out of the previous position (Ci). By moving the term Ci (Ci + 1)to the left (right) of the equation, one can write as

$$S_i - C_i = A_i + B_i - 2Ci+1 \quad (2)$$

Considering equation (2), one can think of a full adder as a design whose operation depends on the carry out of the (i + 1)nth bit position (Ci + 1)and its input operand bits. For this structure, the sum and the carry signals having the equal weights are the outputs .

From the above discussion, we suggest a family of full adders for the RCPFA shown in Fig.

As shown in Fig. 2, these full adders have four inputs and 3 outputs. The inputs are the input operands (Ai and Bi), the carry out of the next bit position (Ci+1), and a forecast signal (Fi). The RCPFA determines the carry (Ci), summation result (Si), and the forecast signal (Fi+1) as its output signals. As mentioned earlier, the advantage by using the RCPA is that the value of the error is in the direction with respect to decrease in the bit significance. This shows that the cumulative impact factor of the error (e.g., because of the delay variation) during the carry propagation is lower for bits with higher significances.

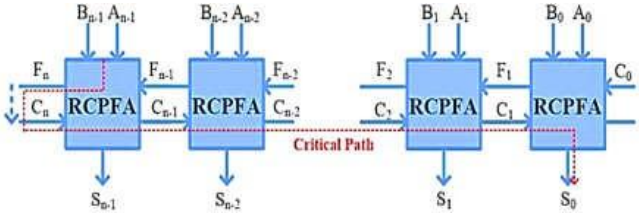

Fig.2 n-bit RCPA.

To determine a structure for RCPFA, the Karnaugh maps of the summation result (S_i) and carry (C_i) were drawn based on (2) and considering the forecast signal (F_i) as an input (Fig. 3) The Boolean equation between inputs gives rise to Si and Ci

$$S_i = C_{i+1}F_i + C_{i+1}A_i + C_{i+1}B_i + A_iB_iF_i \quad (3)$$

$$C_i = C_{i+1}F_i + C_{i+1}A_i + C_{i+1}B_i + A_iB_iF_i . \quad (4)$$

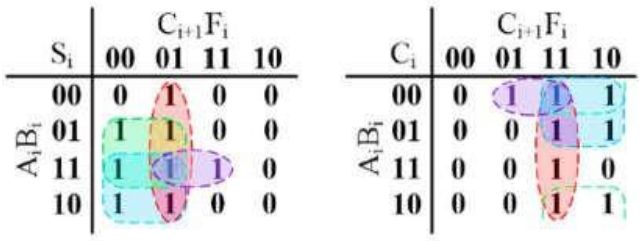

Fig.3 Karnaugh maps for signals *Si* and *Ci* of the general form of RCPFA.

Based on our design requirement we use 3 types of reverse carry propagate adders the designs of those adders is shown below. By using these proposed adders we can implement 3 types of reverse propagate adders and are it is used in the place of approximate adders which is shown on figure 1.

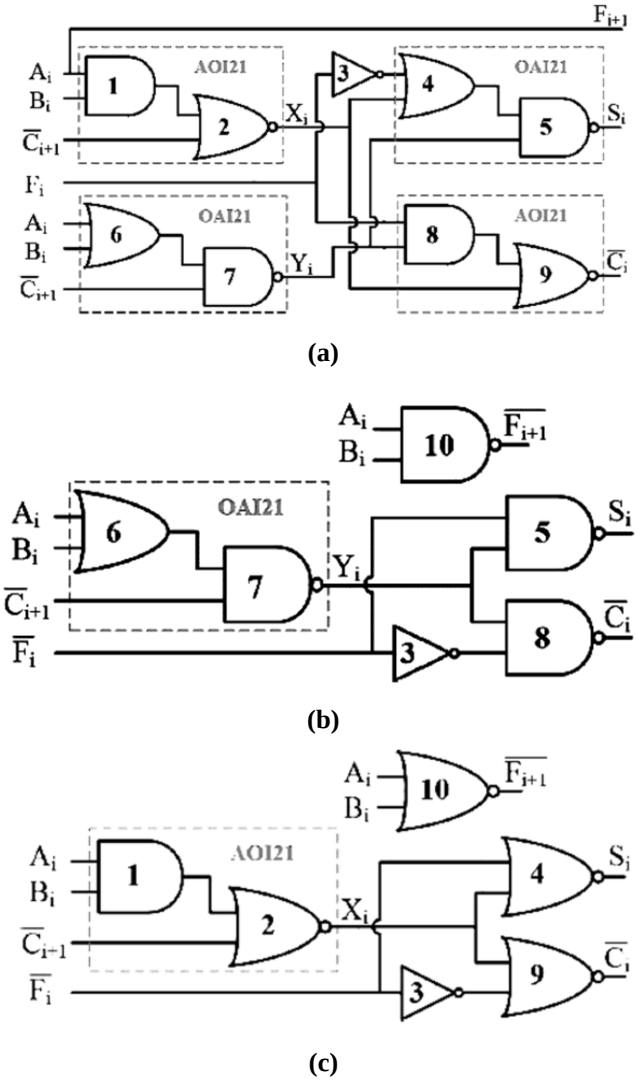

Fig.4 Internal structures of the (a) RCPFA-D1, (b) RCPFA-D2, (c) RCPFA-D3

The block diagram of an n-bit adder which is designed with the help of reverse carry propagate adder is shown in below figure

As mentioned before, the weight of the carry decreases as the carry propagates in a counter-flow manner.

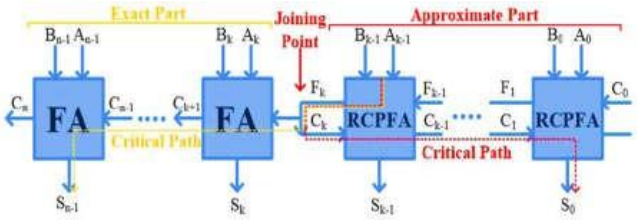

Fig.5 Architecture of an n-bit adder with RCPA This property helps having less vulnerability to the delay variation (due to process and supply voltage variations) impact for this adder when compared to other proposed approximate FAs. This is especially advantageous in the case of hybrid adders with large sizes for the approximate part which determines the critical path of the adder. The proposed RCPFAs may be used in hybrid adders whose general *n*-bit structure based on the RCPFAs is depicted in Fig. 8. Obviously, the design parameters of the adder relay on the width part of the approximate adder.

III. PROPOSED METHOD

Here we will propose a new adder It is called as hybrid n-bit adder where we can see the use of the combination of two kinds of n/2 bit adder to form a n bit adder . To improve the delay performance we will use a parallel prefix adder called Brent–Kung adder. The delay in an adder depends on carry i.e. how fast it reaches each bit position. Thus, the major difficulty caused in design of binary addition is the carry chain which consists of the carries. As the increase in the width of the incoming operand , the delay and length of the carry chain increases. To improve the performance and to decrease the delay, the parallel prefix adders can be employed.

In this concept, parallel prefix adders is to compute a small amount of intermediate prefixes and then find the large group prefixes, until all the carry bits are computed. Parallel prefix addition of the operands A and B of width n is performed in 3 steps as given below:

1. Pre Processing
2. Carry Generation
3. Post processing

1. Pre-processing stage:

In first stage process we compute, The generate signals and propagate signals are utilized such that carry in of each adder is generated. A and B are inputs.

Brent-Kung adder is one of the popular and widely used adder. This adder is used for high performance addition operation. . It is one type of the parallel prefix adders. In case of Brent Kung adders along with the cost, the wiring complexity is also less. It is similar as a tree structure which performs the arithmetic operation. The Brent-kung adder has both gray cells and black cells. Every black cell will be of one OR gate and 2 AND gates . Every gray cell has

only one AND gate. gi refers to generate and it uses one AND gate and OR gate. pi refers to propagate and it uses only 1 AND gate. G_i refers to carry generate and it uses one AND gate and OR gate given in equation supports in first black cell. These signals are shown in the equation 5&6.

$$Pi = Ai \text{ Xor } Bi \ldots \ldots \quad (5)$$

$$Gi = Ai.\ Bi \ldots \ldots \quad (6)$$

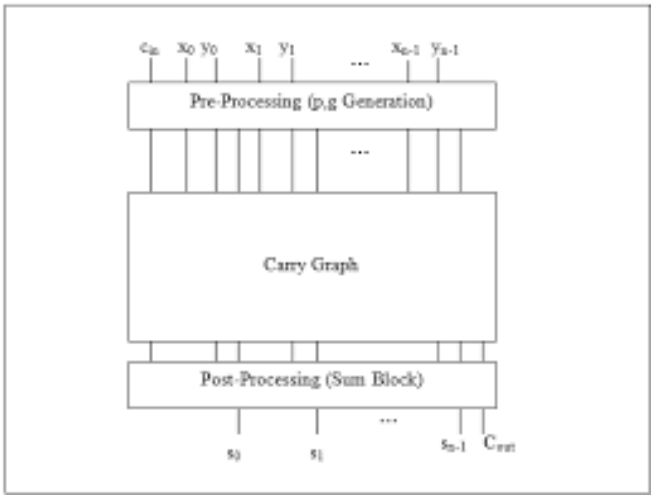

Fig.6 Block Diagram of Parallel prefix addition.

2. *Carry generation stage:*

In this generation stage we will obtain the carries with respect to every bit. Execution is done ased on a parallel form. After the computation of carries in parallel these are divided into many pieces. Carry operator contain 2 AND gates, one OR gate. It uses propagate(P_i) and generate(G_i) as intermediate signals which can be seen in the equations 7&8.

$$P(i:k) = P(i:j) \cdot P(j-1:k) \ldots \ldots \quad (7)$$

$$G(i:k) = G(i:j) + (G(j-1:k) \cdot P(i:j)) \ldots \ldots \quad (8)$$

This carry can generated by using different cell structures such as Gray cell, Black cell and Buffer cell. By use of this cell structures we will be able to calculate final carry and is similar for all parallel prefix adders but the design of carry generation is different.

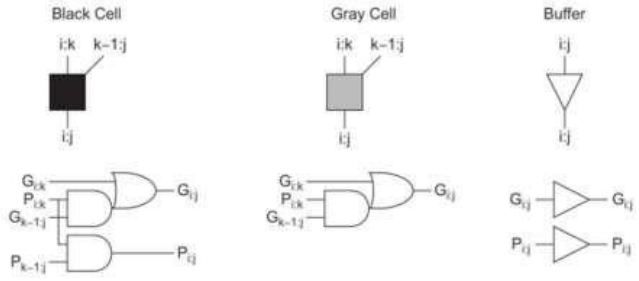

Fig.7 Black Cells, Gray Cells and Buffer cell used for carry generation stage.

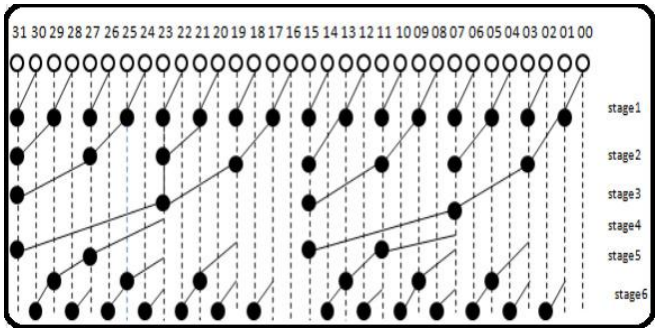

Fig.8 Carry generation of an 32-bit Brent–Kung adder

3. *Post Processing:*

The sum is generated either by the use of simple XOR gates or by the use of conditional sum adders. In conditional sum adders, for each bit position, It generates two tentative sums and the correct one will be selected when the relevant carry for that bit arrives.

Proposed Adder architecture is shown in below figure:

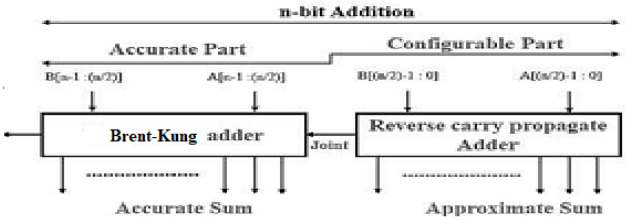

Fig.9 Modified Hybrid adder Architecture.

IV. RESULT

By implementing the adder by using two sub adders like Brent-Kung adder and reverse carry propagate adder we can have better in terms of delay and energy. Here in this paper we present 32- bit adders with the design of reverse carry propagate adders. The results are presented in the below table

S.No	32 bit adder	Existing Method	Proposed Method
1	Area	95	112
2	Delay	21.765	15.296
3	power	5.521	4.485

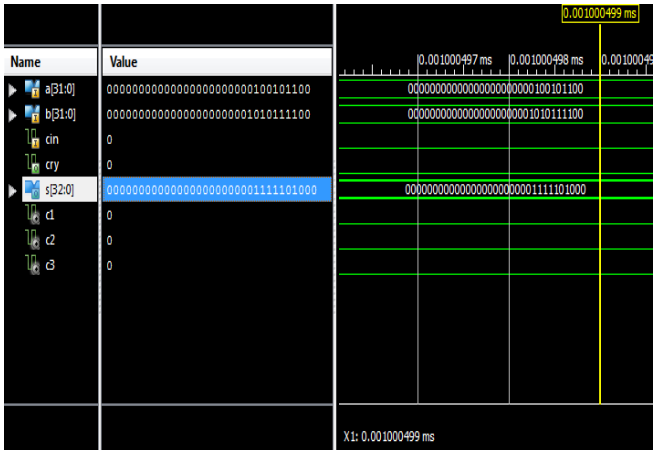

Fig.10. Simulation Results

V. CONCLUSION

Here, we have designed and implemented an n-bit adder with a hybrid architecture by the use of 2 types of adders to implement a large adder. We use approximation in lower half addition that is least significant side and accurate addition in higher half that is most significant side. The accurate adder we used in this project is a Brent-Kung adder which is a form of parallel prefix adder and the approximate adder we used is the RCPA we designed in this paper. By use of this architecture we can save energy and also get better delay..

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Implementation of Area Optimized Hybrid LUT FPGA Architectures

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Abstract— Hybrid configurable logic block architectures for optimized area with high frequency that contain a mixture of lookup tables and hardened multiplexers are evaluated toward the goal of higher logic density and area reduction. This paper proposes Multiple hybrid configurable logic block architectures, both non fracturable with varying MUX: LUT logic element ratios. The designed multiplier Logic element is used for the operation of multiplier. Experimental Results are observed using Xilinx ISE 12.3i and are compared with the proposed and the existing techniques.

Key Words— hybrid complex logic block, multiplexer (MUX)

I. INTRODUCTION

Throughout the history of field-programmable gate arrays (FPGAs), lookup tables (LUTs) have been the primary logic element (LE) used to realize combinational logic. A *K*-input LUT is generic and very flexible—able to implement any *K*-input Boolean function. The use of LUTs simplifies technology mapping as the problem is reduced to a graph covering problem. However, an exponential area price is paid as larger LUTs are considered. The value of *K* between 4 and 6 is typically seen in industry and academia, and this range has been demonstrated to offer a good area/performance compromise. Recently, a number of other works have explored alternative FPGA LE architectures for performance improvement to close the large gap between FPGAs and application-specific integrated circuits (ASICs). In this paper, we propose incorporating (some) hardened multiplexers (MUXs) in the FPGA logic blocks as a means of increasing silicon area efficiency and logic density. The MUX-based logic blocks for the FPGAs have seen success in early commercial architectures, such as the Actel ACT-1/2/3 architectures, and efficient mapping to these structures has been studied in the early 1990s. However, their use in commercial chips has waned, perhaps partly due to the ease with which logic functions can be mapped into LUTs, simplifying the entire computer aided design (CAD) flow. Nevertheless, it is widely understood that the LUTs are inefficient at implementing MUXs, and that MUXs are frequently used in logic circuits.

II. LOOKUP TABLES

The basic method used to build a combinational logic block (CLB) also called a logic element in an SRAM-based FPGA is the lookup table (LUT). As shown in Figure, the lookup table is an SRAM that is used to implement a truth table. Each address in the SRAM represents a combination of inputs to the logic element. The value stored at that address represents the value of the function for that input combination. An n-input function requires an SRAM with locations.

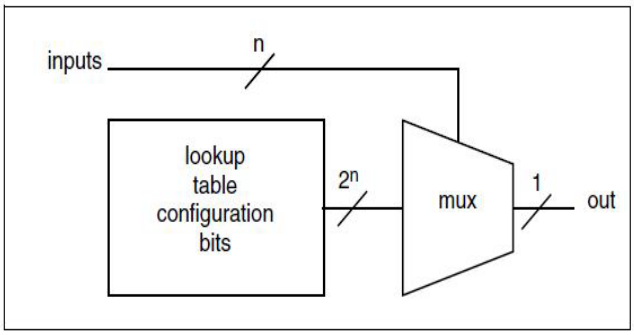

Fig 1: Lookup Tables

Because a basic SRAM is not clocked, the lookup table logic element operates much as any other logic gate as its input's changes, its output changes after some delay.

III. PROGRAMMING A LOOKUP ABLE

Unlike a typical logic gate, the function represented by the logic element can be changed by changing the values of the bits stored in the SRAM. As a result, the n-input logic element can represent functions (though some of these functions are permutations of each other).

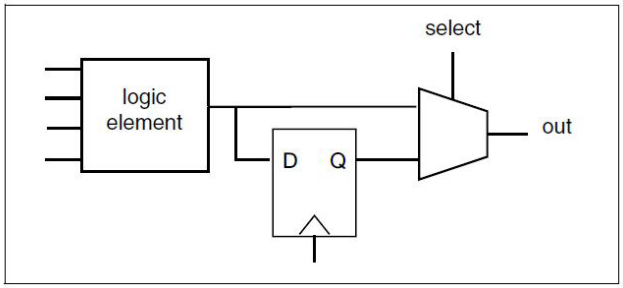

Fig-2 Programming A Lookup Table

A typical logic element has four inputs. The delay through the lookup table is independent of the bits stored in the SRAM, so the delay through the logic element is the same for all functions. This means that, for example, a lookup table-based logic element will exhibit the same delay for a 4-input XOR and a 4- input NAND. In contrast, a 4-input XOR built with static CMOS logic is considerably slower than a 4- input NAND. Of course, the static logic gate is generally faster than the logic element. Logic elements generally contain registers flip-flops and latches as well as combinational logic. A flip-flop or latch is small compared to the combinational logic element (in sharp contrast to the situation in custom VLSI), so it makes sense to add it to the combinational logic element. Using a separate cell for the memory element would simply take up routing resources. The memory element is connected to the output; whether it stores a given value is controlled by its clock and enable inputs. In this paper, we propose incorporating (some) hardened multiplexers (MUXs) in the FPGA logic blocks as a means of increasing silicon area efficiency and logic density. The MUX-based logic blocks for the FPGAs have seen success in early commercial architectures, such as the Actel ACT- 1/2/3 architectures, and efficient mapping to these structures has been studied in the early 1990s. However, their use in commercial chips has waned, perhaps partly due to the ease with which logic functions can be mapped into LUTs, simplifying the entire computer aided design (CAD) flow. Nevertheless, it is widely understood that the LUTs are inefficient at implementing MUXs, and that MUXs are frequently used in logic circuits. In this paper, we present a six-input LE based on a 4-to-1 MUX, MUX4, that can realize a subset of six-input Boolean logic functions, and a new hybrid complex logic block (CLB) that contains a mixture of MUX4s and 6-LUTs. The proposed MUX4s are small compared with a 6-LUT (15% of 6-LUT area), and can efficiently map all {2,3}-input functions and some {4,5,6}-input functions.

IV. LUT/MUX LOGIC ARCHITECTURE

The hybrid lut/mux fpga logic architectures source tool-flow from C through LegUp-HLS to the VTR flow. Sparse crossbars (versus full crossbars in the previous work) have also been included in our CLBs, increasing modelling accuracy. The new transistor-level modelling of the MUX4 also provides more accurate results as compared with the previous work. Results have also been expanded with the inclusion of timing results as well as larger architectural ratio sweeps. The remainder of this paper is organized as follows. The proposed MUX4 LE, the variant used in the fracturable architecture and the design of the hybrid complex logic block. the technology mapping approaches to target the proposed hybrid architecture. we modeled the hybrid complex logic blocks for both the nonfracturable and fracturable architectures in VPR. our evaluation methodology and provides the evaluation results.

A) MUX4: 4-TO-1 MULTIPLEXER LOGIC ELEMENT

The MUX4 LE shown in Fig. 3 consists of a 4-to-1 MUX with optional inversion on its inputs that allow the realization of any {2,3}-input function, some {4,5}-input functions, and one 6-input function a 4-to-1 MUX itself with optional inversion on the data inputs. A 4-to-1 MUX matches the input pin count of a 6-LUT, allowing for fair comparisons with respect to the connectivity and intra cluster routing. Any two-input Boolean function can be easily implemented in the MUX4: the two function inputs can be tied to the select lines and the truth table values (logic-0or logic-1) can be routed to the data inputs accordingly. For three-input functions; consider that Shannon decomposition about one variable produces cofactors with at most two variables. A second decomposition of the cofactors about one of their two remaining variables produces cofactors with at most one variable. Such single variable cofactors can be fed to the data inputs (the optional inversion may be needed), with the decomposition variables feeding the select inputs. Likewise, functions of more than four inputs can be implemented in the MUX4 as long as Shannon decomposition with respect to any two inputs produces cofactors with at most one input.

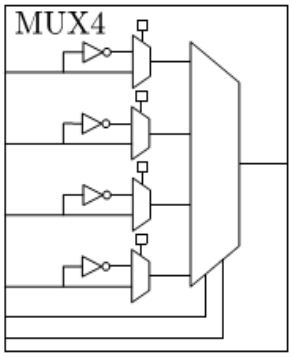

Fig.3. MUX4 LE depicting optional data input inversions

Logic Elements, Fracturability, and MUX4-Based Variants

Two families of architectures were created:

1) Without fracturable LEs

2) With fracturable LEs.

In this paper, the fracturable LEs refer to an architectural element on which one or more logic functions can be optionally mapped. Nonfracturable LEs refer to an architectural element on which only one logic function is mapped. In the nonfracturable architectures, the MUX4 element shown in Fig. 3 is used together with nonfracturable 6-LUTs. This element shares the same number of inputs as a 6-LUT lending for fair comparison with respect to the input connectivity. For the fracturable architecture, we consider an eight-input LE, closely

matched with the adaptive logic module in recent Altera Stratix FPGA families. For the MUX4 variant, Dual MUX4, we use two MUX4s within a single eight-input LE. In the configuration, shown in Fig. 4, the two MUX4s are wired to have dedicated select inputs and shared data inputs. This configuration allows this structure to map two independent (no shared inputs) three-input functions, while larger functions may be mapped dependent on the shared inputs between both functions. An architecture in which a 4-to-1 MUX (MUX4) is fractured into two smaller 2-to-1 MUXs was considered.

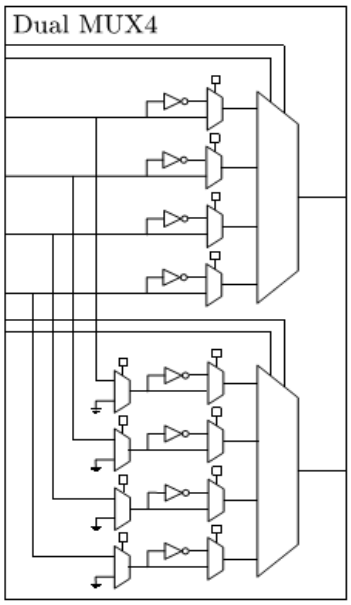

Fig.4. Dual MUX4 LE that utilizes dedicated select inputs and shared data Inputs

V. HYBRID COMPLEX LOGIC BLOCK

A variety of different architectures were considered the first being a nonfracturable architecture. In the non fracturable architecture, the CLB has 40 inputs and ten basic LEs (BLEs), with each BLE having six inputs and one output. Fig.5 shows this nonfracturable CLB architecture with BLEs that contain an optional register. We vary the ratio of MUX4s to LUTs within the ten elements CLB from 1:9 to 5:5 MUX4s:6-LUTs. The MUX4 element is proposed to work in conjunction with 6-LUTs, creating a hybrid CLB with a mixture of 6-LUTs and MUX4s (or MUX4 variants).

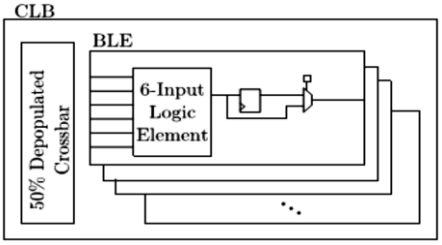

Fig. 5. Hybrid CLB with a 50% depopulated intra-CLB crossbar depicting BLE internals for nonfracturable (one optional register and one output) architecture.

Fig. 6 shows the organization of our CLB and internal BLEs. For fracturable architectures, the CLB has 80 inputs and ten BLEs, with each BLE having eight inputs and two outputs emulating an Altera Stratix Adaptive-LUT. The same sweep of MUX4 to LUT ratios was also performed. Fig. 4 shows the fracturable architecture with eight inputs to each BLE that contains two optional registers. We evaluate fracturability of LEs versus nonfracturable LEs in the context of MUX4 elements since fracturable LUTs are common in commercial architectures. For example, Altera Adaptive 6-LUTs in Stratix IV and Xilinx Virtex 5 6-LUTs can be fractured into two smaller LUTs with some limitations on inputs.

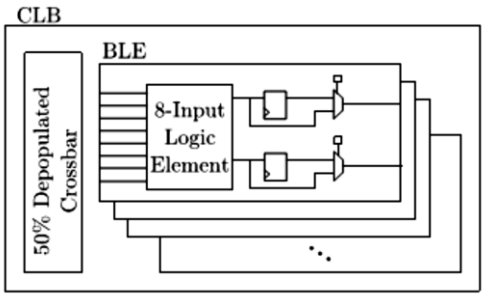

Fig.6. Hybrid CLB with a 50% depopulated intra-CLB crossbar depicting BLE internals for a fracturable (two optional registers and two outputs) architecture.

VI. RESULTS

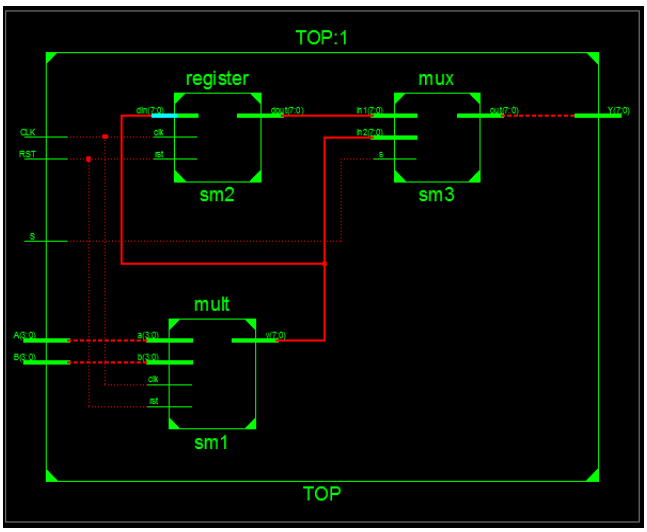

Fig7: RTL Schematic

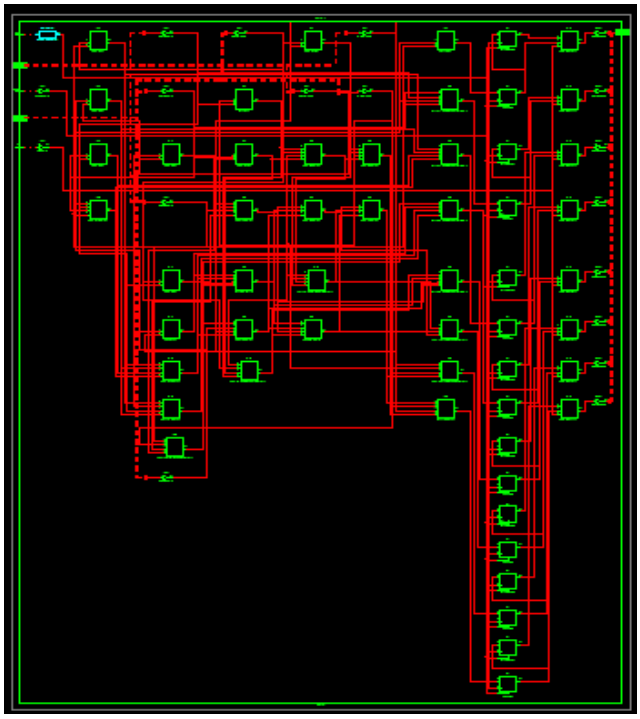

Fig8: View technology schematic

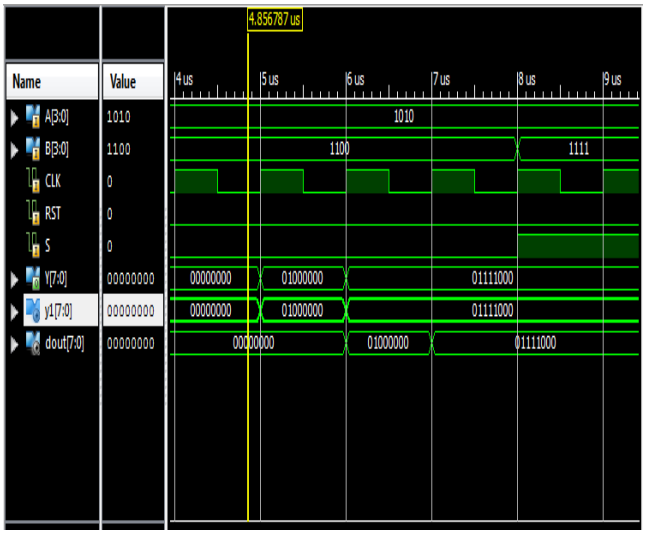

Fig9: simulated wave forms

Table 1: Parameter comparison table

Parameter	EXISTED DESIGN	PROPOSED DESIGN
No of LUTs	64	39
Frequency (MHz)	449.438	742.942
Power (mW)	1.012	0.522

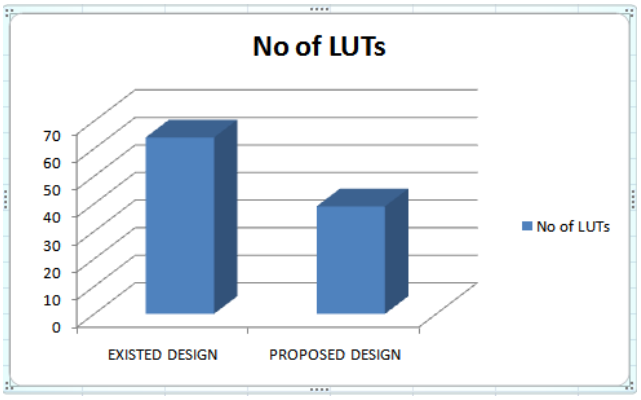

Fig10: LUT comparison bar graph

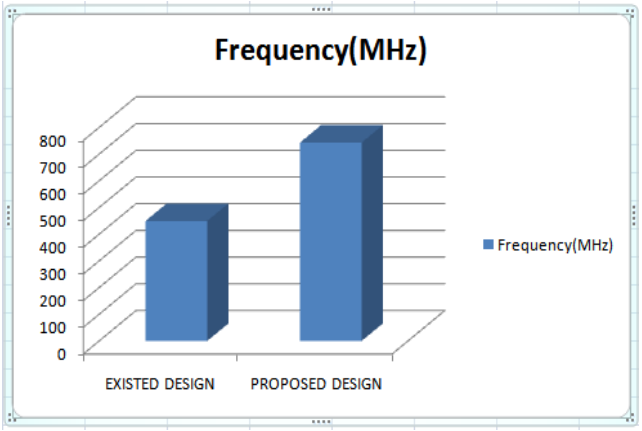

Fig 11: Frequency comparison bar graph

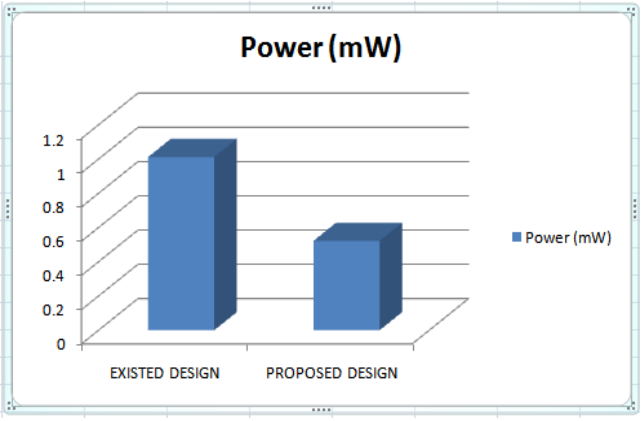

Fig 12: Power Comparison Bar Graph

VII. CONCLUSION

In this paper, a new hybrid CLB architecture containing MUX4 hard MUX elements and shown techniques for efficiently mapping to these architectures. by also providing analysis of the benchmark suites post mapping, discussing the distribution of functions within each benchmark suite. The designing of MULTIPLIER is shown marginally with better performance. Overall, the addition of MUX4s to architectures minimally impact Frequency Max and shown potential for improving logic-density in non-fracturable

architectures and modest potential for improving logic density in architecture.

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A Review on Fragility Analysis of Bridges

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Abstract— As the Bridges make the journey convenient and quicker, but they are vulnerable to forces that might inflict considerable damages and render them hazardous due to earthquake action. Structural harm to bridges, building damage, beginning of slope collapses, and tsunami are common effects of earthquakes. A brief literature on seismic behaviour of bridges under seismic action is presented in this review paper. Numbers of parameters/factors which affect the bridge and efficient method of Analysis identifies from this literature survey. This paper create ease to get a theoretical base for the needful researches, evaluate the correct methodology and get a clear view. To date, some inquiries have concerted on the effects of higher-mode of different parameters on the seismic performance of different types of bridges. Therefore, this paper, in its essence, extract and considers possible factors which influence seismic behaviour of bridges to prioritize retrofit, pre-earthquake planning, and loss measurement tools. The work is conceived in several parts. The introduction briefly describes the Bridge type, seismic design philosophies as well as the selection of possible methods of analysis. This study aims to finding some measures that can help to reduce the several seismic effects on bridge structures.

Key Words— Fragility; Bridges; Non-Linear Static Pushover; Dynamic Time History; Incremental Dynamic Method

I. INTRODUCTION

The design concept for earthquake-safe bridges is focused on the necessity that communications should be maintained to an acceptable level during all earthquakes. This can preferably be accomplished by maintaining that there is an appropriate likelihood of damage occurring at three major earthquake intensity levels over structure's existence. The three levels are defined as follows:

First for earthquakes with a return time lesser than 50% of the structure's duration, which can exist many times over its lifetime, the damage must be minor and contact must not be disrupted. The bridge can sustain significant damage, but it should not collapse. Second level, If an earthquake happens with such a return time of 50 to 150 % of the bridge's life span. Bridges must be restored on a continuous basis to standards suitable for vehicle and earthquake load, and they must be used for emergency traffic following an easy and fast repair. The supervisory authority determines the degree to which this is practiced and third, when bridge can sustain significant damage, but it should not collapse. Damage can be serious in an earthquake with a return time of more than 150 percent of the bridge's lifespan. It can be used after temporary repairs in traffic incidents and may be usable after permanent repairs for lower vehicle loads [11]

II. SEISMIC ANALYSIS OF STRUCTURE

Seismic analysis is a structural analysis which assess the structure's response under earthquake loading. For that region where Earthquake are prevalent, seismic analysis plays most important role in the method of structural design. Most structures have higher response modes, which are differently activated during Earthquake, it can be due to combining effect of more than one load as sometimes Wind with Earthquake load acts at same time. These analyses can be either Linear or Non- Linear. For performing and should be approached with specific objectives, Non-Linear Analysis involves more Advantageous efforts. Some typical case here Non-Linear Analysis is applied for checking the structure's performance are as follows:

→ For designing / analysing retrofit measures for pre construct structures (Bridge, Building, Dam etc)

→ For Designing new structure that possess good response during any hazardous event.

→ For assessing structure's performance according to owner's requirement.

In contrast to well-developed linear design and analysis methods, inelastic analytical techniques that are not linear and their use in design are still developing and requiring engineers to develop new skills. Plastic analysis needs consideration of plastic behaviour and limitation of conditions based on deformations and strength.

III. NON-LINEAR STATIC PUSHOVER METHOD

Pushover is a flexible analysis method where the structure is under load of gravity and the lateral load pattern, which control the displacements. The lateral load can represent amount of shear at base caused by the earthquake load. The output develops static-pushover curve that creates a strength parameter against deflection. For example, performance may be related to the level of strength achieved by certain members against displacement at the critical zone. The results provide information about the ductile strength of the structural system and indicate the load rate and deviation where the failure occurs.

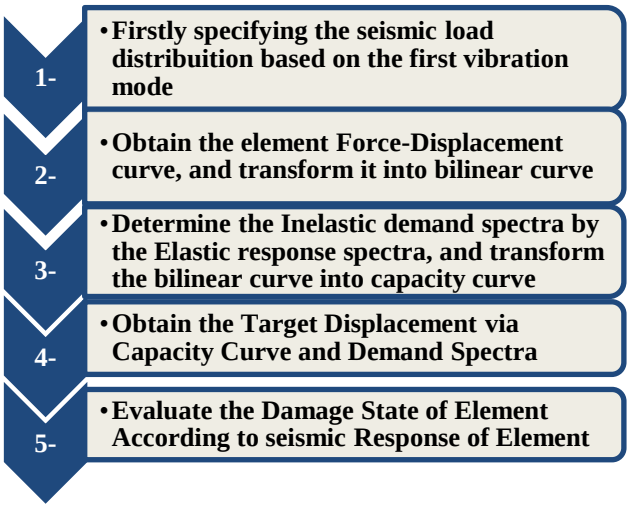

Figure 1 Flowchart of Non-Linear Static Pushover Analysis [10]

IV. DYNAMIC TIME HISTORY ANALYSIS

A typical earthquake history is needed to determine the structure in order to conduct such an analysis. The structural mathematical model is subjected to acceleration from earthquake records describing the predicted earthquake underneath the structure, or a nonlinear response history analysis which can be used to test the output of any structure in any earthquake, in this method. The time history method applies to both elastic and inelastic analysis. In this analysis, the structural stiffness features are thought to remain constant throughout the earthquake. In the inelastic analysis, however, stiffness is considered to be continuous during incremental time only. Analysis of the history of non-linear responses is used to generate demand sets, which predict performance. These sets are used to develop calculations that include median values and the spread of each desired parameter, and to find the correlation between the various requirements in the set.

V. INCREMENTAL DYNAMIC ANALYSIS

The IDA entails running multiple complex model analyses against a set of ground motion data, each of which is restricted to a different degree of seismic intensity. Even as structure experiences a collapse, the levels are suitably chosen to force the structure across the continuum action, from linear to plastic, and finally to strong ground motion variability. Post-adjustment results in IDA curves, for each record of earthquake magnitude, usually expressed by Intensity Measure (IM), comparison to structural response, as calculated by the Engineering demand parameter (EDP). Scalar (or vector irregular) values relative to the intensity of observed ground motion and measured linearly or non-linearly according to its amplitude are possible IM choices. IM is well-chosen in order to produce the necessary hazard curves for centuries-old risk analysis. Conversely, to minimize the amount of response history analysis needed, IM should be followed by a structural response interest. Ground speed acceleration, high ground speed are options, but the most widely used spectral acceleration has a damping of 5% during the first structure mode.

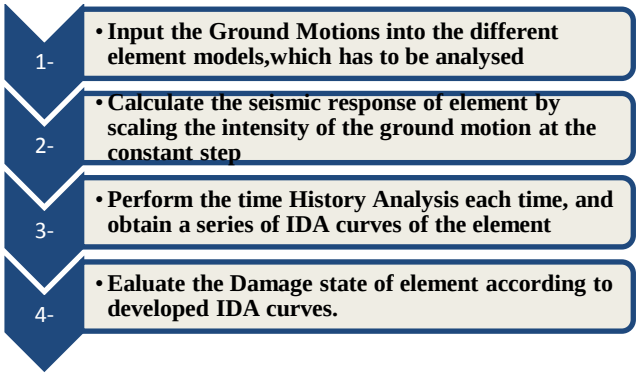

Figure 1 Flowchart of Incremental Dynamic Analysis [10]

VI. SCOPE OF PREVIOUS WORK

The Study depicts the effects of the construction of a standard single circular (RC) bridge pier's fragility curve [6]. The study considers various parameters such as concrete strength, yield strength of longitudinal steel rebar as well as their quantity, axial load level, reinforced compound and carbon fibre, shear span-depth quantitative relationship, PGA values [6]. In that study *The amount of reinforcement, axial load level as well as span-depth ration were found to have a major impact on the collapse fragility of the bridge piers which are retrofitted [6]. NLSPA method was used in that study [6]. One another Study has been carried out by researchers in that High Piers of Bridges Found more efficient than the lower one [4]. Only for peak ground accelerations less than 0.4g does the response of piers against earthquake from pushover comply with those from IDA [4]. Skewness is anlysed in that study [1]. “Reference [1] establish Fragility Curve for the continuous bridge (3-span) multi bent pier having different skew angle using analytical method. Deck torsion increases from 0 KNm to 79.24 KNm as the bridge skew angle changes from 0 degree to 60 degree under the gravity load case only for the studied bridge [1]. They had done their research on the steel rolled H-section to create an innovative type of SRC Bridge (steel reinforced concrete) girder [3] , Through this experimental based study partial SRC bridge were found that new SRC form of bridges has adequate ductility and bending strength. From the girder to the pier, the imposed load was transferred easily via stiff connection, and cracks on the concrete surfaces were within permissible limits [3]. Various Research has been done using Dynamic Time History Analysis on Different Bridge Types [5], [9], [2], [7]. Some damage fragility formulas are configured in this study for earthquake intensities measured in both the horizontal and vertical directions of the bridge using spectral acceleration (Sa) [5]. According to Wei et al. “The super-tall tower cable-stayed bridge having the combined middle tower and side floating towers seems to have the minimum damage possibility while both the cable restraint and horizontal fluid viscous damper can get some

mitigating effect, the fluid viscous damper seems to have a better effect" [9]. Bridge seismic behaviour is typically controlled by the rubber bearing not by pier columns [2]. this study found that the bridge seismic behaviour is typically controlled by rubber bearing not by pier columns so the failure of bearing should be considered while analysing the structure [2]. This research investigates the impact on the Bridge's seismic fragility of seismic incidence angle with different heights of the piers [7]. A highway bridge is used in this research for evaluating the effect of incidence angle on fragility [7]. Wide range of configurations (models) are considered, ranging from normal to so-called highly irregular types [7]. The earthquake incidence angle's effect on the foundation was more effective than that the columns ductility and elastomeric bearings [7]. "Reference [8] had determined that how the variations of fragility for different components change as the degree and direction of ground motion change". Depending upon structural reliability theory, 3 limit state equations which are independent have been used to describe three forms of earthquake risk, two of these are related with pier biaxial shearing and bending vulnerability [8]. This analysis for RC columns determines the limit state function for bearing distortion in addition to the relative displacement of bearings [8]. Also, on basis of the failure plane, limit state equations for pier biaxial shearing and bending are established [8]. Fragility curves have been used to show clearly how the variations of fragility for different components change as the degree and direction of ground motion change [8].

VII. DISCUSSION

This study aims to explore some of the different variables that influence the Seismic behaviour of Bridges and how they affect differently for different types of Bridges and finding some measures that can help to reduce the several seismic effects on bridge structures. After the further study in the area of performance of bridges during seismic action, it was found that no fragility analysis for the bridges located in hilly areas has been done. Some other limitations came out from the previous studies i.e., Currently, none of the considered design codes provides any check on maximum displacement that can be permissible for bridge piers. This limitation results in significantly higher collapse probabilities in case of taller piers.

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A Modified Partial Product Generator for Redundant Binary Multipliers

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Abstract— Due to its high modularity and carry-free addition, redundant binary (RB) representation can be used when designing high performance multipliers. The conventional RB multiplier requires and additional RB partial product (RBPP) row, because an error-correcting word (ECW) is generated by both the radix-4 Modified Booth encoding (MBE) and the RB encoding. This incurs in an additional RBPP accumulation stage for the MBE multiplier. In this paper, a new RB modified partial product generator (RBMPPG) is proposed; it removes the extra ECW and hence, it saves one RBPP accumulation stage. Therefore, the proposed RBMPPG generates fewer partial product rows than a conventional RB MBE multiplier. Simulation results show that the proposed RBMPPG based designs significantly improve the area and power consumption when the word length of each operand in the multiplier is at least 32 bits; these reductions over previous NB multiplier designs incur in a modest delay increase (approximately 5%). The power-delay product can be reduced by up to 59% using the proposed RB multipliers when compared with existing RB multipliers.

I. INTRODUCTION

Digital multipliers are widely used in arithmetic units of microprocessors, multimedia and digital signal processors. Many algorithms and architectures have been proposed to design high-speed and low power multipliers. A normal binary (NB) multiplication by digital circuits includes three steps.

In the first step, partial products are generated; in the second step, all partial products are added by a partial product reduction tree until two partial product rows remain. In the third step, the two partial product rows are added by a fast carry propagation adder. Two methods have been used to perform the second step for the partial product reduction. A first method uses 4-2 compressors, while a second method uses redundant binary (RB) numbers. Both methods allow the partial product reduction tree to be reduced at a rate of 2:1. The redundant binary number representation has been introduced by Avizienis to perform signed-digit arithmetic; the RB number has the capability to be represented in different ways. Fast multipliers can be designed using redundant binary addition trees.

Alternatively, a high-radixBooth encoding technique can reduce the number of partial products. However, the number of expensive hard multiples (i.e., a multiple that is not a power of two and the operation cannot be performed by simple shifting and/or complementation) increases too [14-16]. Besliet al.noticed that some hard multiples can be obtained by the differences of two simple power-of-two multiplies. A new radix-16 Booth encoding (RBBE-4) technique without ECW has been proposed in [14]; it avoids the issue of hard multiples. A radix-16 RB Booth encoder can be used to overcome the hard multiple problem and avoid the extra ECW, but at the cost of doubling the number of RBPP rows. Therefore, the number of radix-16 RBPP rows is the same as in the radix-4 MBE.

However, the RBPP generator based on a radix-16 Booth encoding has a complex circuit structure and a lower speed compared with the MBE partial product generator [10] when requiring the same number of partial products.

II. RB PARTIAL PRODUCT GENERATOR:

As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial products. The addition of two N-bit NB partial products X and Y using two‘ s complement representation can be expressed as follows: where is the inverse of, and the same convention issued in the rest of the paper. The composite number can be interpreted as a RB number. The RBPP is generated by inverting one of the two NB partial products and adding -1 to the LSB. Each RB digit _ belongs to the set _1, 0, 1_; this is coded by two bits as the pair. Note that 1 = −1. RB numbers can be coded in several ways. Table II shows one specific RB encoding, where the RB digit is obtained by performing Both MBE and RB coding schemes introduce errors and two correction terms are required: when the NB number is converted to a RB format, -1 must be added to the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or -2 during the Booth encoding, the number is inverted and +1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding. The conventional partial product architecture of an 8-bit MBE multiplier is shown in Fig. 1, where b_ represents the bit position, and is generated by using an encoder and decoder (Fig. 2). An N-bit CRBBE-2 multiplier includes N/4 RBPP rows and one ECW; the ECW takes the form as follows: where i represent the ithrow of the RBPPs. In a correction term is always required by RB coding. If also corrects the errors from the MBE recoding, then the correction term cancels out to 0. That is to say that if the multiplicand digit is inverted and added to 1, then is 0, otherwise is -1. The

error-correcting digit is determined only by the Booth encoding, no negative encoding1, negative encoding.

III. LITERATURE SURVEY:

In conventional digital computers, integers are represented as binary numbers of fixed length. There are several other number systems that are useful for certain applications. These include the Redundant Signed Digit Number System. In a redundant signed digit representation with radix r each digit is allowed to take more than r-values. Redundancy in representation makes faster addition and subtraction in which each sum or difference digit is a function of only the digits in the adjacent portions of the operands. In this project work we emphasize on the floating point representation of XLU numbers, which is based on signed digits. And various rounding schemes for them, namely truncate, nearest to zero, nearest to even, nearest to positive and negative infinity are discussed. Redundancy in the number system allows a method for fast addition and subtraction. Carry free addition is an attractive property of redundant signed digit number. The requirement for totally parallel addition and subtraction determines the minimum redundancy (r 2 values) which is necessary in the representation of one digit.

Low Power and High Speed Multiplication Design through Mixed Number

Representations

A low power multiplication algorithm and its VLSI architecture using a mixed number representation is proposed. The reduced switching activity and low power dissipation are achieved through the Sign-Magnitude (SM)notation for the multiplicand and through a novel design of the Redundant Binary (RB) adder and Booth decoder .The high speed operation is achieved through the Carry-Propagation-Free (CPF} accumulation of the Partial Products (PP) by using the RB notation. Analysis showed that the switching activity in the PP generation process can be reduced on average by 90%. Compared to the same type of multipliers [I, 2, 31, the proposed design dissipates much less power and is 18% faster on average.

Posibits, Negabits, and Their Mixed Use in Efficient Realization of Arithmetic Algorithms

Positively weighted and negatively weighted bits (posibits, negabits) have been used in the interpretation of 2‘ scomplement, negative-radix, and binary signed-digit number representation schemes as a way of facilitating the development of efficient arithmetic algorithms for various application domains. In this paper, we show that a more general view of posibits and negabits, along with their mixed use in any combination (using inverse encoding for negabits), unifies a number of diverse implementation schemes, while at the same time making the resultant designs more efficient by avoiding custom or modified hardware elements and restricting the implementation to the use of standard arithmetic cells. Such standard cells have been highly optimized and are continually improving due to their wide applicability.

High Speed 16×16-bit Low-Latency Pipelined Booth Multiplier

This paper presents a high-speed 16×16-bit CMOS pipelined booth multiplier. Actually in an n-bit modified Booth multiplier, because of the last sign bit, n/2 +1 partial product rows are generated rather than n/2. The extra row not only increases the delay and power consumption of Wallace tree, but also it leads to irregularity and complexity of Wallace tree designing. In this multiplier the last sign bit is removed by using a simple high-speed approach. This causes 4% reduction in power consumption and 5.2% reduction in transistor count. Also by using new partial product generation and booth encoder circuits and a novel adder, speed of pipelined multipliers is improved. By these new architectures, final adder performs 25 bit addition in only two cycles with high speed (1.6 GHz). Due to lower number of cycles (5 clock cycles), delay of the overall circuit is only 3.1ns and besides power consumption is decreased so that at a data rate of 1 GHz and under the supply voltage of3.3V, power consumption is 169mW.

Arithmetical Operations in Quaternary System Using

While performing the several arithmetic operations such as addition, subtraction and multiplication the speed of modern computers are limited because of carry propagation delay. A carry-free arithmetic operation can be achieved using higher radix number system such as Quaternary Signed Digit(QSD). In QSD, each digit can be represented by a number from-3 to 3. Using this number system any integer can be represented in multiple ways. With constant or fix delay and less complexity carry free addition, multiplication and other operations can be implemented on large number of digits. This paper deals with the implementation of QSD based arithmetic operations. The designs are simulated and synthesized using VHDL software, Model sim software is used for simulation. Arithmetic operations are widely used and play an important role in various digital systems such as computers and signal processors.

High-Speed Booth Encoded Parallel Multiplier Design

This paper presents a design methodology for high-speed Booth encoded parallel multiplier. For partial product generation, we propose a new modified Booth encoding (MBE) scheme to improve the performance of traditional MBE schemes. For final addition, a new algorithm is developed to construct multiple-level conditional-sum adder (MLCSMA). The proposed algorithm can optimize final adder according to the given cell properties and input delay profile. Compared with a binary tree-based conditional-sum adder, the speed performance improvement is up to 25 percent. On average, the design developed herein reduces the total delay by 8 percent for parallel multiplier. The whole design has been verified by gate level simulation.IN various computing and signal

processing applications, parallel multiplier has been a basic building block for many algorithms. Many high performance algorithms and architectures have been proposed to accelerate multiplication.

IV. PROPOSED RB PARTIAL PRODUCT GENERATOR

A new RB modified partial product generator based on MBE (RBMPPG-2) is presented in this section; in this design, ECW is eliminated by incorporating it into both the two MSBs of the first partial product row and the two LSBs of the last partial product row. It is different from the scheme in Fig. 1, where all the error-correcting terms are in the last row. ECW1 is generated by PP_ and expressed as ECW_ = 0 E__ 0 F__. (7)The ECW2 generated by PP_ (also defined as an extra ECW) is left as the last row and it is expressed to eliminate a RBPP accumulation stage, ECW2 needs to be incorporated. A modified radix-4 Booth encoding and a decoding circuit for the partial product are proposed here (Fig.4); an extra 3-input OR gate is then added to the design of [10] (Fig. 2). The three inputs of the additional OR gate are, when, it is clear that, and is set to all ones.

PROPOSED RBMPPG-2:

The circuit diagrams of the modified partial product variables and are shown in Fig. 5. It is clear that has the longest delay path. It is well known that the inverter, the 2-input NAND gate and the transmission gate (TG) are faster than other gates. So, it is desirable to use TGs when designing the multiplexer [5-6]. As shown in Fig. 5 (a), the critical path delay (the dash line) consists of a 1-stage AND-OR-Inverter gate, a 1-stageinverter, and 2-stage TGs. Therefore, RBMPPG-2 just increases the TG delay by 1-stage compared with the MBE partial product of Fig. 2.The above discussion is only an example; the above technique can be applied to design any 2_-bit RB multipliers. It eliminates the extra ECWN/4 and saves one RBPP accumulation stage, i.e., three XOR gate delays, while only slightly increasing the delay of the partial product generation stage. In general, an N-bit RB

RADIX-4 BOOTH ENCODING

Booth encoding has been proposed to facilitate the multiplication of two's complement binary numbers.

It was revised as modified Booth encoding (MBE) or radix-4 Booth encoding. The multiplier bits are grouped in sets of three adjacent bits. The two side bits are overlapped with neighboring groups except the first multiplier bits group in which it is {b1, b0, 0}. Each group is decoded by selecting the partial product shown in Table I, where 2A indicates twice the multiplicand, which can be obtained by left shifting. Negation operation is achieved by inverting each bit of A and adding _1‘ (defined as correction bit) to the LSB [10-13]. Methods have been proposed to solve the problem of correction bits for NB radix-4Booth encoding (NBBE-2) multipliers. However, this problem has not been solved for RB MBE multipliers.

RB PARTIAL PRODUCT GENERATOR:

As two bits are used to represent one RB digit, then a RBPP is generated from two NB partial products [1-6].The addition of two N-bit NB partial products X and Y using two‘ s complement representation can be expressed as follows Both MBE and RB coding schemes introduce errors and two correction terms are required: 1) when the NB number is converted to a RB format, -1 must be added to the LSB of the RB number; 2) when the multiplicand is multiplied by -1 or -2 during the Booth encoding, the number is inverted and +1 must be added to the LSB of the partial product. A single ECW can compensate errors from both the RB encoding and the radix-4 Booth recoding. The conventional partial product architecture

PROPOSED RB PARTIAL PRODUCT GENRATOR:

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Therefore, BMPPG-2 just increases the TG delay by 1-stage compared with the MBE partial product of Fig.

The above discussion is only an example; the above technique can be applied to design any 2_-bit RB multipliers.

V. DESIGN OF RBMPPG-2-BASED HIGH-SPEED RB MULTIPLIERS

The proposed RBMPPG-2 can be applied to any 2_-bit RB multipliers with a reduction of a RBPP accumulation stage compared with conventional designs. Although the delay of RMPPG-2 increases by 1-stage of TG delay, the delay of one RBPP accumulation stage is significantly larger than a 1-stage TG delay. Therefore, the delay of the entire multiplier is reduced. The improved complexity, delay and power consumption are very attractive for the proposed design. A 32-bit RB MBE multiplier using the proposed RBPP generator is shown in Fig. 6. The multiplier consists of the proposed RBMPPG-2, three RBPP accumulation stages, and one RB-NB converter. Eight RBBE-2 blocks generate the RBPP; they are summed up by the RBPP reduction tree that has three RBPP accumulation stages.

PERFORMANCE EVALUATION:

The performance of various 2_-bit RB multipliers using the proposed RBMPPG-2 is assessed; the results are compared with NBBE-2, CRBBE-2 and RBBE-4 multipliers that are the latest and best designs found in the technical literature. All designs of RB multipliers use the RBFA and RBHA of [7]. An RB-NB converter is required in the final stage of the RB multiplier to convert the summation result in RB form to a two‘ s complement number. It has been shown that the constant-time converter in [7] does not exist [19-

21]. However, there is a carry-free multiplier that uses redundant adders in the redution of partial products by applying on-the-fly conversion [22] in parallel with the reduction and generates the product without a carry-propagate adder [23-24].A hybrid parallel-prefix/carry-select adder [25] is used for the final RB-NB converter.

VI. FUTURESCOPE

A new modified RBPP generator has been proposed in this paper; this design eliminates the additional ECW that is introduced by previous designs. Therefore, a RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2_-bit RB multipliers to reduce the number of RBPP rows from __/4 + 1_ to __/4_.Simulation results have shown that the performance of RB MBE multipliers using the proposed RBMPPG-2 is improved significantly in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least32 bits. The PDP can be reduced by up to 59% using the proposed RB multipliers when compared with existing RB multipliers. Hence, the proposed RBPP generation method is a very useful technique when designing area and PDP efficient power-of-two RB MBE multipliers.

VII. CONCLUSION

A new modified RBPP generator has been proposed in this paper; this design eliminates the additional ECW that is introduced by previous designs. Therefore, a RBPP accumulation stage is saved due to the elimination of ECW. The new RB partial product generation technique can be applied to any 2_-bit RB multipliers to reduce the number of RBPP rows from __/4 + 1_ to __/4_.Simulation results have shown that the performance of RB MBE multipliers using the proposed RBMPPG-2 is improved significantly in terms of delay and area. The proposed designs achieve significant reductions in area and power consumption when the word length is at least32 bits.

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Assessment of Postharvest Practices and Qualitative Status of Turmeric Rhizomes from South western Ethiopia: The Case of Yeki, Sheko and Godere Districts

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Abstract— Despite cultivating turmeric as a cash crop to ensure the income of the household, efforts to improve turmeric postharvest practices in southwestern Ethiopia remain low. A cross-sectional survey was conducted in 2017 to assess socioeconomic status, postharvest practices, and quality of turmeric rhizomes in Southwestern Ethiopia. A formal survey involving 151 farmers across three districts of southwestern Ethiopia was conducted using structured and semi-structured questionnaires. With the appropriate perception indices, farmers' perceptions of each constraint in practicing postharvest activity were assessed by the use of a 5-point Likert scale. The result of this study revealed that the majority of the surveyed farmers experience traditional curing methods (94%) and open sun drying on bare land (85.4%) in the field. Only a few farmers used a cement floor (4.6%) and on the bed (4.0%) drying method. The result of the Likert-scale indicated that poor market information, limited access to finance, lack of technology, and unreliable transport were ranked from highest to lowest constraints in the postharvest activity of turmeric production. Besides exhibiting undesirable moisture content (12.32%), the maximum essential oil (3.37%), oleoresin (5.72%), and curcumin (3.53%) contents were obtained from the sample collected from Yeki district. These postharvest problems in the turmeric supply chain can be tackled through providing postharvest training to smallholder farmers.

Keywords— Socio-economic, Postharvest, Curing, Drying, Labor intensive, Marketing

I. INTRODUCTION

Ethiopia is a homeland for many spices, such as korarima (*Aframonum Korarima*), long pepper, Black cumin, white cumin, Bishops weed ('Nech azmud'), and coriander whereas turmeric is an adopted rhizome of *Curcuma longa* from abroad. Turmeric reached Ethiopia sometime during 800 AD probably from India and its systematic production on a commercial scale started only from the 1970s. Because of India's, influence turmeric has become an important ingredient of many of the common Ethiopian dishes (Peethambaran et al., 2016). Now turmeric is cultivated up to an elevation of 1700 meters above mean sea level where the southwestern part of the country is responsible for more than 76% of Ethiopia's turmeric production (Herms, 2016).

Unlike other spices, turmeric is prepared either in its dried form and/or as oleoresin or essential oils extract, thereby fetching foreign currency to the country (Mazaud et al., 2004). The harvested and cleaned rhizomes have to attain stability before they enter the market as dependable and saleable commodities. This involves a thorough postharvest treatment including boiling, drying, polishing, and grinding (Balasubramanian et al., 2016, Nair, 2019). It is strongly believed that postharvest handling and processing methods at the production level forecasted market potential for unprocessed and ground turmeric as well as its extracts such as essential oils and oleoresins (Ravindra and Venkatesh, 2016). However, the smallholder farmers in Ethiopia predominantly conduct commercial farming and selling of turmeric to local and regional traders (Masresha, 2010).

As noted by Girma et al. (2016) and Ungerer (2018) smallholder farmers in southwestern Ethiopia either bypass basic steps or practice inadequate postharvest handling at the production level of turmeric rhizomes. Lack of proper postharvest handling practices will lead to problems of the marketing system and resulting in significant wastage/spillage of the product due to quality deterioration. To overcome this problem it is important to understand the various perceptions of smallholder farmers about several aspects of postharvest handling and processing of turmeric rhizomes at the farm level. This survey was carried out in major turmeric-producing areas of the region. It deals with assessing postharvest practice at farm level, identifying problems in postharvest processing of turmeric rhizome, and qualitatively evaluates dried products collected from three districts of southwestern Ethiopia.

II. MATERIALS AND METHODS

The study was conducted in Yeki, Sheko, and Godere districts of southwestern Ethiopia Accordingly, 151 interviewees were selected by using Yamane (1967) sample size determination formulae with a 90% confidence interval and 8% margin of errors as shown below

$$n = \frac{N}{1+N(e)^2}$$
$$= \frac{5737}{1+5737(0.08)^2}$$
$$= 151$$

Where, n= sample size for the research use

N= total number of households (5737)

e = the acceptable sampling error (8%)

The results of focus group discussion, on-site observation, and face to face interviews with farmers show that HHs in the study area carried out the postharvest activities like cleaning, cooking/curing and drying at farm level.

Physicochemical Analysis: Moisture content, total ash, acid-insoluble ash, essential oil and, oleoresin were determined as per the methods described by ASTA (1968). Curcumin was quantitatively extracted by refluxing the material in alcohol and estimated spectrophotometrically at 425 nm as described in Sadasivam and Manickam (1996) and modified by Pawar et al. (2014). Each determination was carried out three times and the average values were taken for statistical analysis.

III. RESULT AND DISCUSSION

Table 1: Postharvest handling and processing Practice at producer's level

Variables	Category	Frequency (n = 151)	Percent
Harvesting stage	1) >8≤9 months	107	70.86
	2) 9≤10months	39	25.83
	3) >10 months	5	3.31
Curing	1) Traditional	136	90.07
	2) Improved	0	0.00
	3) None	15	9.93
Drying	1) Open yard	129	85.43
	2) Cement floor	7	4.64
	3) Bed	6	3.97
	4) None	9	5.96

Source: Own Survey, 2019

Table 2: Level of constraints faced turmeric postharvest activities

Constraints	Very high (5)	High (4)	Moderate (3)	Low (2)	Very low (1)	Mean	Rank
Lack of labor	140	4	3	2	2	4.84	1st
Lack of market information	41	71	15	18	6	3.81	2nd
Limited access to finance	3	3	137	5	3	2.99	3rd
Lack of technology	-	84	4	38	25	2.97	4th
Unreliable transport	-	-	16	5	130	1.25	5th

Source: Field survey, 2019

Table 3: Physicochemical quality of turmeric from different districts (dry weight basis)

Quality Parameters (%)	Study districts			Allowed range
	Yeki	Sheko	Godere	
Moisture Content	12.32±0.29[a]	11.58±0.50[b]	11.39±0.44[b]	Maximum.12*
Total Ash	10.56±0.53[b]	11.90±0.46[a]	12.53±0.34[a]	Maximum 9.0*
Acid-insoluble ash	1.80±0.07[b]	1.67±0.09[c]	1.91±0.06[a]	Maximum 2.5*
Essential oil	3.37±0.33[a]	3.29±0.33[a]	2.56±0.09[b]	Minimum 2.5*
Oleoresin	5.72±0.20[a]	5.26±0.34[b]	4.67±0.18[c]	8-10**
Curcumin	3.53±0.36[a]	2.62±0.17[b]	3.43±0.31[a]	Minimum 2**

Mean ± standard deviation of different letters are significantly different at p<0.05 across districts; *=European Spice Association, ESA(2018); **=Ethiopian Institute of Agricultural Research, ESA(2013).

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Low Power Design Efficient Fixed Width Adder Using a Replica of Fixed Width Repetition Block

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Abstract— In this paper, the area of efficiency multiplier put a sign suggests a fixed width through a replica redundancy through adoption My tolerance for noise (ANT) architecture with a multiplier of fixed width to build a redundancy version precision cutting Masa (RPR). ANT proposed architecture can meet the demand for high precision, low power consumption, and region Efficiency. RPR fixed-width design with error compensation through the circles of the possibilities and statistical analysis. use the When a partial product of the correct input vectors and vectors fixed in the palace and put in place to reduce truncation errors, hardware Failure holding circuit can be simplified compensation. The multiplier ANT 16 × 16 bits, the circuit area in our RPR fixed width It may be less, energy consumption in the design of ants can be saved as compared with the ANT state of the art design.

I. INTRODUCTION

The rapid growth of mobile and wireless systems In recent years, the need for systems pushing ultra-low energy. To reduce power dissipation, and measuring the voltage. [1] It is widely used as a technology of low energy efficient, and Power consumption in CMOS circuits game The square of the supply voltage. However, in the semi-depth micrometer process technologies, has raised the problems of noise interference Difficultyin design and efficient reliable microelectronic Systems, and therefore, design techniques to improve the noise Tolerance has developed a large scale [2] - [8]. Aggressive low energy technology, referred to as the voltage across the dimensioning (VOS), and aim to reduce the supply volt age out critical supply voltage without sacrificing productivity. However, VOS lead to a sharp deterioration in the signal to noise ratio, Ratio (SNR). My novel noise tolerant (ANT) The combination of technology VOS main block with low resolution Copy (RPR), who is struggling with software bugs effectively, while Achieve significant energy savings. Some ANT deformation The designs presented in [5] - [9] The design concept is ANT Extended system level. However, the designof RPR ANT is intended, and that is not easy Adopted and repeatedly. RPR designs

in ANT designs can work on Too fast, but the hardware complexity is also Complex as shown in Figure 1. As a result, the design RPR ANT design design is still the most popular because of its Simplicity. However, with the adoption of RPR must still pay In the additional area and power consumption. In this work, We also suggest an easy way by using a fixed-width RPR To replace the block RPR full width. The use of a fixed width RPR, a miscalculation can be corrected with low Energy consumption and low overhead region. we use Probability and statistics, and a partial analysis of the product weight Finding a company about compensation for greater accuracy RPR design. In order not to increase the critical path delay, Restricting compensation circuit in the RPR should not be Located on the critical path. As a result, we can achieve ANT is designed with the small area of the circle, low power Consumption, supply voltage and less critical

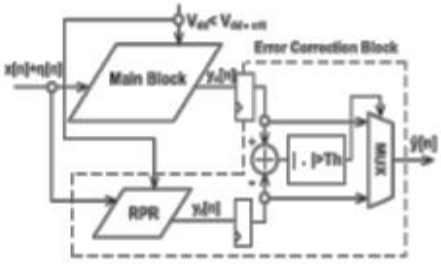


Fig. 1. ANT architecture [2].

II. ANT MULTIPLIER DESIGN PROPOSED US-ING A FIXED-WIDTH RPR

In this paper, we have proposed, and the width RPR-fixed Rip place a total width of blocks RPR ANT design [2], It is shown in Figure 2, which can not only provide thehighest Account accuracy, low power consumption, low Above the area of the RPR, but also carried out with high SNR, The effective area and the tension of the lower layer sup operation and low power consumption to achieve more ANT architecture. We demonstrate our wide design based on RPR fixed ANT multiplier. Constant width designs usually DSP applications applied to prevent the

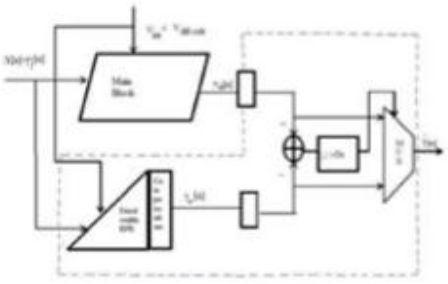


Fig.2. Proposed ANT Architecture with fixed width RPR.

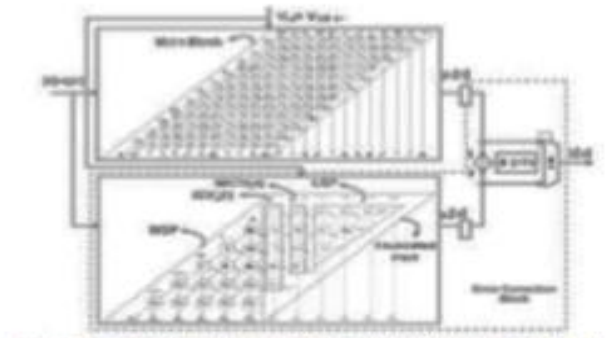
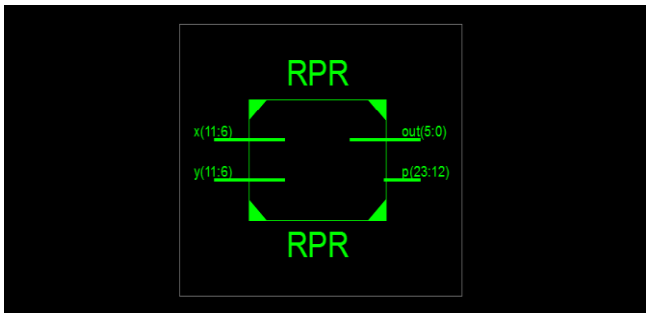


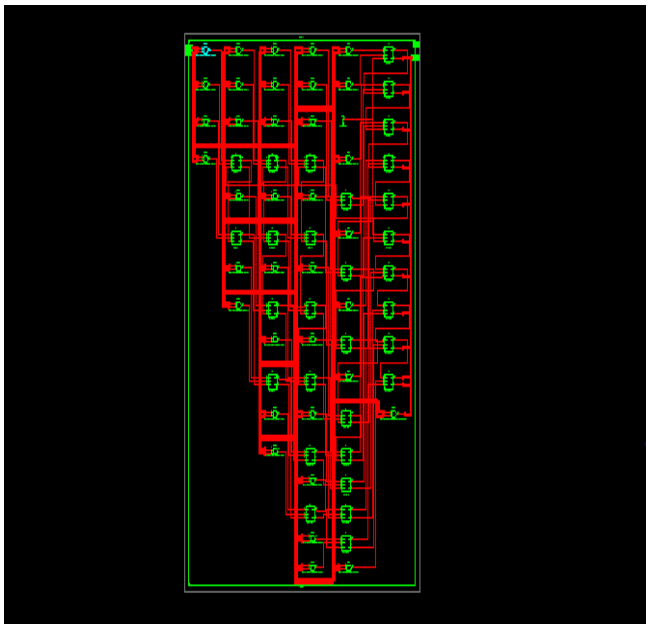
Fig.3.16 × 16 bit ANT multiplier is implemented with the 8-bit fixed width Replica redundancy block.

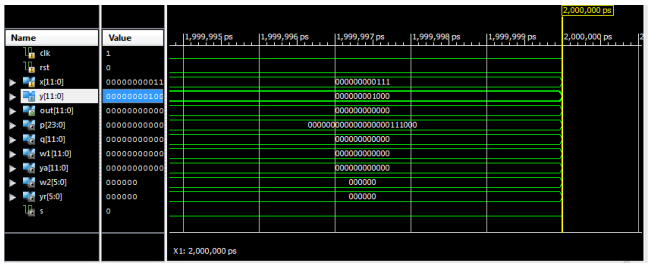
growth of countless little

To show. Court n bits least significant bit (LSB) output is popular solution for the construction of a fixed width with n bits DSP The inputs and outputs n bits. Hardware complexity and power DSP consumption of a fixed width is usually about half One full length. However,truncated LSB results pane In rounding error, you need to compensate specifically. Many of Arts offer to reduce truncation Error correction with the value of continuing with the correct variable Value. The complexity of the circuit to compensate for a fixed The corrected value can be simpler than the variable Correction value. However, approaching the correct variable Usually more accurate, method of compensation is truncation error compensation between longitudinally Multiplier and fixed-width multiplier. However, in RPR has a fixed width of the multiplier ANT, compensation A mistake we have to correct is the general truncation error MSDP mass. On the contrary, we have a method of compensation for truncation errorcompensation between longitudinally MSDP multiplier and fixed-width multiplier RPR. Currently, there are a lot of fixed width multiplier Designs applied to the complications of full width. However, there It is not yet fixed width design RPR applied to the ANT multiplexed designs. To achieve more accurate Error Compensation, which offset truncation error with variable correction value. Error building compensation circuit especially the use of terms of partial products With more weight in less than a big slice. The The algorithm error compensation benefits from the possibility, Statistics, linear regression analysis to find The approximate amount of compensation [16]. To save the hardware Complexity, partial compensation carriers Product What has the greatest weight in less than a big slice And it is injected directly into the fixed RPR offer, which does not Need more logic gates compensation [17]. For more with less Error compensation, but must also take into account the impact of Truncated with the second most important bits products Error compensation. We propose a compensation error Circuit using the simple vector corrected minor tickets He remained offset error. In order not to increase critical path delay, and we are in a position Compensation Service in noncritical path of RPR fixed width. Compared to RPR complete design introduced in [15] and proposed a fixed width RPR multiplier leads not only with high SNR but also Circuits with low area and low power consumption. An error in the static screen proposed correction vector minutes ANT design highlighted in the design, function RPR To correct the errors that occur at the start and MSDP Maintaining the SNR of the entire system during cutting supplies Aalkahrby effort. If a fixed-width RPR is used to ANT Architecture, and it went for a smaller circuit area and power Consumption, but also accelerate the speed of calculation, Compared to traditional total length of the RPR. But nevertheless, We need huge compensation truncationerror due to cut Stop many hardware elements of the MSDP LSB. At MSDP n bits ANT POV-multiplier and the Crown group, two for And it can be expressed in a signed n-bit input X and Y as he (/ 2 N) all Baugh- bit width and partial Crown unsigned product Group can be divided into four sub-groups, which are the most A large part (MSP), correct input vector [ICV (SS)].

III. RESULTS:







IV. CONCLUSION

In this paper, it is to introduce the concept of tolerance in error VLSI design. A new species of snake, and the snake error tolerant, That sells a certain amount of Milan-pastor of the importance of Save energy and improve performance, and propose. Wide comparisons with conventional digital hoses It was shown that the proposed multiplier exceeded Traditional power consumption and speed snakes Performance. Potential applications for the fall of the multiplier Especially in areas where there are no strict requirements Accuracy or where ultra-low power consumption and high speed Accuracy is more important than performance. One An example of these applications in the application of DSP portable devices such as mobile phones and laptops.

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Unmanned Petrol Bunk System Using Microcontrollers

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Abstract— Today almost all petrol pumps have a microcontroller to control the electrical pump, drive the display, measure the quantity and accordingly turn OFF the electrical pump. But still a person is required to collect the money and in addition security is also required for it. Our project is designed to eliminate this human interaction so that there is no need of workers to fill the petrol and also provides security by transmitting the information to the authorized persons.
A Smart card or RFID card is defined as any pocket-sized card with embedded integrated circuits which can process information. The present situation put up at petrol bunks is little inconvenient for the customers as it consumes more time during the money transactions and also repeatedly disputes are raising between the customers and petrol boys due to the human errors. To avoid this type of nuisance and killing time, this project work is taken up by which human involvement can be minimized and errorless output can be obtained from the machine.
In this system, all drivers have a RFID card called just like a petro card. This card can be recharged by some recharge units. The petrol pump is equipped with a RFID card reader. At the Petrol pump, the driver place the card and the RFID card reader reads the amount in the card and will display it on the LCD. The driver then enters the quantity of petrol that has to be filled using a keypad. The corresponding amount is calculated and deducted from his petro card. The electrical pump is then turned ON according to the entered amount, fills the tank and automatically turns OFF.

I. INTRODUCTION

The project work that can be considered as Smart (RFID) Card is designed as un-manned automatic petrol bunk, Smartcard based Technology is implemented in the system to avoid money transactions while filling the fuel. Smart cards are designed as re-chargeable; these cards can be charged. Presently this kind of systems are nowhere existing in our country, when these are implemented, smart cards can be charged very easily by paying money at any authorized centre. Since the system is not existing anywhere and to provide re-charging facility, re-charging unit is also constructed for live demonstration. The entire system is designed with three 8051 Microcontrollers, and a high-level program is prepared in Assembly language to make the petrol bunk as total automatic.

A smart card or RFID card is defined as any pocket-sized card with embedded integrated circuits which can process information. This implies that it can receive data from the main system when it is inserted in to the main processor and at the same time the data stored in card can be sent to the processor as an output. Generally the smart cards are used for many applications and it is denoted as ICC (Integrated Chip Card) applications. There are two broad categories of ICCs, memory cards and microprocessor cards. Memory cards contain only non-volatile memory storage components, and perhaps some specific security logic, whereas Microprocessor cards contain volatile memory and microprocessor components.

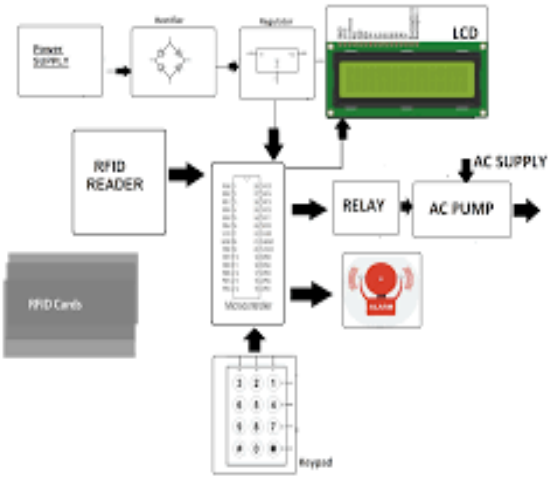
It has been said that smart cards will one day be as important as computers are today. Because smart cards are indeed tiny computers, it's difficult to predict the variety of applications that will be possible with them in the future. It's quite possible that smart cards will follow the same trend of rapid increases in processing power that computers have. Smart cards have proven to be quite useful as a transaction/authorization/identification medium in European countries. As their capabilities grow, they could become the ultimate thin client, eventually replacing all of the things we carry around in our wallets, including credit cards, licenses, cash, and even family photographs. (The photographs could be viewed and/or exchanged by capable terminals or personal computers.) By containing various identification certificates, smart cards could be used to voluntarily identify attributes of ourselves no matter where we are or to which computer network we are attached. The detailed description of the smart cards is provided in the further chapters. Now as described above, the complete working module including re-charging unit is designed with microcontroller chip, since the system is designed with so many interfacing devices like LCD panel, Keys, EEPROM, relay, buzzer etc. lot of I/O lines are required. But here the 89C51 controller is having 32 I/O lines, which is more than sufficient for interfacing all the mentioned devices. Therefore a single controller is sufficient to fulfill the task.

Everything has been digitized. In many existing systems, almost all petrol pumps have a controlling unit to perform the tasks like managing the electrical pump, drive the display, measure the flow & accordingly turn OFF the electrical pump. But still a person is required to collect the money and there is a possibility of many human errors. In this proposed petrol pump automation system, we are using RFID card to access petrol at different petrol stations of different petrol companies across the country and here.

Whenever we want to fill the tank from the fuel dispenser, we just have to place the RFID card near the RFID reader. Then the microcontroller reads the data from the RFID reader and performs the action according to the customer requirements. This digital petrol pump system also provides the security for the customers for filling petrol at the Petrol

stations by avoiding the involvement of human beings, hence reduces the risk of carrying money every time. This petrol pump system consists of Atmega328 microcontroller, RFID module, LCD display, Keypad, Ac pump and alarm. When RFID reader, reads the card it asks for the 3-digit password, if we enter wrong password more than twice it raises an alarm. And when the right password is entered is into the system, the system asks for the amount and it also shows the balance amount. On entering the amount, the motor starts and petrol gets filled in the petrol tank from the fuel dispenser.

II. DESIGN



Hardware's required are:

1) Microcontroller
2) RFID tag
3) RFID reader
4) Relay
5) LCD
6) Keypad
7) Dispensing System
8) Buzzer

When the customer comes to fill the fuel at the station, firstly he will swipe the card. If the card is authorized, RFID card reader will accept the card. Then it will ask for the pin number. If he entered pin number by the customer is correct then it will ask for the amount for the petrol to be dispensed. In such a way system works.

ADVANTAGES

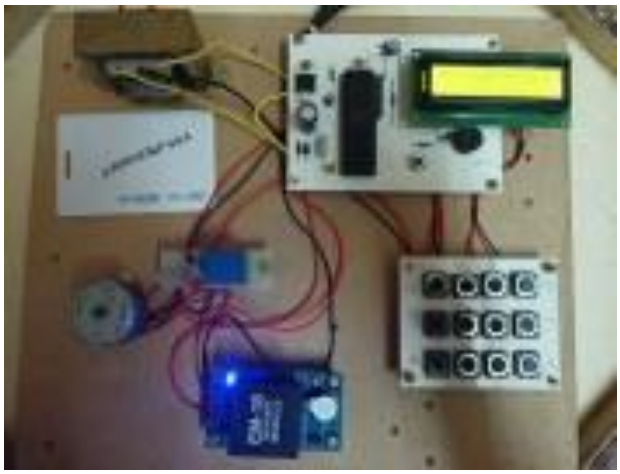
- Man power is reduced because of automated self-service.
- Due to use of RFID system robbery of the fuel is avoided.
- The time is saved.
- Low power consumption.
- Accuracy in the amount of petrol dispensed.
- Highly sensitive.

DISADVANTAGES

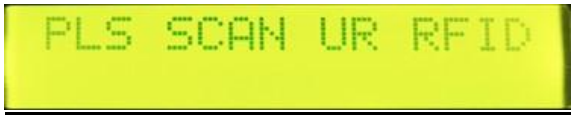
- Awareness about Unmanned Petrol Pumps.
- If network fails then whole system will collapse.

IMPLEMENTATION

Implementation of RFID technology has changed the operation of conventional fuel dispensers. The practical implementation of the system is done by oil products distribution company, Baghdad at its fuel pump. This technology can be enhanced to implement the same system for milk processing industries while distributing the milk and its products to the market. In day-to-day life we can see that water distribution in summer is also one of the problems in front of India. So, it is possible to keep control on water distribution in particular area. The rationing products like vegetable oil as well as kerosene and its sub products may be securely distributed to the customers using the same system we proposed. Also, it is possible to keep record of the distributed products in market which is commercially most important for industries.



III. RESULTS



IV. CONCLUSION

This project is meant for security systems whose access is only for respected authorities. Using a microcontroller, the petrol pump is equipped with a smart card reader/write. At the Petrol Pump, the driver swaps the card and the smart

card reader reads the amount in the card and will display it on the LCD. The driver then enters the quantity of petrol that has to be filled using a keypad. The corresponding amount is calculated & deducted from his petro card. The electrical pump is then turned ON according to the entered amount, fills the tank and automatically turns OFF. Our electronic system performed as expected. We were able to implement all the functions specified in our proposal. The biggest hurdle we had to overcome with this project was interfacing the micro controller with the hardware components. We feel that this electronic system is very marketable because it is easy to use, comparatively inexpensive due to low power consumption, and highly reliable. By using this project one can design a secured system. For filling petrol to vehicles at the petrol bunks using Smart Card based Accessing System.

V. FUTURE SCOPE

- Unmanned petrol station was required for over the years to fulfil the requirement of consumers over the wide area.
- Unmanned petrol station concept is not limited petrol station, but it can be applicable for the availability of food grades at long distinct area.
- It can make human safer from robbery, fraud, and any other unwanted incidences by the use of plastic money.

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Mathematical Modelling and Experimental Analysis of Hydro-Carbon Based MRFD

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Abstract— Magneto-Rheological nature (MR) fluids are known as smart and flexible fluids. The very important qualities of smart solutions are their reversible alters from linear-viscous liquids to semi-solids comprising manageable yield stress in bare magnetic fields. This provides elastic interface among mechanical & electronic control elements and are driven by low-voltage power supply. MR fluids are partially active devices to offer controllable damping forces, along with more attractive in practical applications. The present work aims in focusing the Hydro-Carbon based MR fluid damper characteristics. The work also involves the quantify the quality characteristics of fluids and appropriate dampers to evaluate the performance of the same by varying the parameters like force-current, force-velocity, pressure-current and pressure-velocity.

Keywords— Characterization, MR Fluid, MR Damper, Magnetic Circuit

I. INTRODUCTION

We use smart fluids in semi active damping devices as working media. By varying the application of low power control signals the properties of flow of smart fluids are changed to desired state. The characteristics of damper by using those fluids are precisely changed by sending low power signal and at the same time maintains the important ease of passive damper. MR Fluid is a new brilliant solution and the true characteristic of MRF enables to convert on its own from liquid state to semi solid and even solid state in a very short time, when it is subjected to profound magnetic field intensity, eventually the magnetic field intensity plays a vital role to enable the general operation of MR fluid and investigation of field strength of magnet which is put on MRF is essential.

Normally, to obtain the steadiness and fastness under operating time, the flux lines of magnet around the MRF must be evenly distributed as much as possible. In addition, we need to see that magnetic field must cover the complete MRF and involve in the operation so that we can expect 100 % participation of MRF Solution there by weight and cost of the device can be reduced drastically.

Design of MRF devices is at present an interesting area because of its variable features of magneto rheological solution. Enormous efforts have been made previously and shows some good characteristics of MRF, such as yield stress increasing and allowing it for use in variety of applications [1]. Dynamic characteristic of MRF using various approaches has been considered earlier [2]. New designs and methods have been developed to test the MRF devices [3]. In addition to the same, some work was carried on MRF Damper designing process [4] and device optimization [5] and patents on MRF devices are carried out [6].

II. MATHEMATICAL MODELING

2.1 MR DAMPER GEOMETRY

In the course of reciprocation of the piston solution moves circumferentially through the specified gap, i.e., clearance between the piston and cylinder. The solution cannot pass through the annulus freely since the gap is very small and strong magnetic flux lines are formed proportionally to the input current supplied and profound resistance is offered by the device. Assumptions made for MR liquid in the quasi static process. 1) Magneto Rheological Smart solution devices reciprocate with stable speed; 2) The gap or clearance is completely filled by the solution of MRF; 3) A visco plastic material procedure is adopted to predict the MR liquid response (8).

Bingham's expression is considered to study flow of MR solution through annulus:

$$\tau = c\,\gamma\,(\tau < \tau_y)$$

$$\tau = \tau_y\,(h) + \eta\,\gamma^{*}\,(\tau > \tau_y)$$

From equation (1), γ^{*} - Fluid shear rate, h – magnetic field, c – complex material modulus and η dynamic viscosity. The drop of the pressure in pressure driven flow system (PDF) is obtained by adding a portion of viscous component δP_{η} and a portion of strength in shear due to magnetic field δP_{τ}

In similar way to equation (1), the difference of high pressure and low pressure chambers of the damper can be approximated by:

$$\delta P = \delta P\eta + \delta P_{\tau} = \frac{4.3\,.\,D\,.\,l}{(gap)^{3}.b} + \frac{e.\tau_y.l}{gap}$$

Where l, gap, and b are the distance, clearance and width of the flow chann el between the fixed poles, D-Discharge of the MR liquid through annulus; n-viscosity of the liquid before application of magnetic field; □y-strength in shear

after field applied; c- is a parameter changes from 2 to 3; and λ is a ratio of pressure difference after magnetic field to the pressure difference before magnetic field applied ($\lambda = P_\tau P_\eta$);

Proposed MRFD details as follows [8]:

Below provided the basic information for the developed device is:

Top velocity of piston	= 0.195 m/s
Dead velocity of the piston	= 0.049 m/s
Movement of the piston	= 0.023 m
Inner radius of damper	= 0.02 m
Rod diameter: d_{sh}	= 0.099 m
Top running temperature	= 69∘ *C*
Shear rate: γ^*	= $1000s^{-1}$
Top field strength (magnetic): *h*	= 249 *kA/ m*
Dynamic viscosity: η	= 0.109 Pa-s
Strength in shear: τ_y	= 43.6365 kPa

There are two main stages in design process of MRFD one is Hydraulic Circuit Design (HCD) and another is Magnetic Circuit Design (MCD). These two processes are assumed as iterative calculus. The parametric calculus is as follows [8]:

The important mathematical equations which were used in the design and analysis of proposed device are:

$$a_p = \frac{\pi . \left[(d_{cyl} - 2g)^2 - d_{sh}^2 \right]}{4} \quad (3)$$

$$b = 3.142 \ (2 r_{cyl} - gap) \quad (4)$$

$$e = 2 + \frac{4.3.D.\eta}{4.3.D.\eta + 0.399.b.gap^2.\tau_y} \quad (5)$$

$$D = a_p . V_p \quad (6)$$

2.2 Details of magnetic flux lines intensity circuit:

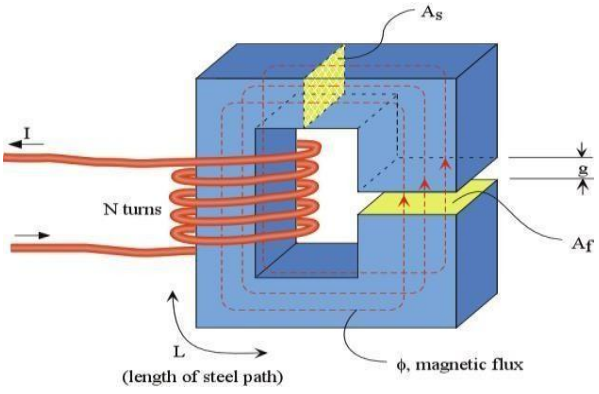

Fig 1: circuit details of magnet

The design of magnetic circuit plays a vital role since it is the key element and it governs the MR liquid to semi solid and even solid state by varying magnetic flux thereby decides the how much amount of resistance developed by the damper will be decided. The selection of damper material and design of circuit in the operating point of view, leakage of magnetic flux and loss of energy while working are very important and taken into consideration. The material used for MRFD magnetic circuit design is low carbon steel; it has excellent permeability of magnetic flux and saturation. The designed circuit must put in all MRF under magnetic field to participate in the operation so no MRF is allowed idle in the device and this is the reason circuit design plays an important role. Its impact is clearly seen in MRF device operating performance.

Design procedure for flux flow lines intensity is given below [8]:

(1) Calculation of Magnetic Flux Density, bf , to get the appropriate shear stress τ_y in the fluid

For τ_y = 43.636 X 10^3 N/mm^2, b_f = 0.799 T

(2) Calculation of Magnetic Field Strength h_f, in the gap between piston and cylinder i.e., in the fluid.

For bf = 0.799 T, h f = 249 X 10^3 A/m

(3) Complete Magnetic Flux Density is determined from $\theta = b_f a_f$. Where a_f active area of the pole combining the fringe flux lines of magnet. The flux density of magnet b_s in the structural steel material is written as:

$$b_s = \theta / a_s = b_f . a_f / a_s$$

a_f = 1.396 X 10^{-3} m^2, a_s = 1.332 X 10^{-3} m^2 and b_s = 0.7998 T

(4) To determine field strength of magnet h_s in structural steel using

if b_s = 0.7998 T, h_s = 0.44 X 10^3 A/m

(5) From law of Kirchoffs's, the appropriate number of Ampere turns (n_i) is:

$$ni = \sum h_i l_i = h_f g + h_s l$$

Where, "l" is steel path length; ni is determined as 282 Ampere turns consider "i" equals 2.1 Amps, obtained n = 142

Below figure shows the detailed longitudinal sectional view of the device been designed and manufactured for testing its accomplishment and to draw the analogy with theoretical results.

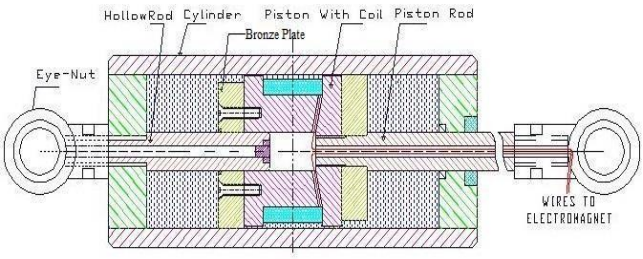

Fig. 2: Sectional view of the developed device (Courtesy [8])

III. EXPERIMENTAL SETUP

After being synthesized, i.e. MRF-I (40% by volume of iron particles) and MRF-II (36% by volume of iron particles) are poured carefully into the devices brought from Lord's Corporation, USA, and after installation in the set-up complete investigation was made at research and development lab available in Muffakham Jah College of Engineering and Technology, Hyderabad. It consists of a damper, hydraulic system, sensors, data acquisition system and power supply. A brief description of each is presented in the subsequent paragraphs [7].

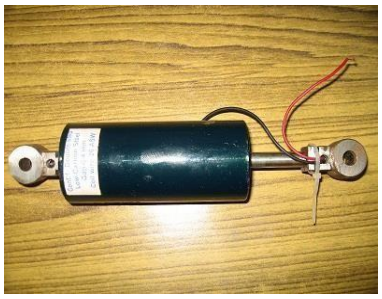

Fig.3: MRF Damper

The details of the experimental setup are shown in figure 4. The description of the equipment used for testing is discussed as follows:

Hydraulic system: The damper is driven by an actuator configured with two 10-gpm Moog servo valves with a bandwidth of 60 Hz. The actuator has a 50 mm diameter cylinder and a 40 mm stroke and is fitted with low-friction Teflon seals to reduce nonlinear effects and it was built by Denison Hydraulics India Limited, Hyderabad. The actuator is controlled by a servo-hydraulic controller in displacement feedback mode. The maximum speed under this configuration was 20 cm/sec.

Sensors: A position sensor, manufactured by OPKON (Model LPT), was employed to measure the damper displacement. The position sensor has a full range of 1000 mm displacement, speed of 2 m/s and repeatability □

0.05%. A load cell of tension and compression type, made by OIML and rated at 20 KN, was used to measure the damper resisting force. The input current going into the MR damper coils was measured by a Tektronix current probe with a sensitivity of 100 mV/A. The pressure difference on either side of the damper piston was measured by two pressure transmitters, made by SPY, have a maximum range of 200 bars. Additionally, a Fluke 80T-IR infrared temperature probe with a sensitivity of 1 mV/°C was utilized to monitor the damper temperature during the experiment.

Fig.4: Experimental setup of MRF damper (Courtesy [8])

Data acquisition: It is an electronic device that records information with a built-in sensor or via external instruments. It has maximum 8 inputs, made by AMBETRONICS is used for information obtaining and examination of device.

Power Supply: An adjustable interrupted energy unit is used to supply direct current with maximum extent of 1.9 Ampere is to be given directly to the MR Device coils for testing in the laboratory (Quasi-Static testing)

IV. RESULTS & DISCUSSIONS

As revealed above pressure-velocity & force and changeable input current achieved tests were conducted by means of the setup revealed above to examine the performance of the synthesized MR fluids. In the experimentation, velocities of 0.00, 0.05, 0.1, 0.15 and 0.2 m/s were employed. The input current to the damper coil was kept constant at 0, 0.5, 1, 1.5 and 2 A respectively.

Force & Pressure-Velocity Behavior: The deliberated force-velocity activities of the synthesized MR fluids at a variety of constant input current stages are plotted and shown in figure 5.

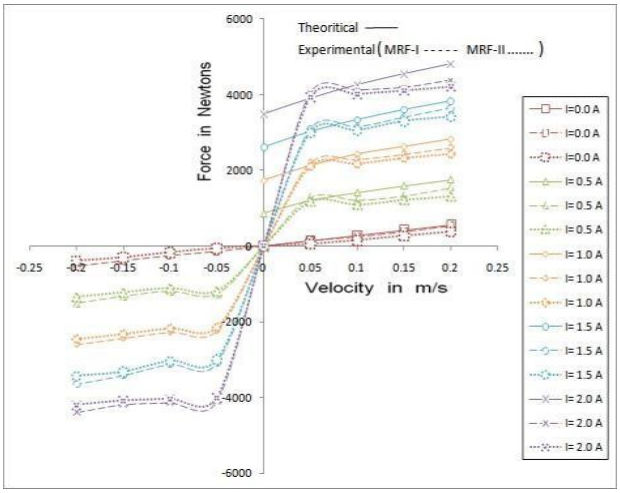

Fig.5: Force - Velocity

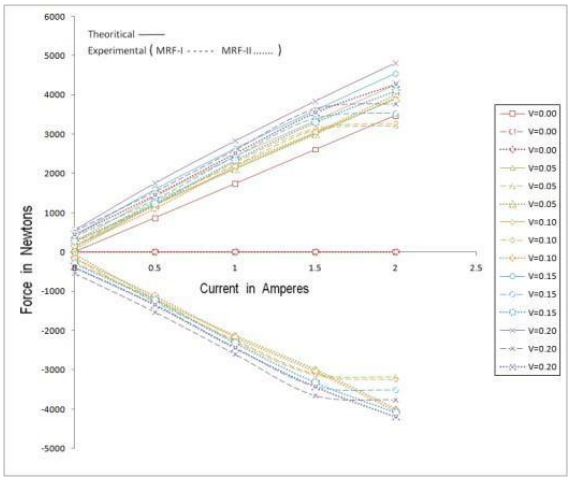

Fig.6: Force – Current

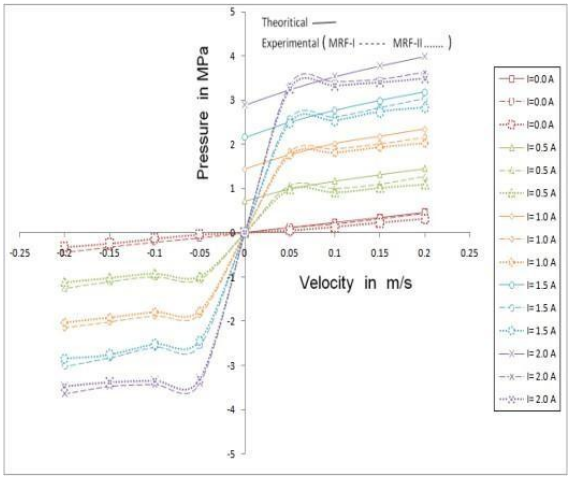

Fig.7: Pressure - Velocity

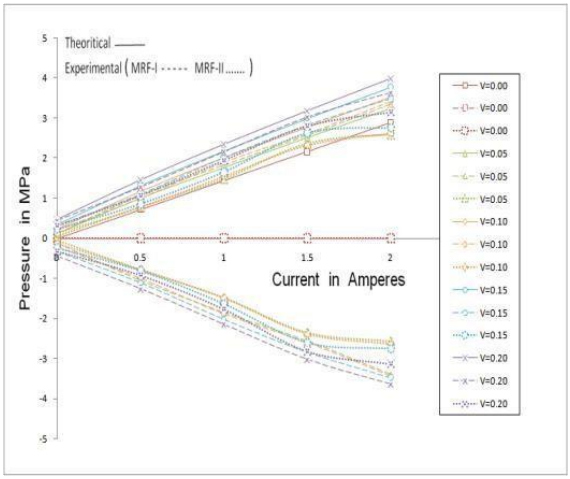

Fig.8: Pressure - Current

V. CONCLUSION

It has been noticed that, the MRF device resisting force is extremely sensitive to the damper input current `rather than the piston speed. Saturation of both the magnetic fluids (MRF-I & MRF-II) occurs at 1.5 Ampere input current. The saturation starts for both the fluids at 1.5 Ampere but MRF-I saturates rapidly compared to the MRF-II.

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Seismic Response of RC Building Frame Resting on Sloping Ground Using Base Isolation - A Review

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Abstract— Earthquake forces are unpredictable and random in nature; the dynamic and static analysis of structure have become the primary concern for civil engineers. Buildings constructed on hills shows different structural configurations in comparison with buildings constructed on plain grounds. Since the columns are of different heights hence, they grab large amount of shear forces and torsional moments and show uneven distribution. If these structures are subjected to earthquake, then it became more vulnerable in sever intensity zone. In this paper a brief literature survey is done on buildings in hilly areas with base isolator and fixed base buildings. The present study makes an attempt to understand the effect of earthquake load on building frame on sloping ground with base isolation at different levels of building and without base isolation under sever intensity zone for safety of these structures and to promote the growth of construction technology in hilly areas by using ETABS Software for linear dynamic analysis. Based on the literature review, it was concluded that Base isolation decouple the structure from its foundation and allow the building to behave more flexibly which improves its response to an earthquake, therefore it reduces the base shear and story acceleration and increases the displacement, story drift and time period.

Keywords— Sloping Ground, Structural Configuration, Base Isolation, Seismic Behavior

I. INTRODUCTION

In the several regions of the world, sloping areas are highly susceptible to earthquake, e.g., northeast part of India. The lack of flat land in hilly areas forces development on sloping land. Hill buildings made of masonry with mud mortar or cement mortar that are not in accordance with the provisions of the Earthquake Law are dangerous and result in loss of life and property in the event of an earthquake. Due to economic upswing population density in hilly areas has increased rapidly. Therefore, there is demand for building multi-story buildings on the hills. The behavior of a building during an earthquake is highly dependent on its mass and stiffness. The lack of normal land in the hill forces construction activities on sloping terrain therefore it causes different important buildings like as hospitals, hotels, school, and colleges resting on slopes. Building can collapse due to the different story of the building step back to the hillside. The buildings become very irregular and asymmetrical due to the different configurations of the buildings on hills, on each floor due to the difference in mass distribution and stiffness along the different vertical axes. Such constructions in areas that are prone to earthquakes experience greater shear and torsion compared to conventional constructions.

II. PROBLEMS ON SLOPING GROUND

Hilly area is more prone to seismic activity:

That is in northeast region of India, buildings situated on hill slopes are generally irregular and torsionally coupled and hence, susceptible to severe damage when affected by earthquake ground motion. Reference [1] determines that in seismic analysis, it is usually assumed that the motion which takes place during an earthquake has one principal direction [1]. Therefore, a well designed structure should be capable of resisting destructive earthquake energy reching it from ant possible direction [1].

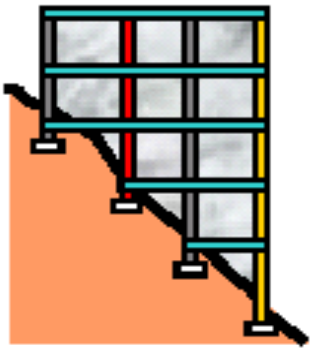

Fig. 1: Building on sloping ground have long and short column which may twist during earthquake [8].

Unsymmetrical configuration:

Buildings with unequal structural member and where mass is not distributed uniformly, twist about a vertical axis and displaced horizontally and perform poorly when shaken at a ground level. Reference [4] states that the north and northeastern part of India have large scale of hilly terrain, which are categorized under seismic zone IV and V. In this region multistory RC framed building has a popular and pressing demand, due to its economic growth and rapid urbanization [4].

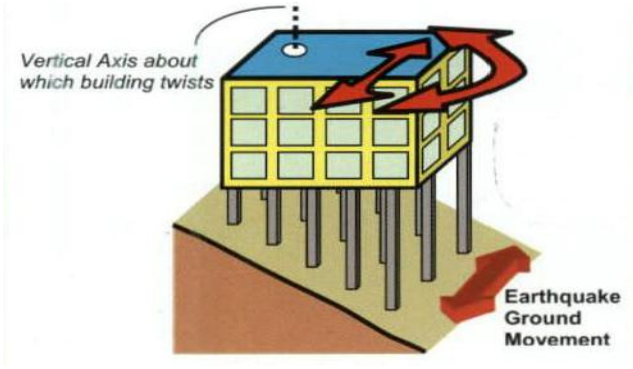

Fig. 2: Torsional behavior of building on sloping ground [8].

Short columns effect:

Reference [1] determines that due to site conditions buildings on hills slopes are characterized by unequal columns heights which results in variation of columns stiffness [1]. It is observed that a short column would be stiffer than the longer one of same cross-sectional area. For vertical load it may not be susceptible to buckling, and hence capable of receiving higher loads [1].

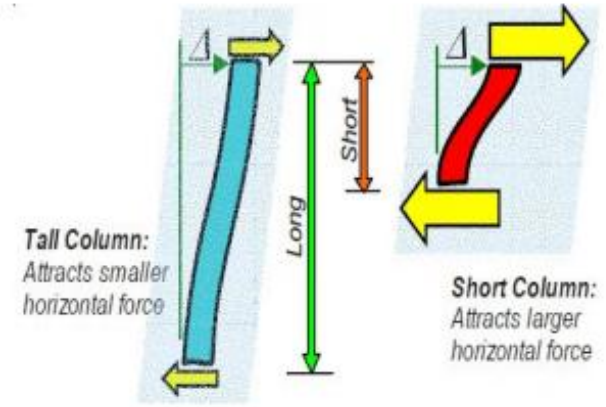

Fig. 3: Short columns are stiffer and attracts large forces during earthquake [8].

Previous work on seismic response of RC framed building resting on sloping ground

In reinforced concrete buildings to increase PGA capacity and to provide strength, *buckling* restrain braces are very effective. As the number of braces increases the PGA capacity also increases [2] . Intensity of seismic excitation and properties of buildings are responsible for the performance of isolated buildings. So, the service load and extreme load subjected on base isolated buildings and torsional effects are investigated [1]. Under low power excitation the performance of isolated buildings can be improved by proper adjustment of mechanical properties like damping and stiffness [1] . Reinforced concrete columns jackets and eccentric steel bracing, these two retrofitting techniques are introduced to enhance the seismic behavior and performance of structure [7]. To reduce deformation and damaging effect during earthquake base isolations techniques are used [3]. The flexibility of structure got improved by introducing isolators. In terms of seismic parameters such as story drift, base shear, displacement, and in exterior and interior of columns the maximum forces [3]. In comparison with fixed base building the story displacement increases, on the other hand inter story drift and base shear decreases due to addition of base isolators [3]. According to reference [5] The response spectrum method with 3-D analysis is used. With respect to the appropriate building configuration on slopes the properties of a dynamic analysis are checked [5]. Conclusions are: The step back buildings during seismic excitation may be more susceptible than other building configurations [5]. The torsion development of step back-set back buildings is lower than in step-back buildings. Hence the steps back-set back building was less susceptible than the step back building during earthquake [5]. The Step back Set back buildings attract more force than Set-back configuration on flat ground, the macroeconomic costs associated with levelling and sloping, and other related issues need to be studied carefully [5].

III. BASE ISOLATION

Base isolation is a device which increases the flexibility and reduces the stiffness of the structure [6]. It is also known as seismic base disconnector and one of the popular techniques to improve the safety of structure against earthquake forces [6]. Different base isolation devices are lead rubber bearing, sliding base isolation system, friction pendulum bearing and spherical sliding bearing [6]. The base isolation device is provided in between the foundation and superstructure of the building to reduce the interaction between the structure and the ground so, the energy induced by earthquake is not transmitted up through the building. Reference [3] determines that the fixed base building has zero displacement at the base of building whereas, base isolated building model shows considerable amount of lateral displacement at base [3]. Also, it has been observed that as floor height increases, lateral displacement increases in fixed base building as compared to base isolated building [3].

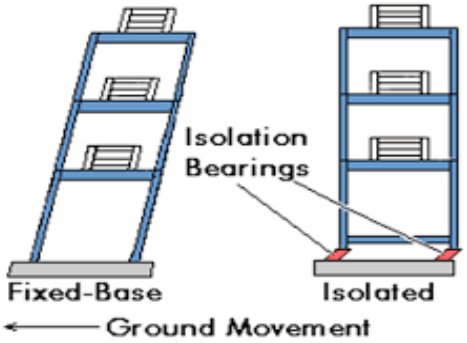

Fig.4: Building with fixed base and with base isolation [9].

Table I: Base isolation mechanism.

1.	Building location	Sloping ground with varying sloping angles
2.	System	Base isolation
3.	Basic concept	Increase flexibility and decrease stiffness.
4.	Location of device	Plinth level and above columns
5.	Advantages	Lengthen period and reduce spectral acceleration and base shear
6.	Cost	Expensive

IV. DISCUSSION

After carrying out a brief literature survey, following points are observed:

- By providing base isolation devices, the base shear, acceleration reduces, and the time period increases.
- By adjusting the mechanical properties, such as stiffness, the performance of base isolated buildings can be improved under low power excitation.
- Due to presence of base isolator the inter story drift and base shear observed to be reduced and story displacement is increases as compared to fixed base structure.
- Base isolation system increases the structures stability against earthquake.

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Comparison of 32-bit Vedic Multiplier with Conventional Array Multiplier

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Abstract— This project presents implementation of 32-bit vedic multiplier using ancient vedic sutra named 'Urdhva Tiryagbhyam'. In this project, two types of adders are used, one is the 'Kogge-Stone' parallel prefix adder and the other one is ripple carry adder. Also, implementation of a conventional Array Multiplier using both the parallel prefix adder and ripple carry adder is performed. Finally, results of all these modules are compared to prove that vedic multiplier outputs less delay than the other modules when it is implemented using parallel prefix adder. The proposed algorithm is developed using verilog HDL and implementation has been done using Xilinx 14.7.

Keywords— Array Multiplier, Kogge-Stone adder, Ripple carry adder, Urdhva Tiryagbhyam Sutra, Vedic Multiplier

I. INTRODUCTION

Due to the ever-growing advancements in technology, need for high-speed processors is increasing day by day. To achieve this, multipliers used in the system should work with more speed. Since multiplication is an important fundamental operation in all mathematical computations, it decides the execution time of the system. While implementing systems with multipliers which are designed using conventional adders like ripple carry adder, carry look-ahead adder etc., speed of the operation is not achieving the desired level. In order to improve the digital processing techniques high speed operations are required.

Vedic multiplier is the fastest and efficient multiplier which can improve the operating speed of digital processing techniques. This can be implemented using ancient vedic sutras. There are totally sixteen number of ancient vedic sutras, out of those "Urdhva-Tiryagbhyam" is the fastest and efficient sutra for mathematical operations. Kogge-stone parallel prefix adder is used in this paper for implementing both vedic multiplier and array multiplier. It is preferred because of its lower fan-out.

This paper presents implementation and comparison of 32-bit vedic multiplier with conventional array multiplier. In this paper, section II presents literature survey which has been done for this project i.e., about vedic multiplier, Urdhva-Tiryagbhyam sutra and kogge-stone parallel prefix adder. Section III deals with the proposed method for comparison of vedic multiplier and array multiplier. Section IV presents results and comparison of both vedic multiplier and array multiplier. Conclusion and references are mentioned followed by section IV.

II. LITERATURE SURVEY

A. Vedic multiplier

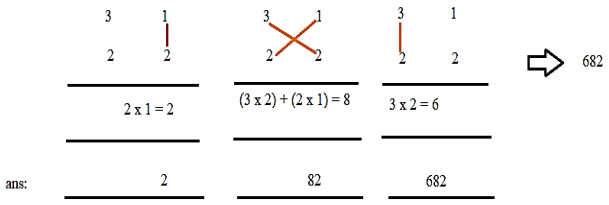
Vedic mathematics - a gift given to this world by the ancient sages of India. A system which is far simpler and more enjoyable than modern mathematics. The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge [1].

The Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras are used for the multiplication of two numbers in the decimal number system. Here, we apply the similar thoughts to the binary number system to build the proposed algorithm [2]. It works based on ancient vedic sutras. "Urdhva-Tiryagbhyam" is the efficient vedic sutra used for implementing vedic multiplier.

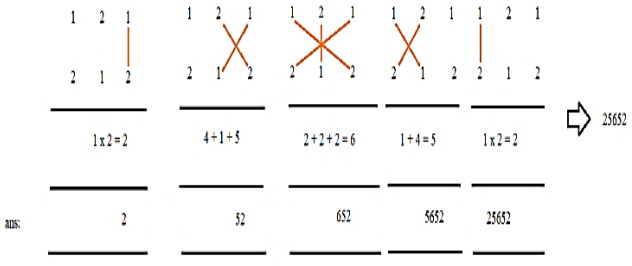
B. Urdhva-Tiryagbhyam sutra

Urdhva–Tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means "Vertically and cross wise" [3].

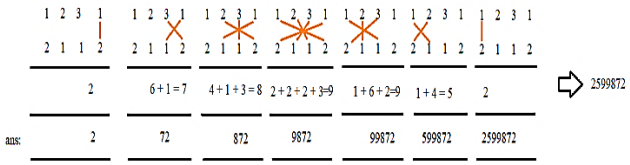
i. Two-digit multiplication:



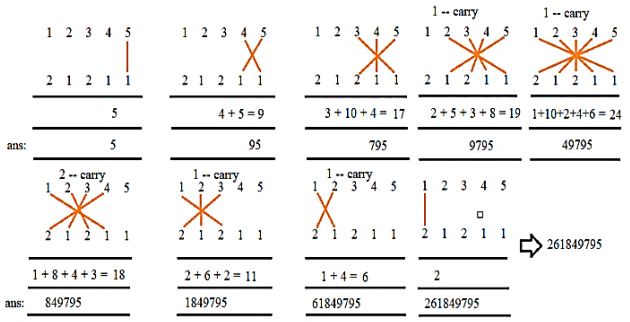
ii. Three-digit multiplication:



iii. Four-digit multiplication:



iv. Five-digit multiplication:



C. Kogge-stone adder

In computing, the Kogge–Stone adder (KSA or KS) is a parallel prefix form carry look-ahead adder. The Kogge–Stone adder takes more area to implement than the Brent–Kung adder, but has a lower fan-out at each stage, which increases performance for typical CMOS process nodes [4].

Kogge-stone adder operation is carried out in three steps. They are:

a. Pre-processing: In this stage, both carry propagated and carry generated are computed. Formulas for both the carries are as follows,

$$Pi = Ai \text{ xor } Bi$$

$$Gi = Ai \text{ and } Bi$$

b. Carry generation network: Carry generation is the second stage of the KSA. At this stage the carries of all the bits are generated separately for each bit. They are divided into smaller pieces and this overall process is carried out in parallel for all the bits. Carry generate and Carry propagate bits are used as intermediate signals and their logical equations are given as follows [5]:

$$CPi = Pi \text{ and } Piprev$$

$$GPi = (Pi \text{ and } Giprev) \text{ or } Gi$$

c. Post Processing stage: In this stage, summation of all the bits is performed. It includes formula mentioned below,

$$Si = Pi \text{ xor } Ci\text{-}1$$

III. PROPOSED METHOD FOR COMPARISON

In this paper, comparison is performed between vedic multiplier and array multiplier. Both of the operations are explained below:

A. Array Multiplier:

Conventional array multiplier is designed by using AND gates, full adders and half adders. It cannot be implemented by taking instance of modules lesser than it. For example, for the implementation of an 8-bit array multiplier, using instance of 4-bit multipliers is not encouraged because it is very difficult to implement it may not give accurate results, so that entire logic diagram has to be designed for 8-bit array multiplier. Similarly for any number of bit array multiplier, no multiplier instance will be supported, entire logic diagram has to be designed and implemented using the HDL language. Simply, it can be said that there is no shortcut for designing higher bit array multiplier. This type of implementation is very difficult when implementing higher bit multipliers in practical.

For the reasons mentioned above, logic diagram for 2-bit, 4-bit, 8-bit, 16-bit and 32-bit array multipliers is separately designed and implemented using verilog HDL. All the above-mentioned array multipliers employed with two different types of adders. Firstly, full adders and half adders are used along with AND gates for the implementation. Secondly, kogge-stone parallel prefix adder is replaced in place of full adder. Now, for this 32-bit implementation and comparison two modules are completed. Delays of these modules also noted.

B. Vedic multiplier:

In order to reduce the delay obtained in array multiplier, vedic multiplier is implemented in this step. Unlike array multiplier vedic multiplier can be implemented with instances of other modules. For example, for designing 8-bit vedic multiplier four 4-bit multipliers can be used which reduces delay as well as design complexity. 4-bit, 8-bit 16-bit and 32-bit vedic multipliers are designed by taking instances of other multipliers. All these multipliers are implemented using verilog HDL. Vedic multiplier also employed with two types of adders same as array multiplier. Firstly, with ripple carry adder (RCA – designed with full adders) and secondly with kogge-stone parallel prefix adder. Remaining two vedic multiplier modules are done in this step. Also, those delays are noted. Now, all the modules required for this paper are ready for comparison.

Let's discuss how vedic multiplier is designed in this paper.

❖ VEDIC MULTIPLIER OPERATION

In the implementation of vedic multiplier, different bits of adders will be used for the addition of partial products generated by multiplier blocks. For a 32-bit multiplier which outputs 64-bit product, one 32-bit adder and two 48-bit adders are required which increases delay and also design complexity.

To reduce this complexity, in this paper 32-bit vedic multiplier is employed with four 16-bit adders. Block diagram of 32-bit vedic multiplier is shown below:

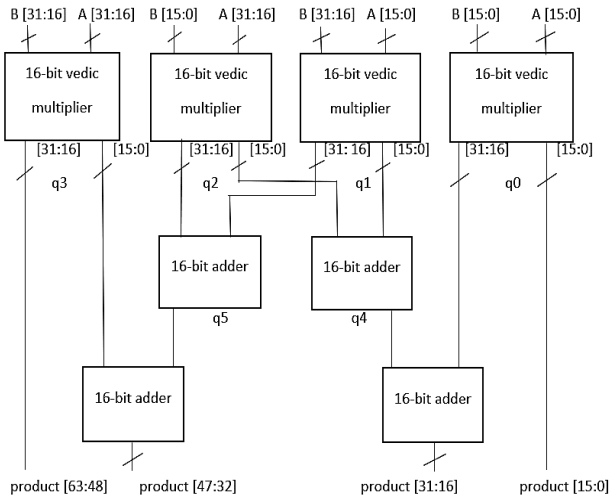


Fig: Block diagram of 32-bit vedic multiplier

As observed in the above block diagram, in place of adder blocks, RCA and kogge-stone adders are replaced for the implementation of different modules required in this paper.

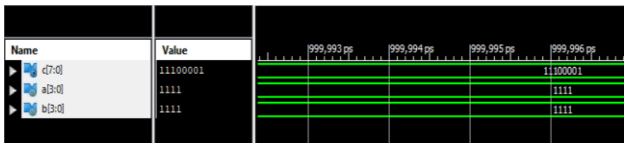
IV. RESULTS AND COMPARISON

A. Simulation results

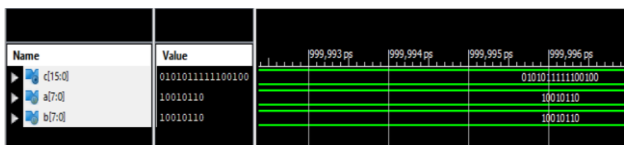
All the four modules i.e., array multiplier with full adders, array multiplier with kogge-stone adder, vedic multiplier with RCA (designed using full adders) and vedic multiplier with kogge-stone adder are tested with similar inputs to test the correctness of output. Each module outputs exact results. Hence, simulation results of 2-bit, 4-bit, 8-bit, 16-bit and 32-bit vedic multipliers implemented by using kogge-stone adder are shown below.

i. 2-bit Vedic multiplier

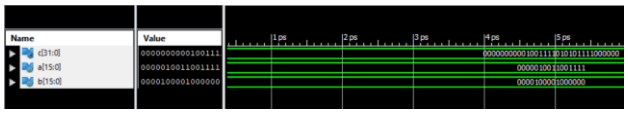
ii. 4-bit Vedic multiplier



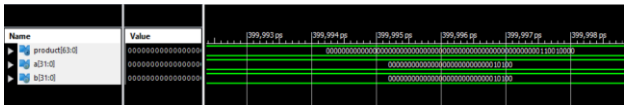
iii. 8-bit Vedic multiplier



iv. 16-bit Vedic multiplier



v. 32-bit Vedic multiplier



B. Results comparison table

Time delays of all the four modules which are mentioned above in simulation results are noted and displayed for comparison in the table below.

Bit size	Array Multiplier using Full Adders	Vedic Multiplier using RCA	Array Multiplier using Kogge-stone adder	Vedic Multiplier using Kogge-stone adder
4-bit	3.848 ns	2.683 ns	4.144 ns	3.188 ns
8-bit	9.785 ns	7.365 ns	10.387 ns	5.840 ns
16-bit	19.697 ns	12.088 ns	20.701 ns	9.540 ns
32-bit	31.594 ns	24.467 ns	32.157 ns	15.154 ns

V. CONCLUSION

With the above experiment on comparison of 32-bit vedic multiplier with the conventional array multiplier, it is proved that vedic multiplier implemented using kogge-stone parallel prefix adder gives less delay compared to remaining modules in this paper.

As observed in the results comparison table, for the 2-bit multiplication, vedic multiplier outputs little more delay than array multiplier, but while increasing the bit size of input numbers vedic multiplier outputs less delay compared to array multiplier. This method of designing vedic multiplier helps in reduction of design complexity. Vedic multiplier can be used in many digital circuits.

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Efficient Intelligent Controller for Heat Exchanger System

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Abstract— Heat exchanger system is generally used in chemical processing industries as it can withstand high ranges of temperature and pressure conditions. The major application of a heat exchanger system is to transfer fluid of hot temperature to cooler temperatures, so that the temperature control of fluid at the outlet valve is the primary objective. This mechanism can be implemented through conventional PID controller, but it has many inherent disadvantages. Inorder to overcome these disadvantages, a soft computing technique, the Fuzzy controller is being proposed. In this work, the main purpose of this controller design is to attain a uniform temperature at the output valve (tube end) of the heat exchanger system by adjusting the liquid flow rate at the input valve for a specified range. To further improve the performance characteristics of the heat exchanger processes, conventional controllers like PI, PID can be employed and the intelligent controller called fuzzy logic controller (FLC) is being employed for the comparative analysis with the conventional controllers.

Keywords— Heat Exchanger System, FLC, fluid temperature, PID controller

I. INTRODUCTION

Heat exchanger system (HES) is generally employed in chemical processing industries as it can withstand high ranges of temperature and pressure conditions. Different types of HE plants are being employed in industrial applications. But most of the industries are based on two types, they are, shell and tube heat exchanger type plants. In this work, the comparative performance analysis of conventional and intelligent controllers has been carried out for a typical heat exchanger plant [1]. The main objective of the introduced intelligent controller in this work is to control and maintain the temperature of the liquid solution at the outlet valve of a shell and as well as tube HE unit to a desired value. Unit step response has been observed for different controllers. It is being observed that the fuzzy logic controller (FLC) provides improved performance and overcomes the disadvantages offered by the conventional controller.

Typical real-time chemical processing unit consists of a chemical reactor and a 'shell and tube' heat exchanger system. The boiler of the system produces super-heated steam and flows through the tubes. Whereas, the process liquid solution always flow through the valves of the 'shell and tube' heat exchanger unit [9]. The output of the chemical reactor, i.e., process liquid solution is stored in the tank (termed as storage tank in case of gas, chemical plants). This storage tank further processes the liquid solution to the heat exchanger unit. The heat exchanger unit heats up the liquid solution to a required (as specified by the designer) set point temperature with the help of super-heated steam being supplied from the boiler. The storage tank processes the liquid solution to the heat exchanger using a pump and a non-returning valve. Then the steam is forced from the boiler and flows through the tubes, whereas, the process liquid solution flows through the shells of the shell and tube heat exchanger unit.

Depending up on the requirements and desired values for the HES, few assumptions and approximations have been made in this work. The first is that the inflow rate and the outflow rate of liquid solution are assumed to be the same; with this the liquid solution level can be maintained at a required value in the heat exchanger unit and the second is the heat storage capability of the insulating wall is assumed to be negligible [6].Two different types of disturbances in this process are being considered for effective analysis of HES, one is the flow variation of input liquid solution (assumed to be dominant) and the second is the temperature variation (most undesired thing) of input liquid solution. The sensing element, i.e., 'thermocouple' is employed along the feedback path of the control architecture. The thermocouple is used to measure the temperature at the valve of the outgoing liquid solution and further the output of the thermocouple is sent to the transmitter circuit, which simultaneously converts the temperature recorded by the thermocouple to a standardized signal in the specified range of 4-20mA by the designer.

Fig.1 shows the feedback control scheme adopted in heat exchanger system.

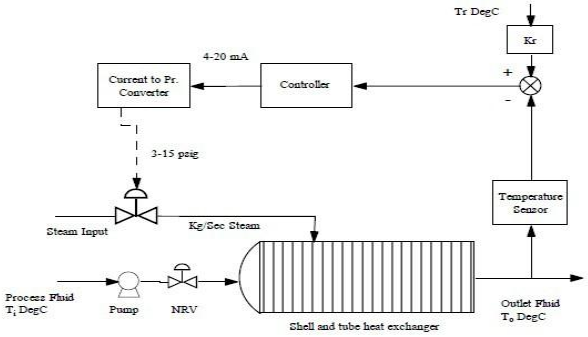

Fig.1 Overview of heat exchanger plant

II. METHODOLOGY

Mathematical Modelling With PID Control Action

The characteristic equation 1+ G(s) H(s) = 0 in this case is obtained as below:

$$900s^3 + 420s^2 + 43s + 0.78K_c + 1 = 0 \quad (1)$$

Applying Routh-Hurwitz stability criterion in the above equation gives

$K_c = 24.44$

Auxiliary equation is,

$$420s^2 + 0.78K_c + 1 = 0 \quad (2)$$

Substituting $s = j\omega$ gives $\omega = 0.218$ and $T = 28.82$

In general, ideal PID controller in continuous time is given as shown in eq.(3)

$$Y(t) = K_p\left(e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{de(t)}{dt}\right) \quad (3)$$

Laplace domain representation of ideal PID controller in eq.(3) is given by

$$G_c(s) = \frac{Y(s)}{E(s)} = K_p\left(1 + \frac{1}{T_i s} + T_d s\right) \quad (4)$$

Internal model controller (IMC) provides sophisticated tuning and design based on PI or PID controllers by matching with very low-dimensional model. Majorly, IMC depends on complexity associated with the model and the approximated performance requirements as designated by the designer [5].

The below table gives experimental tuning rules based on closed loop oscillation method:

Type of Controller	K_p	T_i	T_d
P	$0.5K_c$	∞	0
PI	$0.45K_c$	0.83T	0
PID	$0.6K_c$	0.5T	0.125T

Table 1: Typical controller constants of HES

For a PID controller, the values of parameters obtained using Zeigler Nichols based tuning methods are obtained as$K_p = 14.66$, $T_i = 14.41$, and$T_d = 3.60$.

Generally, the initial design values of PID controller calculated by all means needed to be adjusted/tuned repeatedly through the computer simulation softwares until the closed loop system response is nearer or nearly equal to the desired value. These adjustments are done in MATLAB simulation. The disturbance input introduces error in the system performance. In most of the systems, the disturbance can be estimated and its effect can be eliminated with the help of feed forward controller before it can change the output of the system or affect any other parameter of the system.

$$G_p(s) = \frac{5e^{-s}}{90s^2 + 33s + 1},\ G_d(s) = \frac{1}{30s+1}$$

The transfer function of the feed-forward controller can be given by

$$G_{cf}(s) = \frac{-G_d(s)}{G_p(s)} \quad (5)$$

$$G_{cf}(s) = \frac{-18s^2 - 6.6s - 0.2}{30*l + (30+l) + 1} \quad (6)$$

Here, *l* is the filter parameter. Its range is from 0 to 1.

Fuzzy Logic Controller (FLC)

Fuzzy logic theory is an extended theory of binary logic. As it is well-known that the binary logic is only limited to '0' and '1', the fuzzy logic can be extended in between the values of '0' and '1'. For example: in binary we deal with straight 'yes' or 'no' where 'yes is mapped to 1' and 'no is mapped to 0', whereas in fuzzy logic, we can still consider the variables as 'may be', 'may not be', 'not sure', 'nearly 0', 'nearly 1' and so on. Hence, fuzzy logic theory offers wide range of approximations and is being used on of the advanced intelligent tool in many applications.

The word fuzzy refers to the statements or assumptions which are not clear, incomplete, confusing, twisted, and invalid. Any event, process, or function that is changing continuously with reference to time, cannot be defined as either true or false, which means that we need to define such activities in a fuzzy manner [4].

Fuzzy Logic completely resembles the human decision-making methodology. It deals with vague and imprecise and incomplete information. This is gross oversimplification of the real-world problems and based on degrees of truth rather than usual true/false or 1/0 like Boolean/binary logic. In other words, we can say that fuzzy logic is not logic that is fuzzy, but logic that is used to describe fuzziness.

A fuzzy controller can include empirical rules, that are called Rule base (decision making), and that is especially useful in operator controlled plants.

Block Diagram of Fuzzy Logic:

The primary concept of fuzzy control in industrial applications is to simulate a human expert who can be able to control the system by translating the linguistic control rules into fuzzy set theory. A fuzzy logic controller can include empirical rules that are called a rule base also called as knowledge base or decision making and that is especially useful in operator controlled plants. The block fuzzification converts each piece of input data to degrees of membership by lookup in one or several membership functions [2]-[3].

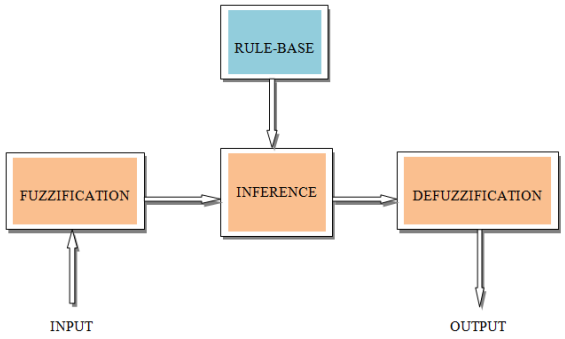

Fig.2. Block diagram of fuzzy logic control

The resulting fuzzy set must then be converted to a number that can be sent to the process flow as a control signal. This mechanism is called defuzzification. There are many types of defuzzification methods. In case the output is defined on standard universe this must be scaled to engineering units. The fuzzy controllers were designed using experimental data obtained from many simulation experiments for various choices of classical 'PID, PI, and P controllers' parameters respectively.

III. RESULTS & DISCUSSION

A. Heat Exchanger System without Controller

Simulink model:

According to the specifications of HE system, the transfer function relating all the variables is formulated. Five transfer functions are framed covering the subsystems (sub-blocks) like valve, process, thermocouple, flow disturbance and temperature disturbance respectively. Here, in this work, we present the performance characteristics of the heat exchanger plant in terms of time domain specifications like peak time, settling time and overshoot without any controller, with internal model controller and fuzzy logic controller and to validate the results, a comparative analysis has been carried out to justify the performance of fuzzy logic controller.

Fig.3 shows the MATLAB simulink model of the plant without controller.

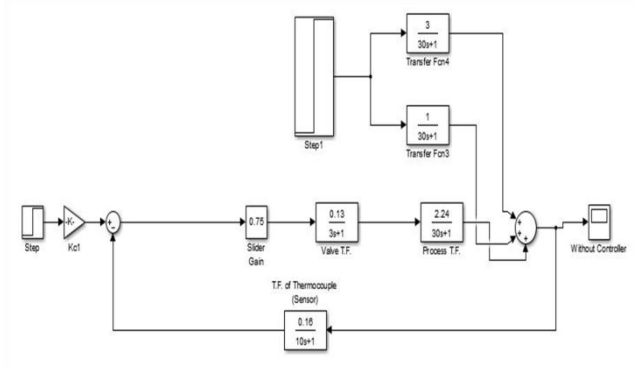

Fig.3. Simulink model of heat exchanger system without controller

Fig.4 shows the time response of the heat exchanger system without any controller. On looking at the response, the peak overshoot is calculated to be 15%, settling time being measured as 102sec and peak time is observed as 33sec. As the major challenging work of this is to regulate the temperature of the outgoing liquid solution in a shortest settling time and minimum or no overshoot, the heat exchanger system is further processed with IMC controller and PID controller.

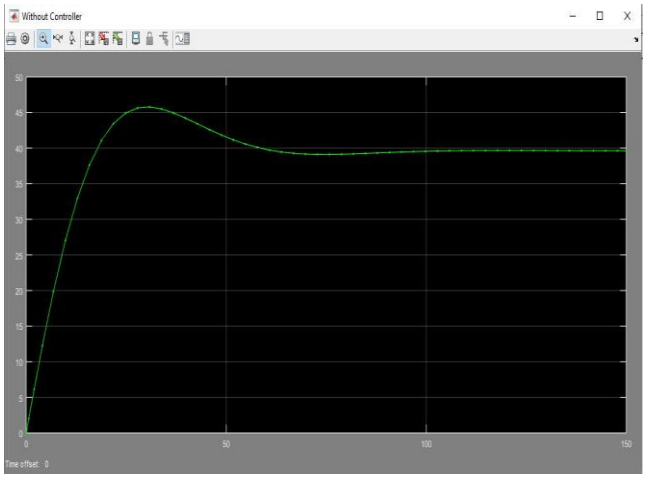

Fig.4. Response of heat exchanger system without controller.

B. Heat Exchanger with PID Controller

Simulink model:

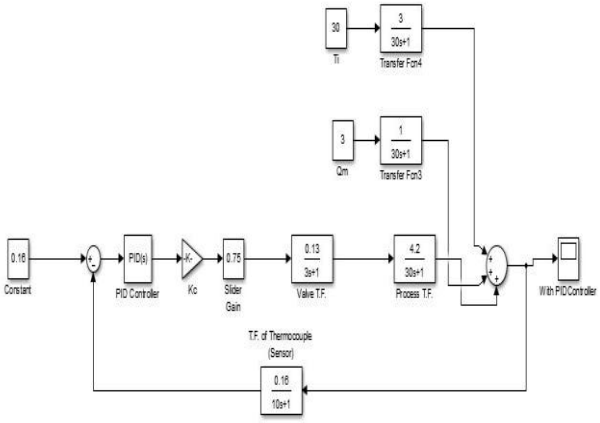

Fig.5.Simulink model of heat exchanger system with PID controller

Fig.5. depicts the simulink model of the heat exchanger plant with conventional PID controller followed by its time response as shown in fig.6. The heat exchanger system with PID controller shows a peak overshoot of 13.6%, settling time of 78sec and peak time of 28sec. It can be clearly observed that, this model has shown good improvement in time domain specifications but still there is a need in improvement of reduced settling time and killing overshoot to give an efficient performance. To this end, the system is

being modeled with most widely used intelligent controller called fuzzy logic controller.

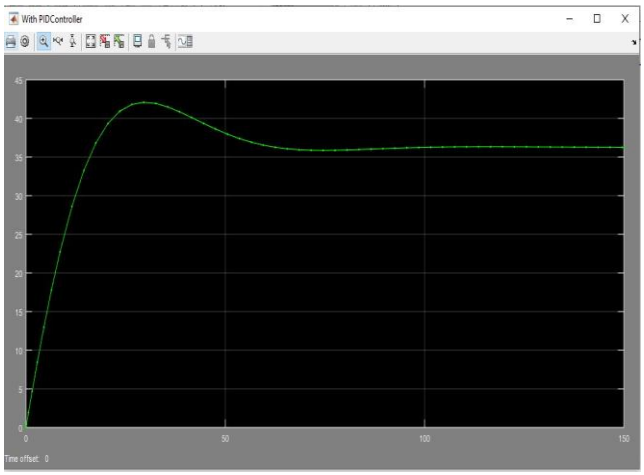

Fig.6. Response of heat exchanger system with PID controller

C. HEAT EXCHANGER SYSTEM WITH FLC

There are three steps in fuzzy interference system (FIS); [7]-[8]

1. Fuzzification (defining and deciding on fuzzy variables)

2. Decision making / Rule base (membership functions and forming set of rules using if, and, then)

3. Defuzzification (giving crisp output)

The FIS type used is mamdani method. The range of input variables is [-21,21]. Two input variables are considered here, they are, error 'e' and rate of change of error '$\frac{de}{dt}$'.

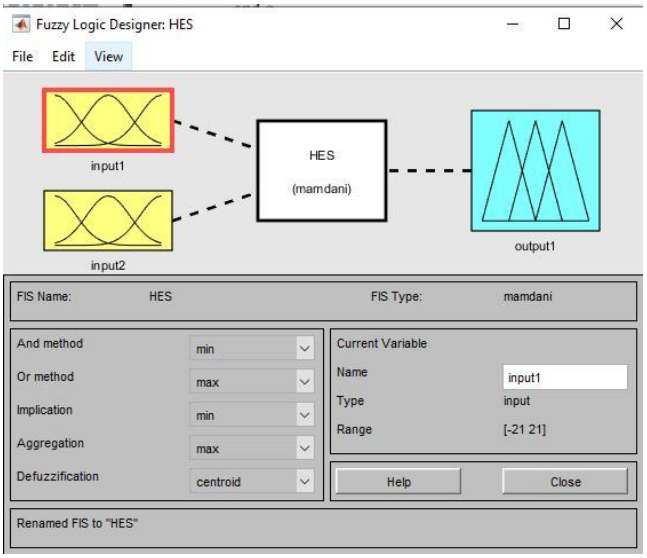

Fig.7. Giving inputs to HES.

The inputs are considered in terms of three triangular membership functions as indicated through negative small (NS), zero (ZE) and positive small (PS) with individual ranges for each membership function.

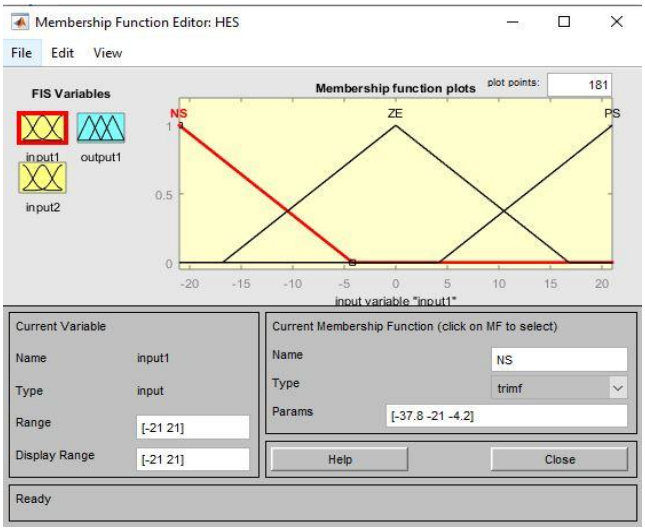

Fig.8. Membership function editor block

It is a single output system i.e. temperature which is again assigned with three triangular membership functions as indicated through small (S), medium (M) and high (H) with individual ranges for each membership function.

Simulink model:

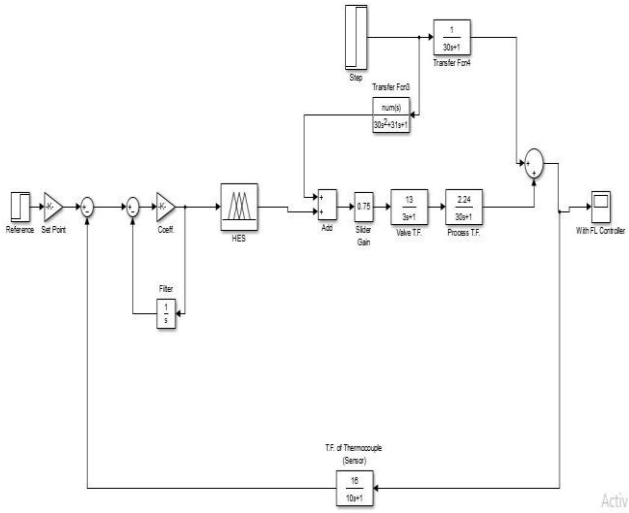

Fig.9. Simulink model of HES with FLC

The response of heat exchanger system as shown in fig.10 with FLC is evident that it has shown 100% improvement in time domain specifications in terms of overshoot and peak time and as well improved settling time.

We can observe that it has no overshoot and therefore no peak time. It is absolutely clear from step response analysis that FLC controller gives better performance than the conventional controllers like PID, IMC.

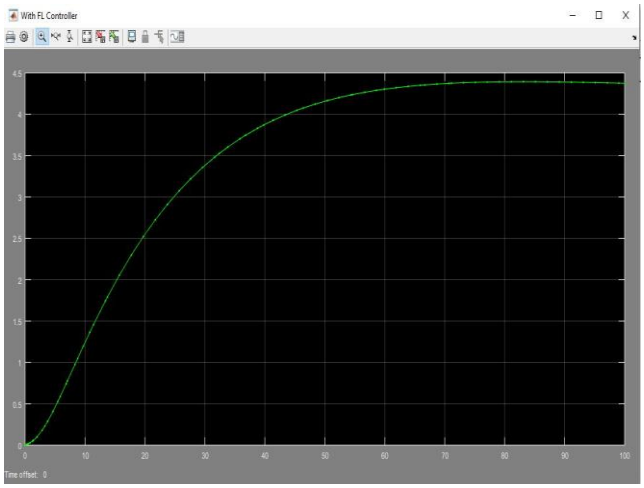

Fig.10. Response of heat exchanger system with FLC

COMPARATIVE ANALYSIS

Controllers	Settling Time (Sec)	Peak Time (Sec)	Overshoot (%)
Without controller	102	33	15
PID	78	28	13.6
FLC	60	-	-

Table.2. Performance analysis of different controllers

The comparative statement displaying the performance characteristics of exchanger system without controller and with IMC, PID and fuzzy controllers is shown in table.2. It is observed that among the different controllers the time domain specifications in terms of settling time, peak time, overshoots, FLC is giving optimal performance when compared to the other conventional controllers.

IV. CONCLUSION & FUTURE WORK

In this work, performance analysis of different conventional and intelligent controller (FLC) has been observed for the dynamics of a typical heat exchanger system. The objective of this proposed controller is to regulate the temperature of the outgoing liquid solution in a shortest settling time with minimum or no overshoot. Unit step response has been observed for controllers like PID and fuzzy controllers. It has been observed that fuzzy controller provides satisfactory performance when compared to other conventional controllers. The proposed FLC has exhibited 100% improvement in time domain specifications in terms of overshoot and peak time and as well improved settling time. Hence, intelligent controllers like fuzzy controllers can be employed for more reliable operation of real time systems like heat exchanger system.

As an extended scope for this work, other artificial intelligent techniques like artificial neural networks, genetic algorithms can be used for further improvement in the performance characteristics of the exchanger system.

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Face Mask Detection for Preventing Respiratory Infections using Arduino UNO

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Abstract— During this COVID-19 pandemic, it is good to wear mask and check body temperature. We wish to have a face mask detect in every crowd places. With this face mask detector, a person is needed to scan his/her face mask before entering. The face mask detector scan will the face mask on human face and open the gate automatically to allow person enter and help preventing or reduce the risk of spreading respiratory diseases from person to person. Otherwise, it will remind the person to wear the mask on LCD screen. This project presents the development of the warning system to the people for wearing the masks by using Arduino Uno.

In this project, we taking the idea of the mask scanner at the front door of every premise, person needs to scan their face before they can enter our premise. With this project, a person without mask cannot enter our premise and only the one wearing mask can enter our premise. This project is to recognize if the person is wearing a facemask or not. The dataset has an accuracy rate of greater than or equal to 80% as to the performance of the trained model. The system develops an Arduino Uno and ESP32 camera real-time facemask detection that captures the facial image if the person detected is not wearing a facemask. This work is beneficial in controlling the spread of the virus and avoiding contact with the virus. This can be integrated with embedded systems for application in airports, railway stations, offices, schools, and public places to ensure that public safety guidelines are followed. This presents the development of the warning system to the people for wearing the masks by using the Arduino Uno.

The system is designed to detect the faces and to determine whether the person wears a face mask or not. Using the above data, we can decide whether the concerned person can be allowed inside public places such as the market, or a hospital. This project can be used in the hospital, market, bus terminals, restaurants, and other public gatherings where the monitoring has to be done. This project consists of Arduino uno board which is used to run the code for all the hardware components used in this project. This project consists of ESP32 camera module that will capture the image of the people entering public places and detect whether the person wears a face mask or not using their facial features.

By using this project, we can develop the prototype device and can suppress the pandemic situation which was facing by whole world. The motive of the work comes from the people disobeying the rules that are mandatory to stop the spread of virus. Main purpose of this project is to provide this device prototype for all with low-cost equipment.

I. INTRODUCTION

As on 11-Sep2020 there are 28,3,66,652 people worldwide infected with Corona virus and 9,14,501 deaths , 20,3,67,966 people are recovered from covid. All sectors are severely affected because of covid many people lost their jobs throughout the world. More than 50. As per the WHO, Scientists guidelines wearing face mask and following other kind of precautions such as social distancing , frequent hand wash will help to reduce the spread of corona virus. After these guidelines many countries have framed their own rules regarding face mask to control the spread but there are many people refused to follow government rules. To catch these people police are struggling and they are unable to find every one everywhere. Face detection and object detection are the some of the computer vision problems will help to identify people who are not wearing masks and assist police to control these people.

Apart from mask detection there are various applications for object and face detection models in different real time domains such as driver less cars, criminal detection, Vehicle number plate detection etc.

Face recognition is a Artificial intelligence technique in which a given image is processed to find out what is the object inside the image whereas face detection techniques are used to find out where a specific object inside the image. Image classification is labelling objects inside the image. Scale invariant feature transform(SFIT): in this approach we are going to identify patches and apply some mathematical transformations on it to generate feature vector, then that feature vectors between images are compared for matching.

II. LITERATURE SURVEY

In earlier days face detection models are implemented using edge, line and center near features and patterns are recognized from those feature. These approaches are used to find binary patterns locally. These approaches are very effective to deal with Gray-scale images and the computation effort required also very less. AdaBoost is a regression based classifier which is going to fit regression function on original data set even some miss classified objects waits also adjusted during back propagation to optimize the results

"Prevention is better than cure" is one of the effective measures to prevent the spreading of COVID-19 and to protect mankind. Many researchers and doctors are working on medication and vaccination for corona.

COVID-19 spreads mostly by droplet infection when people cough or if we touch someone who is ill and then to our face (i.e., rubbing eyes or nose). Ongoing pandemic shows that it is much more contagious and spreads fast. Depending on the infection spreading, we have two cases: Fast and Slow spread.

A fast pandemic will be terrible and will cost many lives. It occurs due to a rapid rate of infection because there are no countermeasures to slow it down. This is because, if the numbers of infected people get too large, healthcare systems become unable to handle it. We will lack resources such as medical staff or equipment like a ventilator.

To avoid the above situation, we need to do what we can to turn this into a slow pandemic. A pandemic can be slowed down only by the right responses, mainly in the early phase. In this phase, everyone who is sick can get treatment and there is no emergency point with flooded hospitals.

In this pandemic, we need to engineer our behaviour as a vaccine. that is, "Not getting infected" and "Not infecting others". The best thing we can do is to wash our hands with soap or a hand sanitizer. The next best thing is social distancing.

To avoid getting infected or spreading it, it is essential to wear a face mask while going out from home especially to public places such as markets or hospitals.

Coronavirus disease (COVID-19) is an irresistible infection caused by a newfound Coronavirus. A great many people tainted with the COVID-19 infection will encounter mellow to direct respiratory ailment and recoup without requiring exceptional treatment. More seasoned individuals, and people with fundamental clinical issues like cardiovascular infection, diabetes, ongoing respiratory ailment, and malignant growth are sure to create genuine ailment. The most ideal approach to forestall and hinder transmission is to be all around educated about the COVID-19 infection, the illness it causes and the way it spreads. Shield yourself as well as other people from disease by washing your hands or utilizing a liquor-based rub regularly, not contacting your face and wearing a veil. The first three parts need to be governed by ourselves but it can either urge people or motivate them to wear masks, the proposed project implementation has attempted to make people aware that face masks are essential for their own and other's safety.

III. METHODOLOGY

In this paper we have proposed a new architecture called as Face Mask Detection for Preventing Respiratory Infections using Arduino UNO to detect weather a person wearing mask or not. The proposed architecture is easier to implement as well as the cost is also low . The system is designed to detect the faces and to determine whether the person wears a face mask or not. Using the above data, we can decide whether the concerned person can be allowed inside public places such as the market, or a hospital. This project can be used in the hospital, market, bus terminals, restaurants, and other public gatherings where the monitoring has to be done.

This project consists of a camera that will capture the image of the people entering public places and detect whether the person wears a face mask or not using their facial features.

IV. RESULT AND DISCUSSION

We have used many images to check whether the person is wearing the mask or not. And also the kit will detect the percentage of the mask covered by the person who is entering into any public or private places.

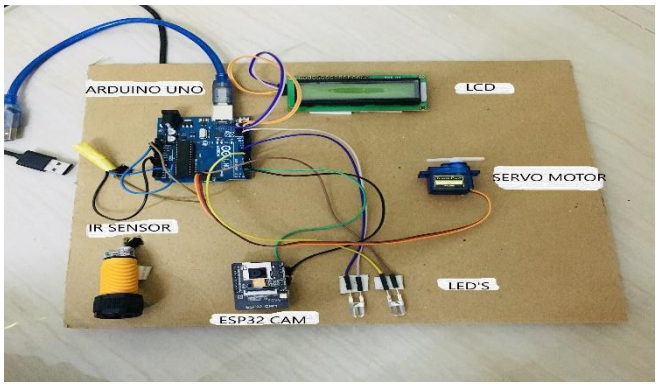

Figure: 4.1 Implementation of project.

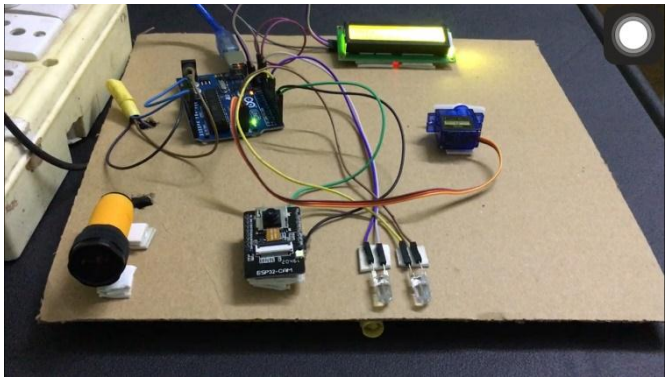

Figure: 4.2 Power supply to the kit.

Whenever the power supply is given to the kit the kit starts working as we can see in the above figure 4.2.

Figure:4.3 The kit starts connecting to the WIFI .

As the power supply given to kit, the kit starts connecting to WIFI where the credentials are giving in the code which was dumped in to the Arduino UNO .

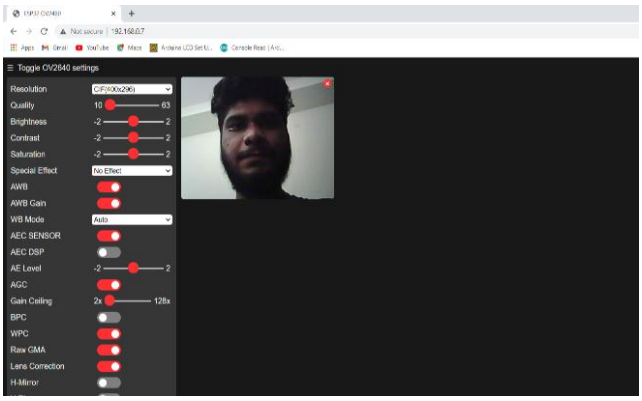

Figure:4.4 ESP32 CAMERA Module streaming.

As the kit is connected to WIFI then the ESP32 Cam Module will produce an IP Address in LCD display, by pasting that IP Address in chrome it will connect to the server and then start streaming in laptop, mobile. The final of our project that it will detect the percentage of the mask covered by the person who is entering into any public or private places.

This project is used to control the spreading of covid virus and also many fungus variants are raising day by day, the fungus variants are spreading rapidly through air so that by proper monitoring of the public we can control the spreading of virus. Our project implemented with low cost so that in every private and public place's every one can afford and place this at their residence or offices. Our main motto is that everyone should join their hands to stop this virus with our project.

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Implementation Fault Tolerant Full Adder/Subtractor Using Reversible Logic Gates

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Abstract— Reversible logic is most popular concept in energy efficient computations and this will be demand for upcoming future computing technologies. Reversible logic is emerging as an important research area and it will be having wide applications in many fields such as optical information processing, quantum computing and Low power CMOS design. Under ideal conditions, the reversible logic gates will produce zero power dissipation. So this concept will helpful for Low power VLSI design. This paper will proposes the design of Full adder/subtractor circuit using fault tolerant reversible gates. The design can work singly as an adder/subtractor. The proposed design offers less hardware complexity and is efficient in terms of gate count, delay, constant inputs and garbage outputs compared to previous Fault tolerant Full Adder/Subtractor design. A parallel adder/subtractor design using fault tolerant reversible gates also proposed in this paper. The proposed circuits will be simulated using ModelSim simulator and implemented in Xilinx FPGA platform.

Keywords— Adder/Subtractor, Parity preserving reversible gates, Parallel Adder/Subtractor, Reversible logic gates

I. INTRODUCTION

Today's new technology offers faster, smaller and complex circuits. Moore's law states that Performance (speed) of an integrated circuit per unit cost increased by a factor two for every 18 months. In order to achieve higher speed the clock frequency must be high and for smaller, complex circuit's the number of transistors in the IC must be large and they are more closely packed in order to save area. As the IC will be faster, complex means that will increases the power dissipation in the circuit. Almost all conventional computers comprises of million numbers of gates that are irreversible in nature. During logical operations in the circuit some information is erased or lost that will causes heat dissipation and energy loss. R Landauer [1] has shown that circuit with irreversible components, during computation each bit loss generates kTln2 joules of energy, where k is Boltzmann's constant and T is absolute temperature. At a temperature T for one bit loss it will generates 2.86 × 10-21 J of energy that will be small but we cannot neglect this value. The heat dissipated in the circuit will gradually decrease the performance and also life span of the circuit or device. In order to overcome these types of problems we require low power consumption and less dissipation components in the circuit. C H Bennet [2] shown that if we use reversible logic gates instead of irreversible components in the circuit, we can achieve zero energy dissipation in the circuit. He proposed two conditions of reversibility.

1st condition: For any device to be reversible if its input and output will be uniquely retrievable from each other called logical reversibility.

2nd condition: A device can run actually backwards then it is called physically reversible.

The reversible circuits are those in which reversible logic gates are basic building blocks and there is no energy loss. The reversible logic gates will be having n-input and n-output i.e. equal number of input and equal number of output, and also with oneto-one mapping i.e. inputs can be uniquely recovered from the outputs.

II. LITERATURE REVIEW

Reliable computing and quantum computing is one ofthe emerging areas in today's world. Berger codes can detect stuck-at faults and skews in asynchronous systems which is a part of reliable computing [l3]. On the other hand, reversible logic is a growing technique in low power applications such as quantum computing. Work proposed in [l4] discusses different concurrent error detecting arithmetic and logic units using Berger codes such as signed and unsigned addition and subtractions, l6 logical operations, shift operations, multiplication and division. Authors in [lO] used Berger code as a means of in corporating CED (Concurrent Error Detection) into a selfchecking register file. A Berger check prediction circuit is an external circuit that needs to be built to test errors. In the mean while, Fault Tolerant reversible circuits are those which do not require any additional hardware, but has an inherent property of detecting errors. Several Fault Tolerant Adders and Subtractors has been proposed in the literature. Fault Tolerant Full Adder using Fredkin gate with Feynman gate to preserve the parity has been proposed in [4]. In the same way reversible FullAdder has been proposed using IG gate and F2PG gate by the authors in [l5] and [5] respectively. In the literature, this is the first attempt of designing a reversible Berger check prediction circuit using reversible gates. Also, a reversible Fault Tolerant circuit has been designed with optimized parameters. The designed circuits are analyzed in terms of performance parameters to detect unidirectional errors. In case of parity preserving technique, if multiple errors occurs on the same line then it cannot

detect them, as one error may cancel other. Hence this technique cannot detect multiple errors.

In"Irreversibility and Heat Generation in the Computing Process" It is argued that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of *kT* for each irreversible function. This dissipation serves the purpose of standardizing signals and making them independent of their exact logical history. Two simple, but representative, models of bistable devices are subjected to a more detailed analysis of switching kinetics to yield the relationship between speed and energy dissipation, and to estimate the effects of errors induced by thermal fluctuations

IN "DESIGN OF LOW POWER COMPARATOR USING DG GATE" In recent studies, reversible logic has emerged as a great scene of research, having applications in low power CMOS circuits, optical computing, quantum computing and nanotechnology. The classical logic gates such as AND, OR, EXOR and EXNOR are not reversible. In the existing literature, reversible sequential circuits designs are offered that are improved for the number of the garbage outputs and reversible gates. Minimizing the number of garbage is very noticeable. In the present paper, we show a design of the reversible comparator based on the quantum gates implementation of the reversible DG gate. The reversible DG gate is designed by using 3 × 3 quantum gates such as NOT, CNOT, Controlled-V and Controlled-V+ gates. Also, we have used the TR gate and various types of quantum gates in the implementation results. Low power three-bit comparator is designed using DG Gate, New Gate and Fredkin Gate. In order to evaluate the benefit of using the DG gate proposed in this paper, one-bit comparator is constructed. The design is useful for the future computing techniques like quantum computers. The proposed designs are implemented using VHDL and functionally investigated using Quartus II simulator.

In "Optimized Nanometric Fault Tolerant Reversible BCD Adder" In recent years, reversible logic has become one of the most important areas of researches because of its applications in several technologies; such as low-power CMOS, Nano-computing and optical computing. In this paper, we have presented designs of a compact and efficient fault tolerant reversible Binary Coded Decimal (BCD) adder as well as a fault tolerant reversible Carry Skip BCD adder. We have proposed new reversible fault tolerant gates and heuristic algorithms to design compact BCD Adders. The proposed reversible fault tolerant BCD adder achieves the improvement as reducing cost of 23.07% on the number of gates, 52.67% on quantum cost, 31.03% on garbage outputs, 29.16% on the number of constant inputs and 23.07% on unit delay over the existing best one. Similarly, the proposed reversible fault tolerant carry skip BCD adder achieves the improvement as reducing cost of 34.72% on the number of gates, 43.24% on quantum cost, 37.5% on garbage outputs, 37.14% on the number of constant inputs and 34.72% on unit delay over the existing best one.

In "Fault-Tolerant Reversible Circuits" Reversible hardware computation, that is, performing logic signal transformations in a way that allows the original input signals to be recovered from the produced outputs, is helpful in diverse areas such as quantum computing, low-power design, nanotechnology, optical information processing, and bioinformatics. We propose a paradigm for performing such reversible computations in a manner that renders a wide class of circuit faults readily detectable at the circuit's outputs. More specifically, we introduce a class of reversible logic gates (consisting of the well-known Fredkin gate and a newly defined Feynman double-gate) for which the parity of the outputs matches that of the inputs. Such parity-preserving reversible gates, when used with an arbitrary synthesis strategy for reversible logic circuits, allow any fault that affects no more than a single logic signal to be detectable at the circuit's primary outputs. We show the applicability of our design strategy by demonstrating how the well-known, and very useful, Toffoli gate can be synthesized from parity- preserving gates and apply the results to the design of a binary full-adder circuit, which is a versatile and widely used element in digital arithmetic processing

Reversible Logic Gates

The main object in reversible logic theory is the reversible function, which is defined as follows.

Definition1. The multiple output Boolean function *F*(*x*1*; x*2*; :::; xn*) of *n* Boolean variables is called reversible if:

1. The number of outputs is equal to the number of inputs;

2. Any output pattern has a unique preimage.

In other words, reversible functions are those that perform permutations of the set of input vectors.

Definition2. Garbage is the number of outputs added to make an *n*-input *k*-output function ((*n; k*) function) reversible.

We use the words "constant inputs" to denote the present value inputs that were added to an (*n; k*) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs

Input + constant input = output + garbage.

The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the Equations 1, 2 and 3.

V * V = NOT …… (1)

V * V+ = V+ * V = I …….. (2)

V+ * V+ = NOT ……. (3)

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates [2],[3].

2.1 NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.

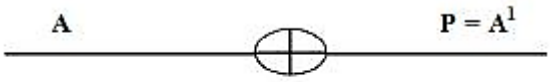


Figure1. NOT gate

2.2 Feynman / CNOT Gate

Controlled NOT (CNOT) gate is an example for a 2*2 gate. The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q = A B) is as shown in the Figure 2.

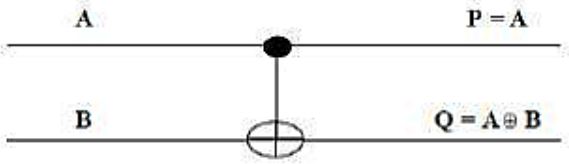


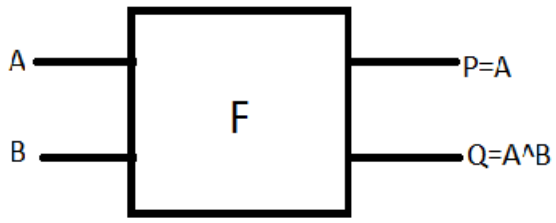
Figure2. Feynman/CNOT gate

There are many 3*3 Reversible gates such as F, TG, PG and TR gate.

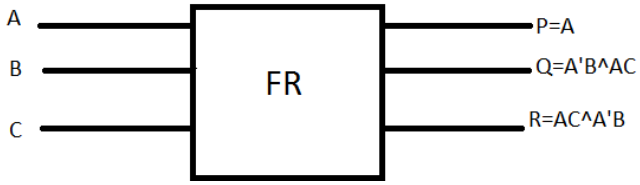
III. REVERSIBLE GATES

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

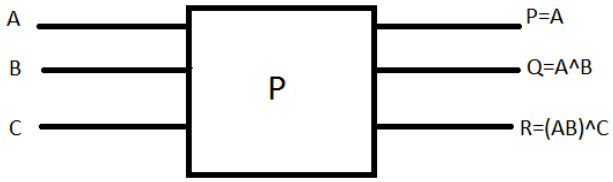
Feynman Gate: Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1



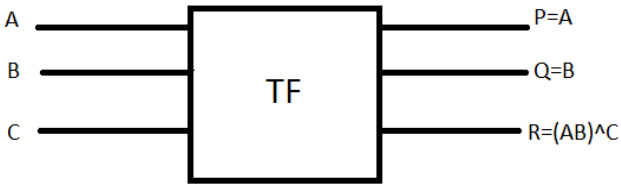
Fredkin Gate: It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2:



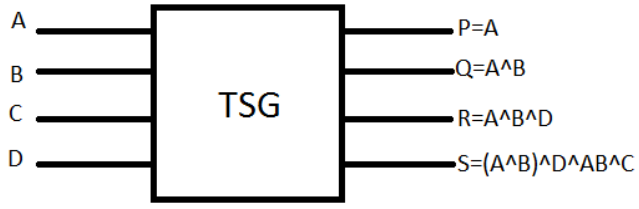
Peres Gate: It is a basic reversible gate which has 3- inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:



Toffoli Gate: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

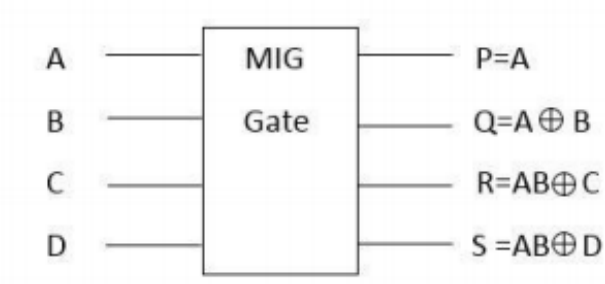


TSG Gate: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A, Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:



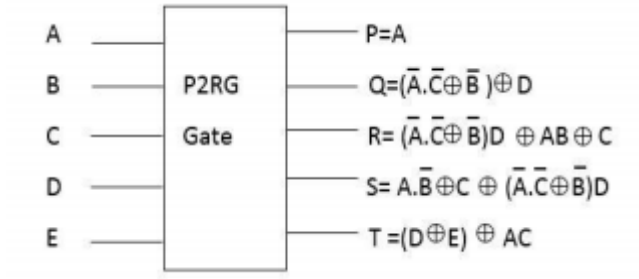
MIG GATE:

Modified IG Gate (MIG): Fig. 4 shows 4*4 Modified IG [7] gate. It has A, B, C and D input vector and output vector as P = A, Q = A⊕ B, R = AB ⊕C and S = AB'⊕D.



Modified IG Gate (MIG) Parity Preserving Reversible Gate (P2RG): Fig.5 shows 5*5 parity preserving reversible gate

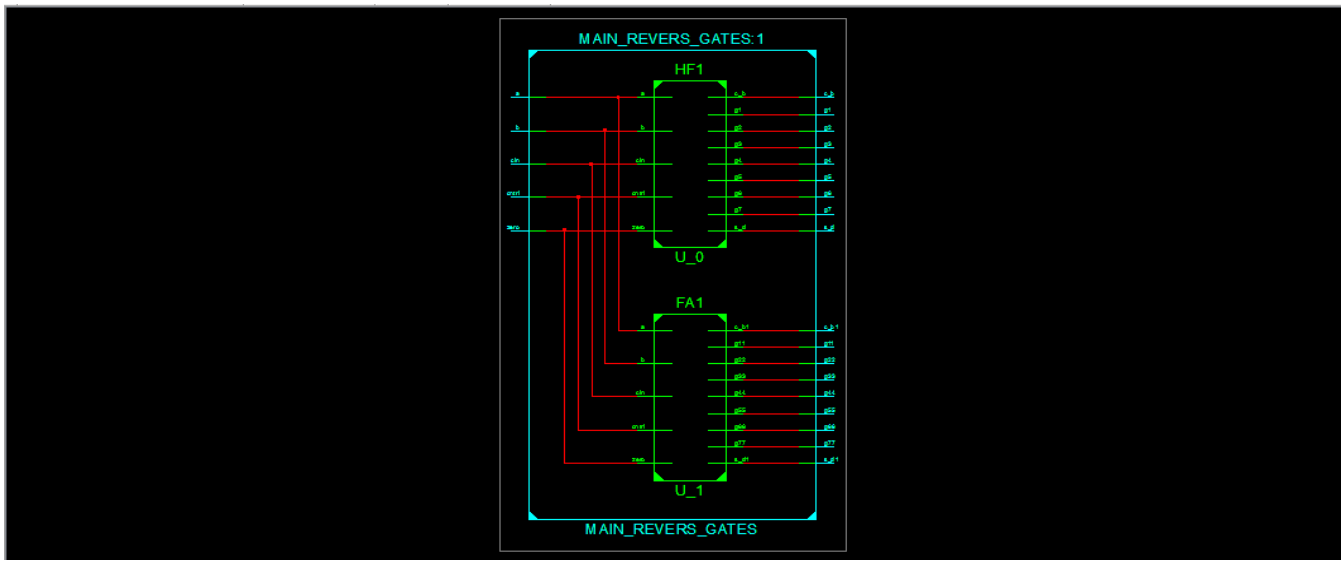
[10], P2RG. It has A, B, C, D and E input vector and output vector as P=A, Q= (A'C'⊕B') ⊕D, R= (A'C'⊕B') D⊕AB⊕C, S=AB'⊕C⊕ (A'C'⊕B')'D and T= (D⊕E) ⊕AC.

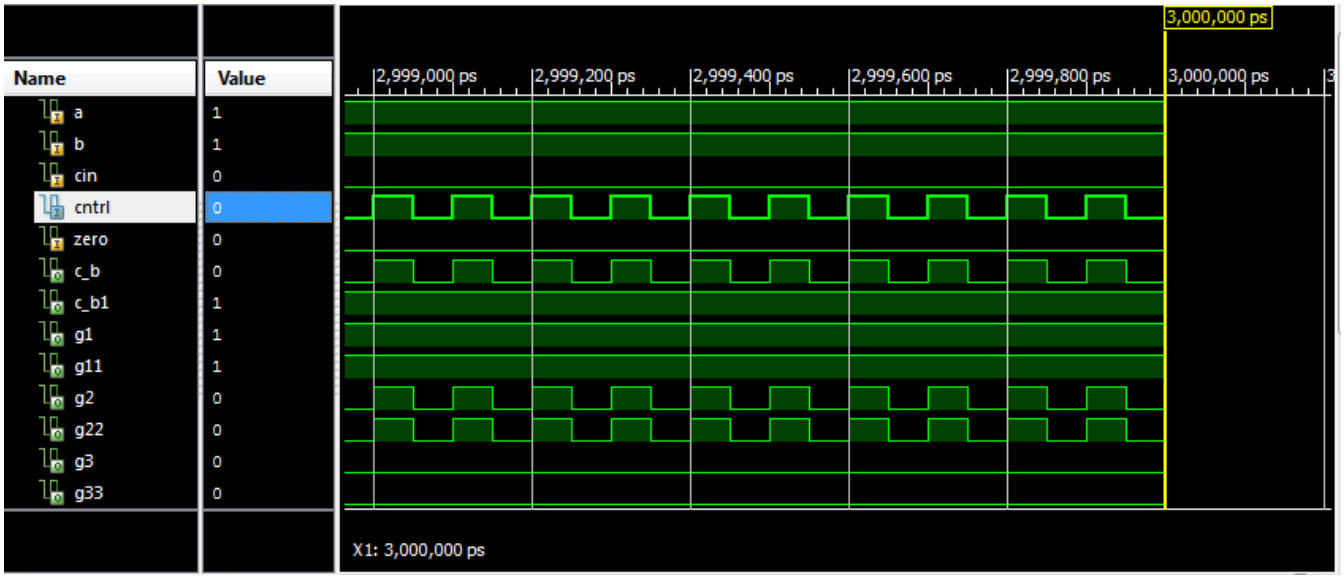


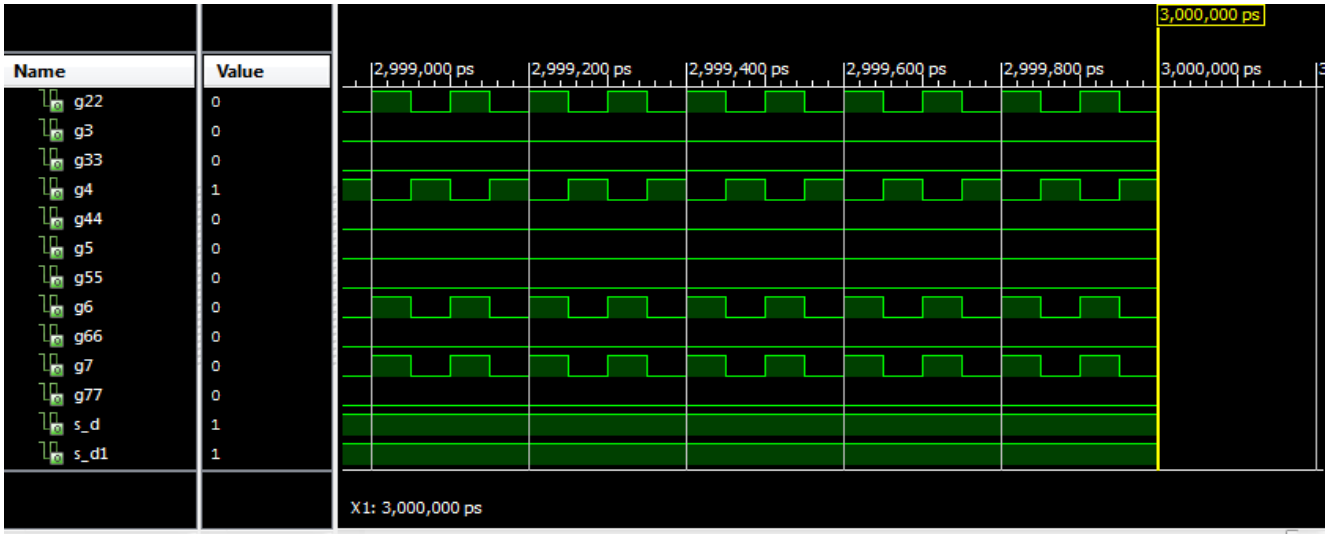
Parity Preserving Reversible Gate (P2RG)

Full Adder is design by use MIG and COG based Reversible Logic gate. The proposed design model contain control signal which is using for control the adder and subtractor operation. Figure 6 is showing the diagram for MIG (Modified Islam Gate). In this four inputs and 4 Output are using. Figure 7 is showing the COG Gate which has 3 Input and 3 Output. Figure 8 is showing the proposed circuit for design Fault Tolerant Full Adder / Subtraction. In this two MIG gates are using and one COG gate is using. There are A, B, C, Cntrl are in input and C/B and S/C are the output. The control signal is using for control the operation of Adder / Subtraction. For the Logic, 0 Adder will work, and for Logic 1 Subtractor will work.

IV. RESULT







V. APPLICATIONS

The reversible logic will have many applications. Some important areas of reversible logic include the following [13, 14]

- Nanocomputing
- Bio Molecular Computations
- Laptop/Handheld/Wearable Computers
- Spacecraft
- Low power CMOS.
- Design of low power arithmetic and data path for digital signal processing (DSP).

VI. CONCLUSION AND FUTURE WORK

This paper presents efficient approach for the design of fault tolerant full adder/subtractor and parallel adder/subtractor. The proposed design can work as single unit that can acts as adder as well as subtractor depending upon our requirement. The proposed design offers less hardware complexity, less gate count, less garbage bits and constant inputs. The reversible computation can be done efficiently with less number of garbage bits and constant inputs. The proposed Fault tolerant Adder/Subtractor design can be used to realize some arithmetic components such as carry save adder, carry skip adder and multiplier/divisors etc,. In future we are planning to design more optimized Fault tolerant Adder/Subtractor design and other fault tolerant circuits i.e. less garbage bits and constant input.

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Area Optimized VLSI Architecture for Dynamic Accuracy Configurable Multiplier using Higher Order Compressors

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Abstract— In this paper, presents dadda multiplier by 8:2compressors, it has the ability to operate in exact addition modes. These dual-quality compressors take up less space and use less energy, but they have a lesser precision. Each of these compressors has a different degree of precision. The use of these compressors in parallel multiplier structures results in adjustable multipliers whose accuracies, powers, and areas can change dynamically during runtime.

By comparing their parameters to those of state-of-the-art accurate multipliers, the efficiency of these compressors in an 8-bit Dadda multiplier are analyzed in VLSI technology. In the xilinx12.3ise design suite, the simulation and synthesis findings were concluded. In some image processing applications, the effectiveness of these compressors is also evaluated.

Keywords— 8:2 compressor, dadda multiplier algorithms

I. INTRODUCTION

The multiplier is one of the most important arithmetic blocks, and it is frequently utilized in a variety of applications, particularly signal processing applications. The multipliers can be built in two different architectures: sequential and parallel. Sequential designs are low-power, however they have a very long delay.

Parallel architectures, on the other hand, (such as Wallace tree and Dadda) are fast but consume a lot of power. Parallel multipliers are utilized in high-performance applications where their excessive power consumption could result in hotspots on the chip.

The adjustment of these parameters for multipliers becomes vital since power consumption and speed are crucial elements in the design of digital circuits. Frequently, the optimization of one parameter is done while the other parameter is constrained. Specifically, given the limited power budget of portable devices, getting the desired performance (speed) is a difficult task.

Furthermore, achieving the system's desired performance may be hampered by a certain level of reliability. A variety of solutions at various design abstraction levels have been proposed to achieve the power and speed specifications. Approximate computing methods are based on meeting target parameters at the expense of computation precision.

The method can be utilized in situations when there isn't a single correct solution and/or a set of responses that are close to the correct outcome is acceptable. Multimedia processing, machine learning, signal processing, and other error-tolerant computations are among these applications.

The simplification of arithmetic unit circuits is the foundation of approximate arithmetic units. Many previous studies have focused on approximation multipliers, which offer better speeds and reduced power consumption at the expense of reduced accuracy.

Almost every proposed accurate multiplier is based on a constant level of accuracy during runtime. The runtime accuracy reconfigurability, on the other hand, is thought to be a beneficial feature for delivering various levels of service quality throughout system operation.

Four dual-quality reconfigurable accurate 8:2 compressors are shown in this work, with the option to switch between the exact during runtime. The compressors can be used in dynamic quality customizable parallel multiplier designs. The proposed compressors' basic structures are made up of two parts: approximation and supplemental.

II. DADDA MULTIPLIER

Multipliers are critical in the present advanced flag handling and for different applications. Numerous scientists have attempted and many are endeavoring to plan the multipliers which will enhance the outline parameters like – speed, low power utilization less range or by combining these into a single multiplier, they can be used in a variety of rapid, low-power VLSI applications.

The basic idea of DADDA multiplier depends on the underneath framework shape appeared in Fig 1 the partial product is framed in the principal organize by AND gates.

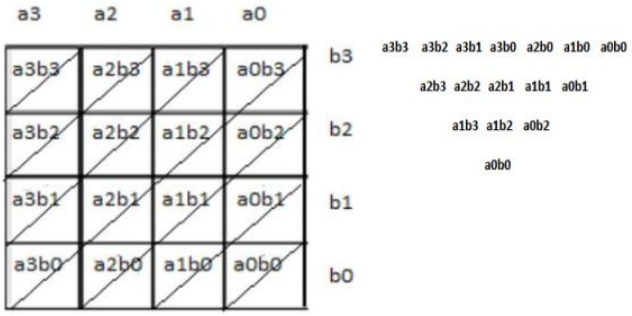

Fig1. Algorithm of Dadda multiplier

Algorithm:

Let's say the final two-row matrix height is d1 = 2, and the subsequent matrix heights are calculated using dj+1 = 1.5 * dj, where j = 1,2,3,4,..... The fraction in this matrix height should be rounded down to the smallest possible value. 13.5 = 13 is a good example (rounded). The matrix heights will be in the following order: 2,3,4,6,9,13,19,28.....

Finally, the greatest dj should be found so that the resultant matrix height does not exceed the overall height of the matrix.

1. The column compression should be done with the [3,2] and [2,2] counters in the first reduction stage such that the reduced matrix height does not exceed dj. The total must be passed to the same column in the next reduction stage, and the carry must be given to the next column, during compression.

2. Repeat the previous two procedures until a final two-row reduced matrix is obtained.

3. Exact 4:2, 8:2 Compressor

4:2 and 8:2 compressors are commonly used to shorten the latency of the partial product summation stage of parallel multipliers. Some compressor constructions have been presented that have been optimized for one or more design criteria (for example, delay, area, or power consumption). This study focuses on the exact 4:2 ratio and includes a compressor.

This sort of compressor contains four inputs (x1–x4) and an input carry (Cin), as well as two outputs (sum and carry) and an output Cout, as shown schematically in Fig. 2. As illustrated in Fig. 3, the internal construction of an exact 4:2 compressor is made up of two serially coupled complete adders. weights of all inputs and the total output are the same in this structure, but the weights of the carry and Cout outputs are one binary bit greater. The total, carry, and Cout outputs of the 4:2 compressors are obtained.

This sort of compressor, as illustrated in Fig. 2, has four inputs (x1–x4) and an input carry (Cin), as well as two outputs (sum and carry) and an output carry (Cin). As illustrated in Fig. 3, the internal construction of an exact 4:2 compressor is made up of two serially coupled complete adders. The weights of all inputs and the total output are the same in this structure, but the weights of the carry and Cout outputs are one binary bit greater. The total, carry, and Cout outputs are produced from

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \quad (1)$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4 \quad (2)$$

$$\text{Cout} = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1. \quad (3)$$

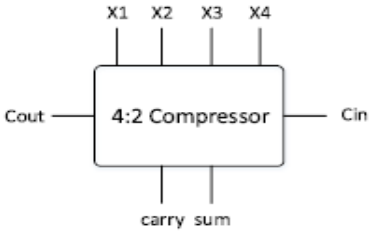

Fig.2. 4:2 compressor block diagram.

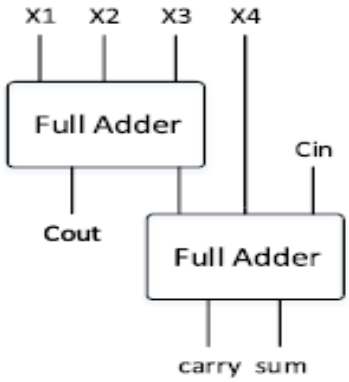

Figure. 3. Structure of the 4:2 compressor.

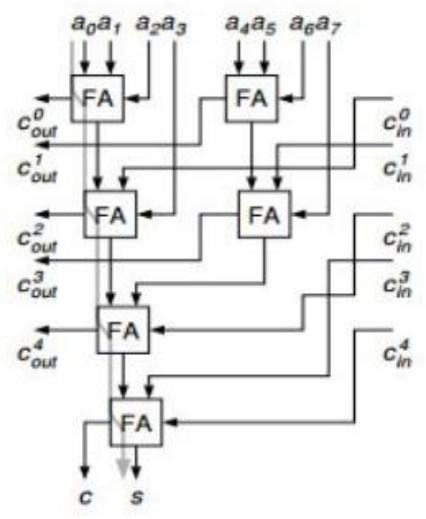

Fig. 4. Structure of the 8:2 compressor.

8:2 compressors are commonly used in parallel multipliers to shorten the latency of the partial product summation stage. The 8:2 compressor having 8 inputs, five carry inputs and this structure produces four internal carry outputs, one main carry output and sum.

Compressor structures have been presented that have been optimized for one or more design criteria (e.g., delay, area, or power consumption). The exact 8:2 compressor is presented in figure4.And the proposed multiplier structure designed by 8:2 compressing adder as shown in figure 5and this compressor input signals are eight and remaining 5

input signals are working as a carry input signal and each level compressor delivers 5 output carry signals.

These output carry signals are work as a input carry signals to the next compressing level as shown in figure5. At final state all inputs are added through the arithmetic addition to overcome the repeating of compressing output carry signals.

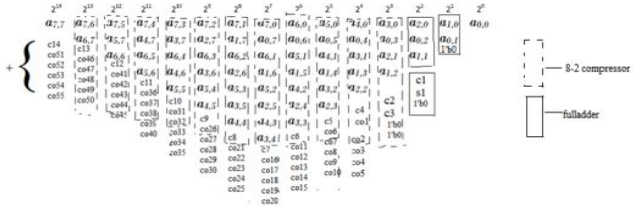

Fig. 5. Reduction circuitry of an proposed 8-bit Dadda multiplier.

III. RESULTS

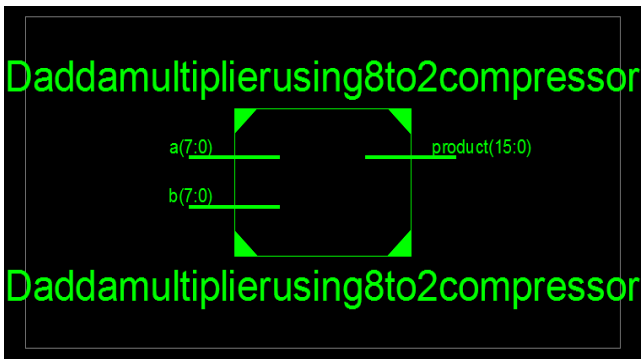

Fig 6:RTL schematic view

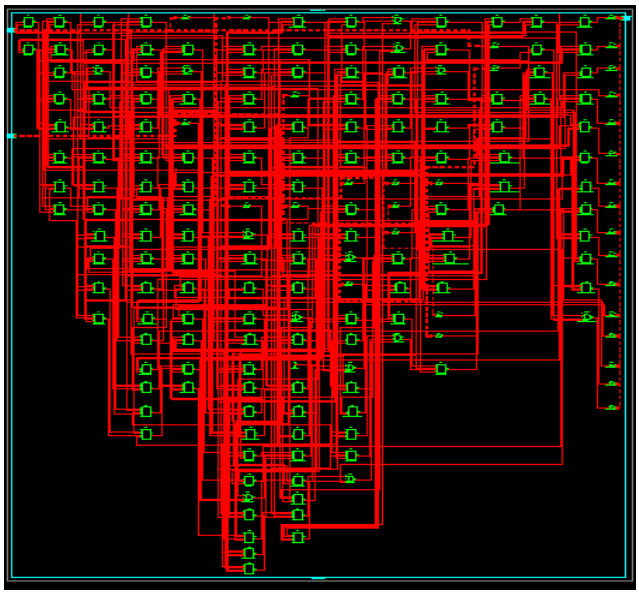

Fig 7:View Technology Schematic

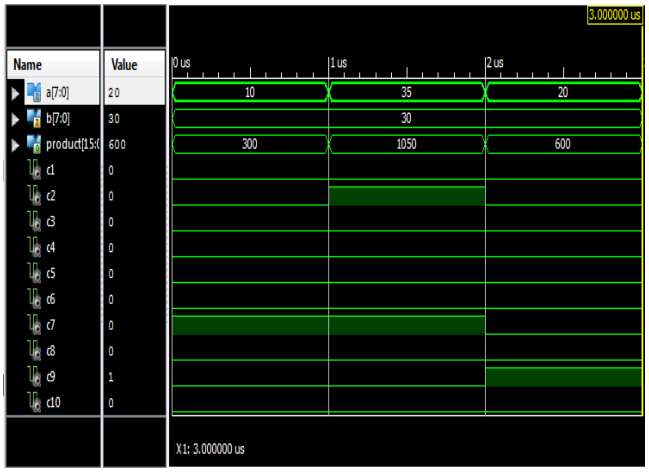

Fig 8: simulated waveforms

Parameter	Dadda multiplier using 4:2compressor	Dadda multiplier using 8:2compressor
No of LUTs	169	157
Power (mW)	1.379	1.281

Table 1:parameter comparison table

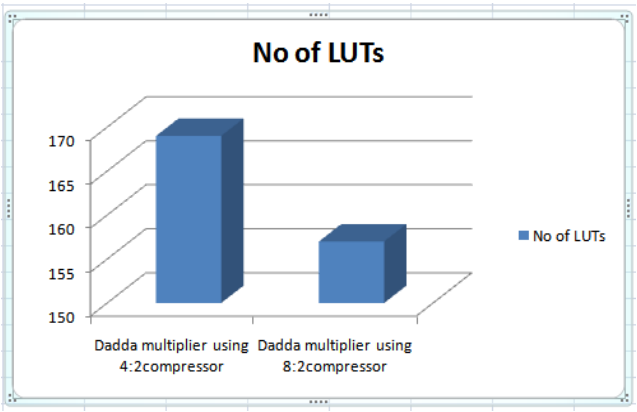

Fig9:LUTs comparison bar graph

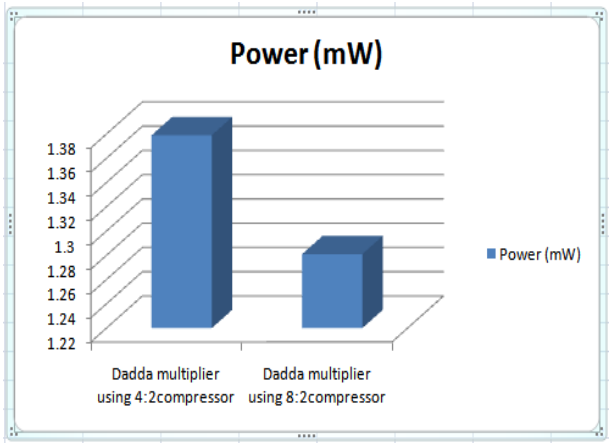

Fig10:Power comparison bar graph

IV. CONCLUSION

The proposed Dadda multiplier with an 8:2 compressor compresses better than the existing Dadda multiplier with a 4:2 compressor in this study. From the table 1 the proposed design uses less LUTs 157 when compared with the existing design with an LUTs count of 169. At the same time, the proposed design consumes 1.281 mW of power, which is significantly less than the previous design power consumption with a value of 1.379mW, those are shown in table1.This work presents the 8:2 compressing adder structure.

The experimental results were observed in Xilinx 12.3 ISE design suit, that the proposed multiplier delivers significantly a small area and less power overhead than those of the conventional dadda multiplier. The proposed multiplier accomplishes the initial goal of providing an unbiased optimum result area, as well as power and delay, without sacrificing precision.

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VLSI Architecture for Power Detection by using FPGA

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Abstract— Now a day's Wireless network and mobile everywhere .But the main problem in the wireless networks are limited spectrums. So to solve this spectrum scarcity and to provide high bandwidth to mobile users via heterogeneous wireless network architectures a promising technology Cognitive radio (CR) is developed. The CR technology provides the way for utilization of spectrum completely by means of identifying the unused holes in the spectrum band. But the spectrum has to be sensed for identifying the available spectrum which is somewhat complicated. However the sensing of spectrum can be done by power detection technique. In this paper newly optimized power detection architecture is implemented, in which the area and power performance will be optimized. Such power detection based spectrum sensing can be developed by Verilog coding using FPGA.

Keywords— CR; sensing scheme; Power detection; spectrum utilization; FPGA

I. INTRODUCTION

Today's emerging technology and devices paved the way for major demand of spectrum resource usage and it is gradually increases as the technologies grow rapidly. In order to solve this demand, the overall spectrum has to be utilized properly by all primary as well as secondary users of the wireless network.

Generally there are primary users named as licensed users and secondary users (named as unlicensed user) of a network. Sometimes the primary user part of the spectrum is not used and it is said to be white holes. Such holes will be efficiently used by assigning it to the unlicensed users in the network.

Cognitive radio networks, spectrum sensing aims to detect the unused spectrum channels in order to use the radio spectrum more efficiently. Various methods have been proposed in the past, such as energy, feature detection, and matched filter. These methods are characterized by a sensing threshold, which plays an important role in the sensing performance. Most of the existing techniques used a static threshold. However, the noise is random, and, thus the threshold should be dynamic. In this paper, we suggest an approach with an estimated and dynamic sensing threshold to increase the efficiency of the sensing detection. The matched filter method with dynamic threshold is simulated and its results are compared to those of other existing techniques.

Field-programmable gate arrays (FPGAs) are integrated circuits, which constitute the "new kid in town'' where digital hardware technology is concerned. An FPGA is an array of logic blocks (cells) placed in an infrastructure of interconnections, which can be programmed at three distinct levels[1]the function of the logic cells,[2]the interconnections between cells, and [3]the inputs and outputs. All three levels are configured via a string of bits that is loaded from an external source, either once or several times. In the latter case the FPGA is considered reconfigurable. FPGAs are highly versatile devices that offer the designer a wide range of design choices and options. However, this potential power necessitates a suite of tools in order to design a system. Essentially, these tools generate the configuration bit string, given such inputs as a logic diagram or a high-level functional description. So In this paper newly optimized power detection architecture is implemented, in which the area and power performance will be optimized. Such power detection based spectrum sensing can be developed by Verilog coding using FPGA..

II. LITERATURE REVIEW

The concept of cognitive radio was first proposed by Joseph Mitola III in a seminar at KTH Royal Institute of Technology in Stockholm in 1998 and published in an article by Mitola and Gerald Q. Maguire, Jr. in 1999. It was a novel approach in wireless communications.

Two main types of cognitive radio:

- **Full Cognitive Radio** (Mitola radio), in which every possible parameter observable by a wireless node (or network) is considered.
- **Spectrum-Sensing Cognitive Radio**, in which only the radio-frequency spectrum is considered.

Other types are dependent on parts of the spectrum available for cognitive radio:

- **Licensed-Band Cognitive Radio**, capable of using bands assigned to licensed users (except for unlicensed bands, such as the U-NII band or the ISM band).
- **Unlicensed-Band Cognitive Radio**, which can only utilize unlicensed parts of the radio frequency (RF) spectrum.

Cognitive exertion:

Spectrum mobility: Process by which a cognitive-radio user changes its frequency of operation. Cognitive-radio networks aim to use the spectrum in a dynamic manner by allowing radio terminals to operate in the best available frequency band, maintaining seamless communication requirements during transitions to better spectrum.

Spectrum sharing: Spectrum sharing cognitive radio networks allow cognitive radio users to share the spectrum bands of the licensed-band users. However, the cognitive radio users have to restrict their transmit power so that the interference caused to the licensed-band users is kept below a certain threshold.

Sensing-based Spectrum sharing: In sensing-based spectrum sharing cognitive radio networks, cognitive radio users first listen to the spectrum allocated to the licensed users to detect the state of the licensed users. Based on the detection results, cognitive radio users decide their transmission strategies. If the licensed users are not using the bands, cognitive radio users will transmit over those bands. If the licensed users are using the bands, cognitive radio users share the spectrum bands with the licensed users by restricting their transmit power.

Database-enabled Spectrum Sharing, In this modality of spectrum sharing, cognitive radio users are required to access a white space database prior to be allowed, or denied, access to the shared spectrum. The white space database contain algorithms, mathematical models and local regulations to predict the spectrum utilization in a geographical area and to infer on the risk of interference posed to incumbent services by a cognitive radio user accessing the shared spectrum. If the white space database judges that destructive interference to incumbents will happen, the cognitive radio user is denied access to the shared spectrum.

Spectrum management: Capturing the best available spectrum to meet user communication requirements, while not creating undue interference to other (primary) users. Cognitive radios should decide on the best spectrum band (of all bands available) to meet quality of service requirements;

Therefore, spectrum-management functions are required for cognitive radios. Spectrum-management functions are classified as:

a. Spectrum analysis

b. Spectrum decision

Functioning's of cognitive radio:

Power Control: Power control usually used for spectrum sharing CR systems to maximize the capacity of secondary users with interference power constraints to protect the primary users.

Spectrum sensing: Detecting unused spectrum and sharing it, without harmful interference to other users; an important requirement of the cognitive-radio network is to sense empty spectrum. Detecting primary users is the most efficient way to detect empty spectrum. Spectrum-sensing techniques may be grouped into three categories.

Transmitter detection: Cognitive radios must have the capability to determine if a signal from a primary transmitter is locally present in a certain spectrum. There are several proposed approaches to transmitter detection.

Matched filter detection: When the information of the primary user signal is known to the secondary user, the optimal detector in stationary Gaussian noise is the matched filter since it maximizes the received signal-to-noise ratio (SNR). While the main advantage of the matched filter is that it requires less time to achieve high processing gain due to coherency, it requires a priori knowledge of the primary user signal such as the modulation type and order, the pulse shape, and the packet format.

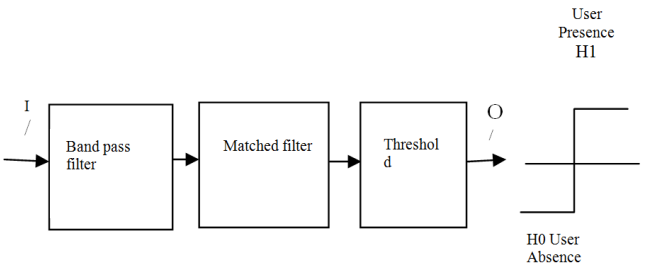

Fig1: Matched Filter Detector

Power detection: Energy detection is a spectrum sensing method that detects the presence/absence of a signal just by measuring the received signal power. This signal detection approach is quite easy and convenient for practical implementation. To implement energy detector, however, noise variance information is required. It has been shown that an imperfect knowledge of the noise power (noise uncertainty) may lead to the phenomenon of the SNR wall, which is a SNR level below which the energy detector can not reliably detect any transmitted signal even increasing the observation time. It has also been shown that the SNR wall is not caused by the presence of a noise uncertainty itself, but by an insufficient refinement of the noise power estimation while the observation time increases.

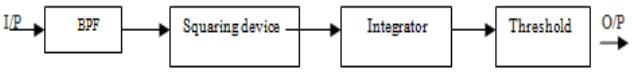

Fig2: Block diagram for power detector

Cyclostationary-feature detection: These type of spectrum sensing algorithms are motivated because most man-made communication signals, such as BPSK, QPSK, AM, OFDM, etc. exhibit cyclostationary behavior. However, noise signals (typically white noise) do not exhibit cyclostationary behavior. These detectors are robust against noise variance uncertainty.

The aim of such detectors is to exploit the cyclostationary nature of man-made communication signals buried in noise. Their main decision parameter is comparing the non zero values obtained by CSD of the primary signal. Cyclostationary detectors can be either single cycle or multicycle cyclostatonary.

III. PROPOSED SYSTEM

Power Detection technique (PD) is a non cooperative type of detection technique. It is one of the easy detection techniques because of the information behind the input signal are not needed for detection process and hence it is named as "null signal detector". In power detection technique, spectrum can be sensed through power calculation. Power detector model detects the spectrum by measuring the input signal's power value with appropriate frequency band, and it is said to be action meter. The spectrum is used or not decides by received signal power value.

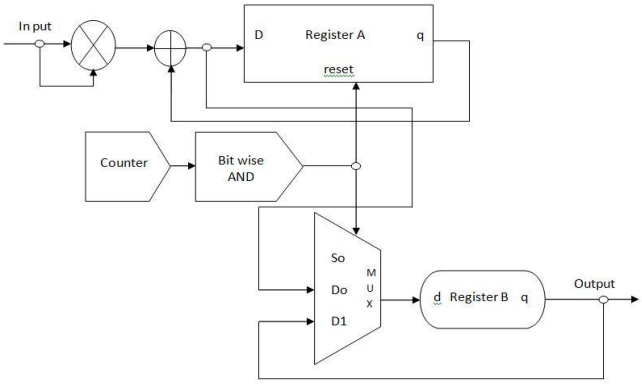

Figure 3: proposed power detector architecture

The power detector Architecture implemented based on VLSI.

The power detector model individual blocks are their, these are multipler, adder, register A, counter, bitwise AND, 2X1multiplexer,register.multipler acts as a squaring unit, adder produces a average value. This entire architecture is tested by providing various discrete samples of signals as an input to this detector.

The input signal enters to the multiplier the signal samples are multiplied, multiplier produces squared value of the input samples. The squared samples are summarized by the giving it to the adder and accumulated on register A.

In register A the signal will be reset these signal is passed through counter block in counter the signal will be allow and set the counts. This Architecture using 16-bit counter because of higher number of sample detection purpose, it given proficient accuracy in performance.

In this detector apply 8-bit input signal samples then the signal samples promoted 16-bit samples because squared the value. The squared signal is reset in register A then passed bitwise AND.

This architecture counter is designed to 0 count, counter is allow the signal and count 0,then its generate count value "1"by bit-wise AND unit, bit-wise AND is coded to generate either"1" or "0" as an output. Register A is store a value or transfer it.

In this architecture using 2X1 Multiplexer. Multiplexer unit is used to select the signal from its two input (one is energy value of samples and another is output signal from Register2 block).Whenever the selection line of MUX is set to "1", it selects the energy value of 16samples and its output is directly applied to register B. Multiplexer used in the architecture is for selecting the appropriate signal by the help of its selection lines.

Here 2x1MUX is used to select the adder units output and the output of register2 by applying "1" and "0" to its selection line respectively. Thereby the measured value is compared with fixed value to detect the presence of signal.

IV. RESULTS

At the beginning, individual modules are designed independently and the entire model is collectively implemented afterwards. The proposed architecture of energy detector block is coded using a standardized hardware description language, verilog. Thereby, the presence or absence of the signal is decided.

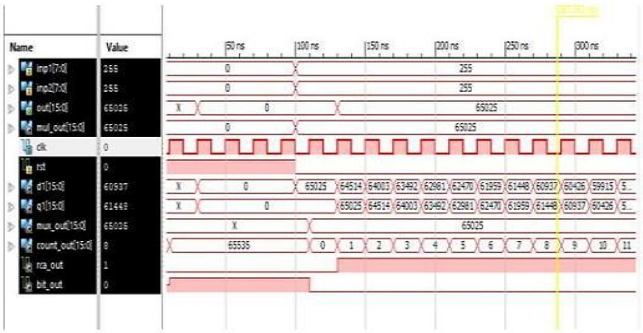

Figure 4: Simulation waveform of architecture using ripple carry array multiplier and ripple carry adder

Figure 3: Power Estimation of architecture using ripple carry array multiplier and ripple carry adder

V. CONCLUSION

This project provides a newly optimized energy detector architecture implementation based on VLSI and such energy detection block can be developed by verilog HDL using XILINX ISE Design suite 14.7 software. Since it has

reduced computational and implementation complexity while compared with other alternative techniques.

Even though it is simple and popular, the performance is limited than other sensing schemes. In order to improve such performance of energy detection in cognitive radio, the task of performing comparison of energy value with threshold value is important.As an extension, the existing project can be evaluated by using FPGA Zed board.

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Area Delay Efficient Binary Adders in QCA

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Abstract— Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. This paper presents an optimized reversible BCD adder using a new reversible gate. A comparative result is presented which shows that the proposed design is more optimized in terms of number of gates, number of garbage outputs and quantum cost than the existing designs.

I. INTRODUCTION

Reversible logic is an interesting area, which is highlighteddue to its involvement in numerous technological design implementations. It is one of the potential techniques in the field of nano scale engineering where power dissipation reduction is a major criteria. The existing technologies are more prone to the heat dissipation, which is a major disquiet from the point of designer as well as end user. When the designer introduces a new design, as example mobiles, which include highly scalable technology may use impractical and in adequate range of parameters such as voltage or temperature. The major advantage of any design with reversible logic is complete reduction of power dissipation, which results in zero heat-generated products. Investigations based on irreversible logic shows that the energy lost on every bit of information is kTln2 joules; where T is absolute temperature and k is Boltzmann constant.1 Such energy lost would not occur if the process uses reversible method.2 This is because the amount of energy that is dissipated has a direct connection with the number of bits that are erased during the computation. This result in a circuit with reversibility technique, in which any bit of information will not lose energy while employing the reversible computation, where as the reversible computation is performed using reversible gates.3,4 Despite of their large area, reversible gate designs are proved their low power advantage compared to their counter designs using CMOS logic. The important measuring parameters for logic design using reversible gates includes the number of gates usedfor the design with less number of unused outputs alsocalled as garbage outputs. The optimized design also concerned about minimum number of inputs, which are left constant. The crucial design aspect for reversible logic lies in reduction of number of unused outputs because the accumulation of garbage by at least single digit causes an exhaustive and excessive execution of the circuit. Hence, a very important design aspect of reversible logic is to use less number of garbage bits. One of the design aspects behind reduction of garbage outputs is to use large number of gates in the circuitdesign. Dynamic programming is the one that allows the user with lowest garbage count during the synthesisstep. Circuit that uses Toffoli and Fredkin reversible gates results in minimal garbage. Switches that use “don’t cares” also results in minimal garbage. Quantum technologies are the one that may use reversible logic. An example of complex antenna simulation design in which reversible logic is implemented in hidden but may not be seen as a separate logic. However, the importance of simulation reveals the reversible transformation in the process of propagating a wave.

II. MATERIALS AND METHODS

In this paper, BCD adder is implemented in two waysprimarily using logic gates in traditional way and the same using reversible logic Gates, the corresponding flowchartshown in Figure 1 represents algorithm steps required.

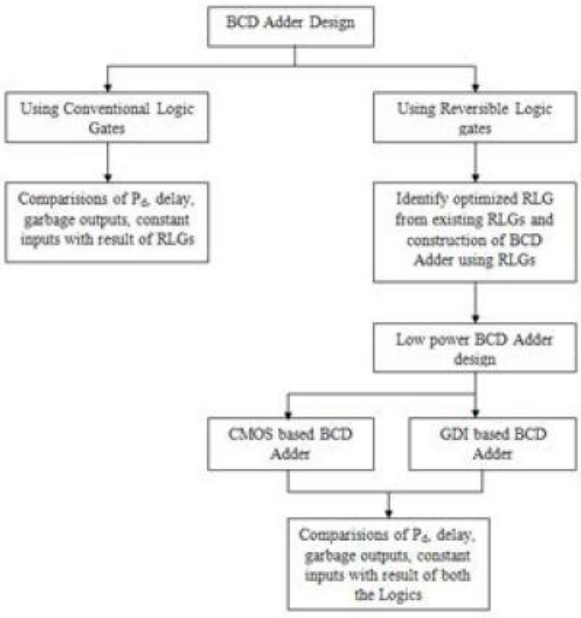


Figure 1. Flowchart.

Traditional BCD Adder

The traditional BCD adder is implemented by considering logic gates as shown in Figure 2. It uses two 4-bit adders and one correction circuitry in which OR and AND Gates were used.

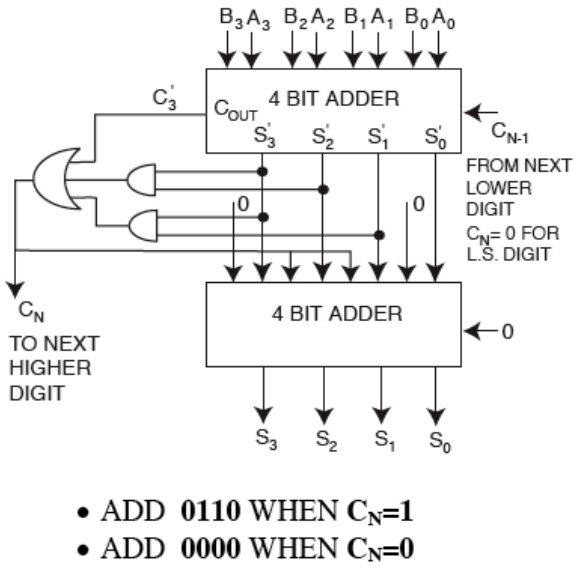


Figure 2. Conventional BCD Adder

III. DESIGN OF BCD ADDER USING RLG

Reversible Logic Gates (RLG) is differentiated based on their complexity and input/output relation. Basic RLG's exists with sizes from minimum 2x2 to maximum 5x5 input/output combinations. The proposed work considered three types of RLG's namely HNG, TSG and BBCDC for the design of BCD adder.5

HNG GATE

A HNG (Hybrid New Gate) is a basic RLG gate, which uses four variables for input/output combinations as shown in Figure 3. The best implementation of this gate isripple carry adder since using single gate itself it produces sum as well as carry output hence reduces the number of

garbage and gate counts

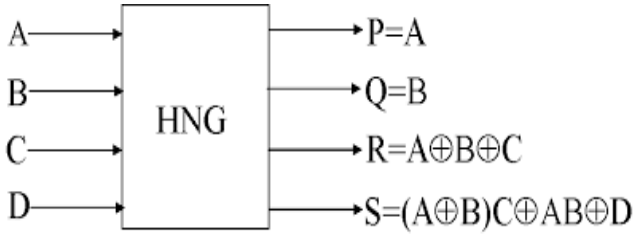


Figure 3. HNG 4x4 Gate.

TSG Gate

Figure 4 shows TSG gate implementation for full adder.If the input C is made zero then the circuit acts like a full adder and the output R gives the sum and the output Sgives the carry out.

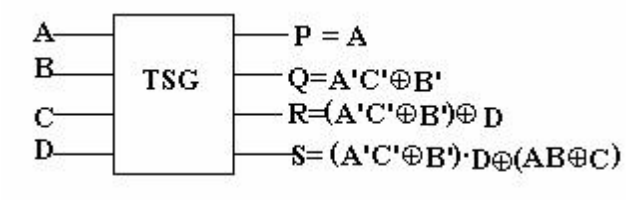


Figure 4. TSG 4x4 Gate.

BBCDC Gate

A BBCDC (Binary to BCD conversion) is a 5X5 reversible gate shown in Figure 5, is used in the implementation of BCD adder.9 Table 1 shows the corresponding input/ output vectors. Design of BCD adder using reversible BBCDC gates is shown in Figure 6, which requires a minimum of nine inputs A0-3, B0-3 and five outputs in which four bits are for sum bits S0, S1, S2, S3, and Cout.5-17 Four bits are required to code the augends, which makes eight bits, and including circuit carry bit it makes the nine bits input.

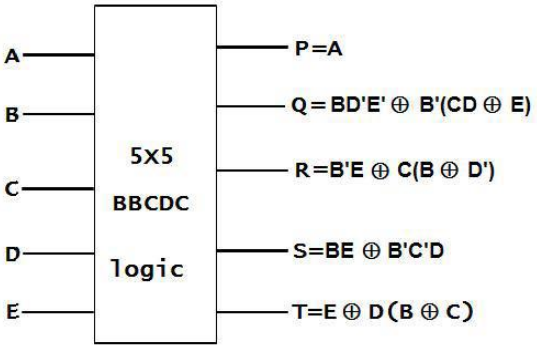


Figure 5. BBCDC 5x5 Gate.

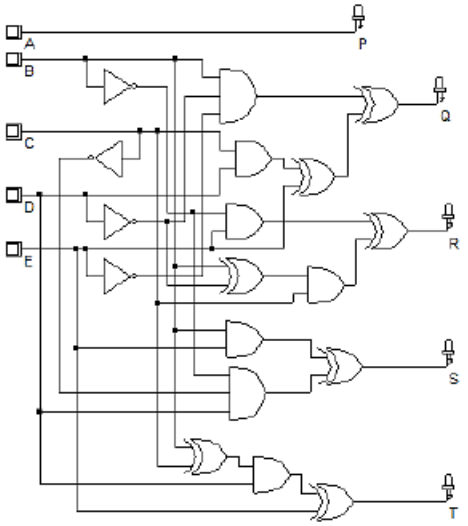


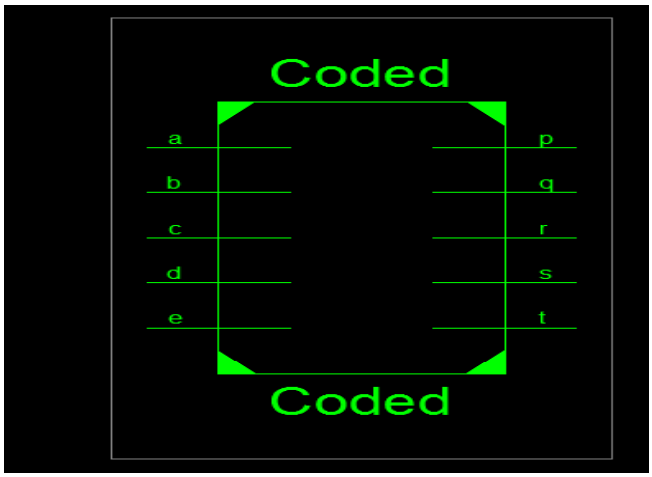
Figure 6. BBCDC 5x5 Gate.

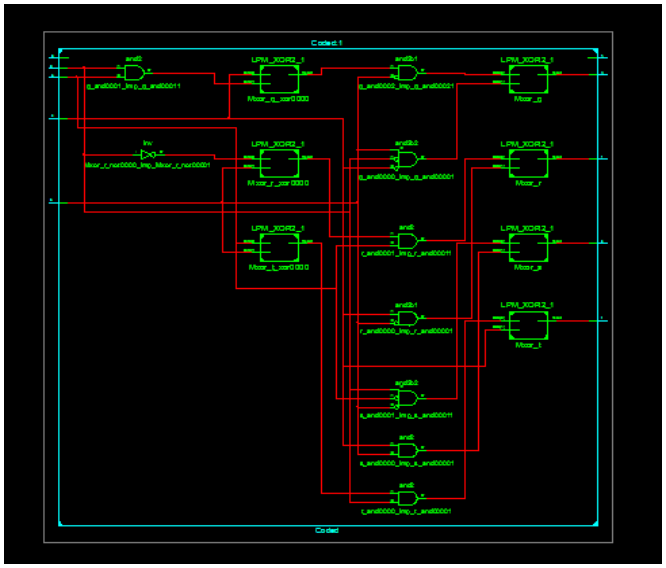
Table 1. Truth table of BBCDC Gate

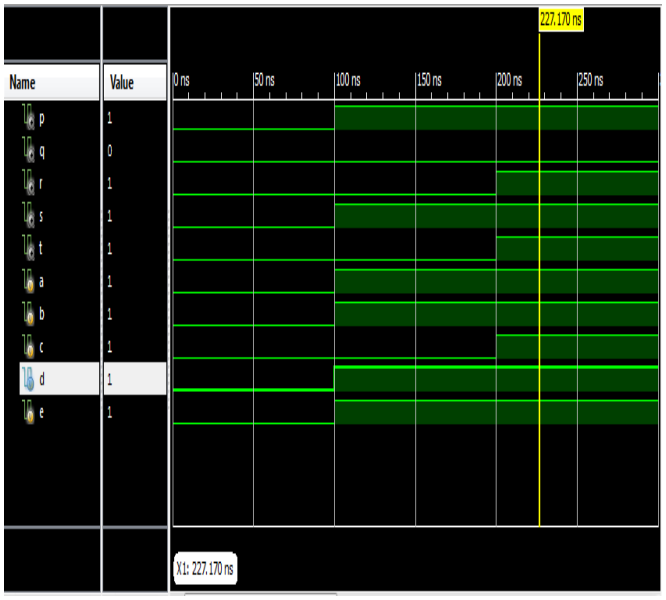
Inputs					Outputs				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Consider adding 9+9+1 in decimal, gives 19, instraight binary this should produce an output of 100112,but this is an invalid number in BCD. Because in BCDcode the four bits binary which only represents decimal numbers 0-9. Table1 shows decimal numbers 0-19 with their binary and BCD codes.

IV. SIMULATION RESULTS







V. CONCLUSION

Low power BCD adder was implemented using BBCDCreversible logic. Different parameters such as number of unused outputs, constant inputs, delay, area, number gates used, power, and PDP are compared for different BCD adder logic designs.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Design and Simulation of Semicoupled 12T transistor Based SRAM USIN 15nm Technology

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Abstract— Technology is contracting down rapidly and almost all the low power gadgets require memory which works faster, considering that new high speed SRAM cell has been designed. The designed 12T SRAM cells also consume less power. In our design, transmission gates have been used as access transistors. The Simulation results such as power dissipation, delay, PDP (Power Delay Product) of the proposed SRAM cell have been calculated and contrasted with those of some other existing models of SRAM cell. In this present work a novel low power 12T SRAM cell is proposed. A charge recycling technique is used to minimize the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

I. INTRODUCTION

Usage of SRAM based cache memories has increased over years for portable devices, mobile phones and all kinds of multimedia devices to attain high speed. Low power and high speed performance is the major puzzling task for Integrated circuit design in Nano scale technologies as VLSI chips are in demand in mobile communications and computing Devices. Since there is a wide spread use of battery powered smart devices, Nano medical devices, low power process has turned out to be a serious problem with system on chip design (SOC).In order to analyze an SOC we can consider a low power SRAM because it occupies the major portion of area in the SoC, it really disturbs the overall power of SOC. Depending on how frequently we access the SRAM cell the power consumption varies largely. If we use a SRAM cell at high frequencies it consumes much power but at the same time if we use it at a slower speed in applications with moderately clocked microprocessors it consumes almost negligible power. There are many techniques for managing power in SRAM based memory structures. The adverse effect of variations in the threshold voltage (Vth) becomes substantial at low operating voltages as SRAM cell is vastly susceptible to the differences in Vth. For a low power procedure in a conservative 6T SRAM cell a lot of adjustment is required between READ and WRITE operations to obtain required stability.

2. SRAM CELL DESIGN A. 7T, 8T, 10T, 12T Cell Design From the figure 1 we can observe that the 7T SRAM-cell schematic which is utmost usually used SRAM cell structure. It has a stumpy fixed power indulgence. However, There is a problem existing with this SRAM- cell structure, ie., lack of potential stability. During the read operation at a node V1 of NMOS (N1) touches the beginning voltage(Vth) of NMOS N2, it will be turned on and pull down the voltage at node V2 to "0" this results PMOS (P1) is turned on and pull up the voltage ant node V1 due to positive feedback mechanism. A new architecture of an 8T SRAM implementation was suggested [1], to decrease problem during the read operation, for which the data retaining component and the data output component should separate by using separate read/write bit and read/write word gesture lines. In turn, the cell employment offers a read-interrupt-free operation. However, this implementation uses eight transistors, which results in a cell area increase of 30% in contrast to the conservative 7T-cell design.

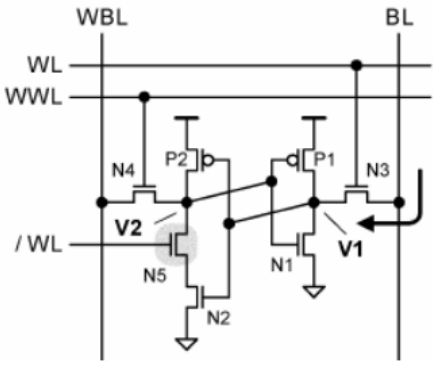

Fig1:7T SRAM schematic

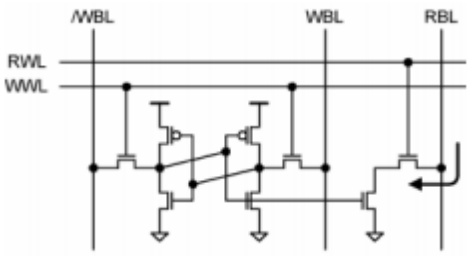

Fig2:8T SRAM -Cell schematic

The 7T cell design [2] also employs dispersed read and write signal lines but uses only one extra NMOS transistor to achieve read-disturb-free operation, thus increasing the

cell area by 13%. NMOS transistor, whose gate is controlled by signal WL, is additional between node V2 and NMOS transistor, to the 7T-cell design as seen in Fig. 1.

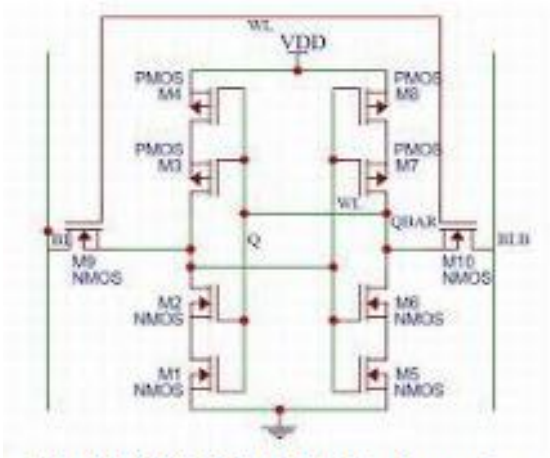

Fig3:10T SRAM -Cell schematic

Whereas the cell is being accessed, WL is set to "0" to turn off NMOS transistor. In the case of a "0" read, even if the voltage at node V1 reaches the Vth of NMOS transistor N2, node V2 cannot be pulled down to "0" and thus preserving the stored data. During data retention period, WL is set to "1", and the cell operates in the similar process as the 6T-cell circuit. A 10T SRAM cell in figure3 has a read buffer on each side to improve the read performance and also write buffer on each side to progress the write performance apart from that it has six main body transistors which make its functionality similar to that of a 6T SRAM cell. Further to improve the steadiness of the SRAM device a 12T transistor SRAM is proposed as shown in figure4 with one transistor on the top and the other in the bottom connected to Vdd and Gnd respectively

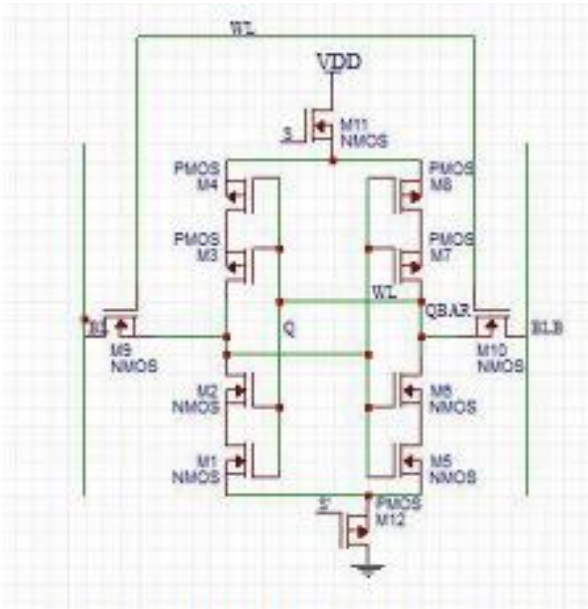

Fig4:12T SRAM -Cell schematic

Table1: Performance comparison of 7, 8, 10 and 12-Transistor topologies

S.No	Bit cell	SNM	Power consumption	Supply voltage
1	7T	290mv	20nw	1V
2	8T	310mV	25nw	1V
3	10T	330mV	30nw	1V
4	12T	340mV	33nw	1V

Table1 shows the comparison of various presentation metrics related to static noise margin, power dissipation and supply voltage of different topologies. 3. C.STATIC-NOISE-MARGIN (SNM) The SNM is used to measure the SRAM cell steadiness. It is the extreme value of a dc disturbance that can be accepted by the cell before changing states [3]. Graphically, the SNM is characterized by the major square box that can be tailored in the butterfly characteristic curves of the SRAM cell [3]. The three designs in above figure were simulated such that all transistors are minimum-sized devices to achieve minimum cell area. During the read operation, the SNM is much smaller for the 6T design because the characteristic curves are tainted by the voltage separator among the access transistors (N3 and N4) and the drive transistors (N1 and N2). Without the read-disturb, the characteristic curves of the 8T design is that of two cross fixed inverters, which provide a larger SNM (Fig.6). Figure 5 shows the characteristic curves for the 7T design during its retention period and read access period. For a "0" read, the SNM for the 7T design is much larger than that for the 6T design, and thus improving the stability of the SRAM cell. Yet, if a time limit is set (word line is only active for a finite amount of time), the SNM actually increases as VDD decreases. This is since at a minor VDD, the cell current drawn from the bit line is smaller during a "0" read, so the charge stored onto the parasitic capacitance at node V1 is less, thus a lower voltage at node V1 is touched after a short amount of time, which means more static noise voltage can be tolerated before the cell change state. Here, SNM is the largest Vn that causes a state change in the cell after 400ps. Note that SNM is affected by the device ratio between the access transistors (N3 and N4) and the drive transistors (N1 and N2). Finally, figures below demonstrates that device mismatch degrades the SNM. Here, mismatch is introduced to the drive transistor N1. (1% mismatch is equivalent to WN1 = 0.99Wmin). In practice, process induced variations is not only limited to device geometry mismatch but also includes threshold voltage variability, which is not modeled in the simulations of this project. Therefore, SNM degradation can be more severe in reality

II. CONCLUSION

Designed four SRAM cell topologies of 7T, 8T, 10T and 12T stability performances have been presented. The speed of SRAM cell is increased based on the process technologies continue to advance, but devices will be more vulnerable to gaps, which damage the static-noise margin of SRAM cells. Due to performance concerns, the dual port

designs that shows read disturb-free feature such as that seen in the 7T and 8T cell implementation might become more practical in the future SRAM cell implementation. And further if the technology is scaled beyond 45nm in order to increase the performance, performance of the device in terms of speed and power dissipation can be achieved by replacing CMOS with FinFET devices and also by applying different power reduction techniques.

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Reinforcing the Black Cotton Soil Subgrade by Using Stone Dust

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Abstract— Soil stabilization is the interaction that includes upgrading the actual properties of the soil to improve its strength by mixing or blending in with added substances. The various sorts of techniques utilized for soil stabilization are Soil stabilization with concrete, Soil stabilization with lime, Soil stabilization utilizing bitumen, chemical Compound stabilization, and another arising innovation of stabilization. In this investigation, we are utilizing stone dust as Material for the stabilization of soil. With the acquaintance of stone dust with the soil, the CBR esteems will improve and in this manner the thickness of the asphalt layer likewise gets decreased. It likewise decreases the force of weight on sub evaluation. Stone dust is effectively accessible, eco-accommodating, and furthermore financially savvy. The CBR estimation of the soil with the expansion of 0.25%, 0.5%, 0.75%, and 1.0%, stone dust by weight of soil is discovered to be expanded. From the restricted research facility study directed we presumed that the 0.75% of stone dust fiber can considerably improve the properties of black cotton soil. Also, consequently 0.75% of stone dust fiber is the ideal fiber content for black cotton soil to resist the stresses from the top of the pavement.

I. INTRODUCTION

A non-industrial nation like India which has an enormous topographical territory and populace, requests huge framework for example organization of streets and structures. In India, soils are characterized into six gatherings specifically alluvial soil, marine soil, laterite and lateritic stores, sweeping soils, sand ridges and stone deposits[1]. On a normal 1 lakh sq.km region is covered by lateritic soil stores, 3 lakh sq.km region is covered by dark cotton soil, and 5 lakh sq.km region is covered by sand dunes[2]. Experiencing land having delicate soil for development prompts a consideration towards receiving ground improvement strategies, for example, soil adjustment [3].

Soil adjustment is the cycle which includes upgrading the actual properties of the dirt to improve its solidarity, solidness and so on by mixing or blending it in with added substances. Geo engineered materials are manufactured items produced using different sorts of polymers which might be either Woven or Non-Woven[1]. These are utilized to improve the attributes of soil and have given a useful method of developing structural designing constructions financially [6].In this investigation, we are utilizing stone residue as geo manufactured material for adjustment of soil. With the acquaintance of stone residue with the dirt the CBR esteems may improve and thickness of asphalt layer additionally may get decreased [5]. It might likewise decrease the force of weight on subgrade. Stone residue are such a materialwhich is effectively accessible, eco-accommodating and furthermore savvy [7]. With the utilization of soil adjustment strategy in development measure the general expense may get decreased when contrasted with the common technique for development.

1.1.Needs and Advantages of soil stabilization

Soil properties fluctuate an extraordinary arrangement and development of constructions relies a great deal upon the bearing limit of the dirt, consequently, we need to settle the dirt to improve the heap bearing limit. The degree of the dirt is likewise a vital property to remember while working with soils. The dirts might be very much reviewed which is alluring as it has less number of voids or consistently evaluated which however sounds stable yet has more voids[5].

Advantages of soil stabilizations are as follows

- In the event that during the development stage Weak soil layers are experienced, the typical practice followed is supplanting the feeble soil with some other great quality soil. With the use of soil adjustment method, the properties of the locally accessible (soil accessible at the site) can be upgraded and can be utilized viably as the subgrade material without supplanting it.
- The expense of setting up the subgrade by supplanting the Weak soil with a decent quality soil is higher than that of setting up the subgrade by balancing out the locally accessible soil utilizing distinctive adjustment strategies.
- The strength giving boundaries of the dirt can be adequately expanded to a necessary sum by adjustment.
- It improves the strength of the dirt, in this way, expanding the dirt bearing limit
- It is more practical both as far as cost and energy to build the bearing limit of the dirt instead of diving for deep establishment or pontoon establishment.
- It is likewise used to give greater strength to the dirt in slants or other such places.

- At times soil adjustment is likewise used to forestall soil disintegration or development of residue, which is extremely helpful particularly in dry and dry climate.
- Adjustment is additionally accomplished for soil water-sealing; this keeps water from going into the dirt and consequently helps the dirt from losing its solidarity.
- It helps in diminishing the dirt volume change because of progress in temperature or dampness content.

II. II.EXPERIMENTAL INVESTIGATION

CBR value and shear strength for various grouping of Geo manufactured material with black cotton. The method for California Bearing Proportion (CBR) Test has been performed dependent on IS 2720 (Section 16) – 1987[16]. The CBR rate esteems for various soils are determined for 2.5mm and 5mm entrance by a standard loads of 1370 and 2055 Kilograms respectively.The CBR esteem distinctive proportioning of Geosynthetic stone residue at 2.5mm and 5mm is determined utilizing equation 1

$$CBR = PT/PS \times 100 \quad (1)$$

where PT = Corrected test load corresponding to the chosen penetration from the load penetration curve.

PS = Standard load for the same penetration

III. DATA ANALYSIS

California Bearing Ratio (CBR) on Black cotton soil with mixing Optimum Moisture Content (OMC) shown in Table 1and the soil CBR alone has been shown in the Table 2 and the values of CBR with mixing of 0.25%, 0.50%, 0.75% and 1.0% Stone dust are shown in Table 3,Table 4,Table 5 and Table 6 respectively.

Table 1. OMC adopted for Black cotton soil

Type of Soil	OPTIMUM MOISTURE CONTENT (OMC)				
	Plain Soil	Soil+0.25% SD	Soil+0.5% SD	Soil+0.75% SD	Soil +1.00 % SD
Black Cotton Soil(BCS)	19%	20.10 %	19.00 %	17.20%	16.90%

The CBR estimation of soil alone was discovered to be 1.82% and soil with expansion of 0.25%, 0.5%, 0.75% and 1.0%, stone residue by weight of soil is discovered to be 3.49%, 3.96%, 5.41% and 3.96% separately. The California bearing proportion (CBR) of the dark cotton alone is acquired as 1.82% individually as well as dark cotton soil it has expanded to 5.41% rate in the wake of balancing out it with ideal level of stone residue fiber the accompanying entrance to the Heap in kilograms are been appeared in the diagrams of Figure 1 to 5.

a. CBR Test on Black cotton soil

Table 2.CBR Test on Black cotton soil

Penetration (mm)	CBR Test on Black cotton soil		
	Trial 1	Division	Load (kg)
0	0	0	0
0.5	0.8	4	6.4
1	1.8	9	14.4
1.5	2.4	12	19.2
2	2.8	14	22.4
2.5	3	15	25
3	3.2	16	25.6
4	3.6	18	28.8
5	4	20	32
7.5	4.6	23	36.8
10	5	25	40
12.5	5.6	28	44.8

b. CBR Test on Black cotton soil +0.25% SD

Black cotton soil added with fibers 0.25% by weight the following observations were

made: OMC = 20.1%

Table 3.CBR Test on Black cotton soil +0.25% SD

Penetration (mm)	CBR Test on Black cotton soil		
	Trial 1	Division	Load (kg)
0	0	0	0
0.5	2	10	16
1	3.6	18	28.8
1.5	4.6	23	36.8
2	5.4	27	43.2
2.5	6	30	48
3	6.4	32	51.2
4	7.2	36	57.6
5	7.8	39	62.4
7.5	8.8	44	70.4
10	9.4	47	75.2
12.5	10	50	80

Load as obtained from graph at 2.5 mm penetration = 48 kg

CBR of Specimen = (48/1370) *100=3.49%

Load as obtained from graph at 5 mm penetration = 62.4 kg

CBR of Specimen = (62.4/2055) *100=3.02%

c. CBR Test on Black cotton soil +0.50% SD

Black cotton soil added with fibers 0.5% by weight the following observations were

made: OMC = 19.00%

Table 4.CBR Test on Black cotton soil +0.50% SD

Penetration (mm)	CBR Test on Black cotton soil		
	Trial 1	Division	Load (kg)
0	0	0	0
0.5	2	10	16
1	3.8	19	30.4
1.5	5	25	40
2	6	30	48
2.5	6.8	34	54.4
3	7.6	38	60.8
4	8.8	44	70.4
5	9.8	49	78.4
7.5	11.4	57	91.2
10	12.4	62	99.2
12.5	13.4	67	107.2

Load as obtained from graph at 2.5 mm penetration = 54.4 kg

CBR of Specimen = (54.4/1370) *100=3.96%

Load as obtained from graph at 5 mm penetration = 34 kg

CBR of Specimen = (78.4/2055) *100=3.80%

d. CBR Test on Black cotton soil +0.75% SD

Black cotton soil added with fibers 0.75% by weight the following observations were

made: OMC = 17.20%

Table 5.CBR Test on Black cotton soil +0.75% SD

Penetration (mm)	CBR Test on Black cotton soil		
	Trial 1	Division	Load (kg)
0	0	0	0
0.5	4.2	21	33.6
1	6.2	31	49.6
1.5	7.6	38	60.8
2	8.6	43	68.8
2.5	9.8	49	78.4
3	10.6	53	84.8
4	12	60	96
5	13.2	66	105.6
7.5	15.4	77	123.2
10	17.2	86	137.6
12.5	18.8	94	150.4

Load as obtained from graph at 2.5 mm penetration = 78.4 kg

CBR of Specimen = (78.4/1370) *100=5.41%

Load as obtained from graph at 5 mm penetration = 105.6 kg

CBR of Specimen = (105.6/2055) *100=5.12%

e. CBR Test on Black cotton soil +1.00% SD

Black cotton soil added with fibers 1.0% by weight the following observations were

made: OMC = 16.9%

Table 6.CBR Test on Black cotton soil +1.00% SD

Penetration (mm)	CBR Test on Black cotton soil		
	Trial 1	Division	Load (kg)
0	0	0	0
0.5	2	10	16
1	3.4	17	27.2
1.5	4.6	23	36.8
2	5.8	29	46.4
2.5	6.8	34	54.4
3	7.6	38	60.8
4	9	45	72
5	10	50	80
7.5	12.2	61	97.6
10	14	70	112
12.5	15.6	78	124.8

Load as obtained from graph at 2.5 mm penetration = 54.4 kg

CBR of Specimen = (54.4/1370) *100=3.96%

Load as obtained from graph at 5 mm penetration = 80 kg

CBR of Specimen = (80/2055) *100=3.88%

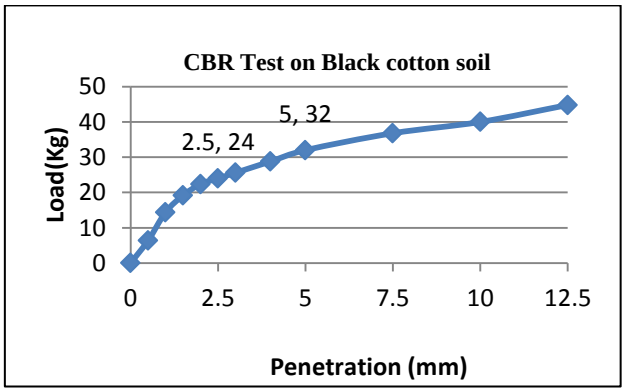

Figure 1: CBR Test on Black cotton soil

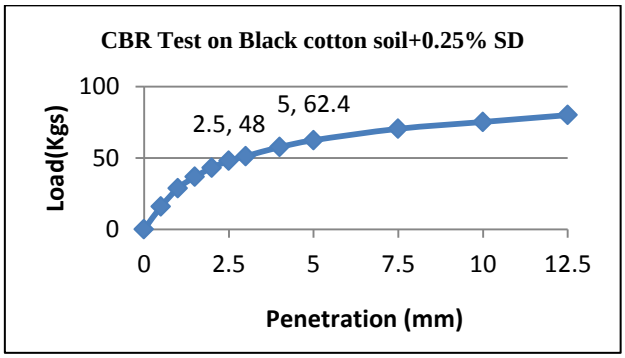

Figure 2: CBR Test on Black cotton soil+0.25% SD

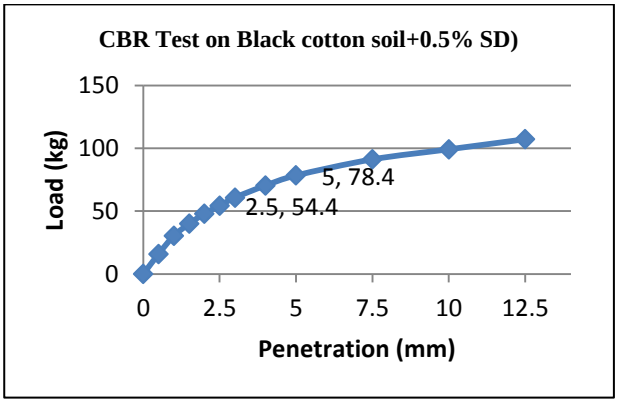

Figure 3: CBR Test on Black cotton soil+0.50% SD

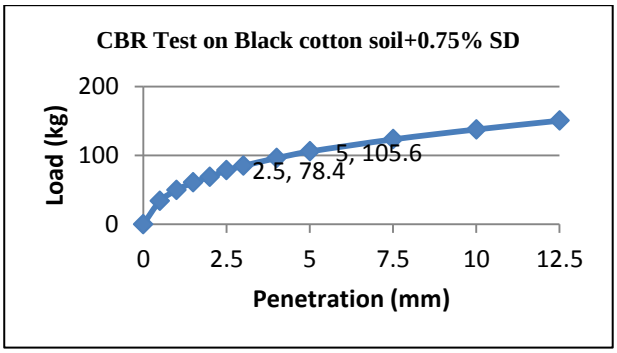

Figure 4: CBR Test on Black cotton soil+0.75% SD

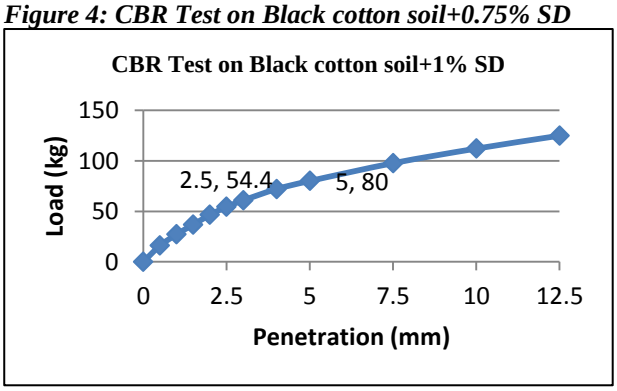

Figure 5: CBR Test on Black cotton soil+1% SD

IV. CONCLUSION

Black cotton soil with combination of 0.75% of stone dust has shown higher strength maximum dry density compared to regular black cotton soil . By using this mix combination in pavement sub grade can reduce the use of conventional materials like course aggregates. the increased CBR strength in sub grade can reduce the thickness of the pavement.. Stone dust creates dumping issues and air pollution when it is exposed to the environment. The usage these industrial waste products in below surface layers of pavement, it leads to decrease of the pollution by industrial waste.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Effectual Use of Coal Mine Waste in the Production of Eco Friendly Bricks

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Abstract— In India coal mining is essentially doing by the human needs and necessities like electricity generation. The coal mining is majorly done for the extraction of coal and with that we can generate the electricity. Due to the extraction of large area annually millions of tons of waste is generating in the form of shale's, rocks and tailings. It is settled over the soil surface like a hill. However coal tailings are used as wall or tall hill after the complete mining. The extracted soil, which is blended with calcium, lime, fly-ash and other minerals can be reused and recycled. Coal mining can be done mostly over the sides of the river banks, due to the flotation of molten lava in the past centuries. So the soil or rock beneath it is burned or combusted and from that coal is formed and covered up with soil. That stored coal is extracted and used for power generation. In this research we are taking the waste generated materials like shale's rocks and tailings to manufacture the clay bricks.. The taken waste soil materials are mixed up with black cotton soil which is a general material in the manufacture of bricks. It is compacted thoroughly and burnt at a temperature of 12000c to form a brick. So that bricks can be used as a building construction material. The over burnt brick can be tested further for the flexural testing to find out the strengthening properties.

Keywords— Bricks, Coal mine waste, Flexural testing, Reuse and Recycling.

I. INTRODUCTION

Coal mine waste generation is a large pollutant in the world, which is largely growing in coal producing counties. As per the records india is the largest producing coal waste country in the world after china. The generated and digged materials were pored over the soil and it will be glowed like as a hill. That will leads to the environment pollution as well as the soil erosion. The dust that is floats in the air and cause air pollution. In the same way the raw minerals and chemicals in the coal waste will leads to the soil erosion. It will effect on the soil to degradation and stops the growth of plants. To overcome this situation the waste generated can be recycled and reused. In both Andhra Pradesh and Telangana two coal mine industries are there. One is singareni and other one is ellendu. The coal mine company and the coal mines were located over the side of river bed. Lots of coal resources are available in these areas to generate the coal. With the extracted coal it is been using for power generation. The dumps were dumped over the large areas and the utilization of those was being done by growing neelagiri plants. The one and only tree that can grow over those soils. The recycling and reusing can be done by restoring with the manufacture of raw materials. In the world lots of researches were being conducted on the coal mines by reusing them to make mud bricks and cement bricks. So that an amount of waste can be reused and recycled.

II. II. LITERATURE REVIEW:

Shailendra Kumar Singh, Ramjeet singh 2020 mentioned the making of bricks from using the coal mine waste of chattisgarh locality. The bricks were made with the coal waste, Sodium silicate and ordinary Portland system with a size and shape of 9"5"3" dimensions. After the brick manufactured it is exposed to atmosphere for 24 hours. To find out its strength characteristics, water absorption test and compressive test were conducted. At the end they have concluded in the result as a compressive strength of 9.5 N/mm^2 was recorded and made a significant usage can be deployed and it can reduce the environment pollution.

Hossain MdAnawar Et al.2020 were done a deep study on coal mine industries like how much of coal is generating per annum in metric tons year wise over the countries. The waste that generating are gradually becoming like tailing to use for no purpose and making hazardous to the environment. In this scenario these have mentioned the materials that can be recycled and reused. Those are of fly-ash, coal, and tailings. They have also mentioned that how the waste is also being controlled and how it is going to reduce the coal waste.

Yassine Taha Et al.2017 were recycled coal mine waste materials to make eco friendly bricks. In this first they were considered coal mine waste rocks CMWR, and secondly Treated coal mine Tailings TCMT. The collected materials were burned at 1020^0 c and the gases were emitted. The fine material then mixed together to form the making of bricks. After making the bricks they tested it for flexural strength test and porosity and water absorption test and concluded a significant usage of bricks can made.

Moises Frias Et al.2016 were recycled the tailings from the coal mines and reused in the manufacture of cementatious material. In this paper they were explored the significance of waste materials to reuse and converting it into pozzolona. In the finding they have showed that the

presence of 20% activated coal mine waste favors the formation of cementatious materials and aluminous phases.

Adibee, N Et al.2013 were discussed on waste generated coal mines generate sulfur residues and contaminate the soil. The disposal of such materials had to inert and recycled for reuse. In this article they have mentioned the impacts of waste dump on the environment and how it can be resolved. The collected data was compared to the previous waste dump storage and mentioned the level of increase. They have concluded to growth the forestry by planting zelkava trees.

Bian, Z Et al.2009 have done a deep study on tones of coal mine residues to generate in annually and how that is going to be utilized to recycle and reuse. In this they have mentioned the disposal techniques to control the coal mine waste that are generating from coal mine industries. They have also discussed that how the pollution is going to be controlled by using these techniques.

III. III. MATERIALS USED:

Coal mine waste: Coal mine waste is generated from the coal mine industries, where large quantities of coal waste are produced. Most of the waste is coal dust and remaining are raw materials like silica, sulphates, shale's and bituminous materials. It is free and soft when freshly digged and after that it will become hard due to atmospheric conditions.

Black cotton soil: Black cotton soil is a most used soil material for making of mud bricks. It is having good bonding properties, so that it can be easily blend and mixed and this soil is also having expansive in nature. Because of its expansive nature, the volume of soil when it is supposed to form a brick will be of 20-30%.

Fly-ash: It is a fine powder generated from the burning of coal from electric power plants. It is a combination of aluminous and siliceous materials. Fly-ash when mixed with water act like a blending material. It is a most often material used in brick manufacturing, which can give excess strength to the mud to bond well.

Rice-husk ash: The rice-husk ash is a waste by product generated from the rice mill industries. It is burned at 500-800 ^{0} c. The husk above the rice burned will form in to black colored ash. It is used in may construction purposes. It is a low cost material and gives some grip as w ell as a porous material. It will help in removal of excess moisture content.

IV. TEST METHODOLOGY:

The following flow chart will give a clear vision on the test methodology.

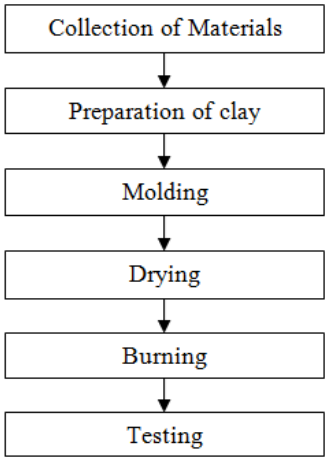

Figure1. Test methodology of brick making

V. EXPERIMENTAL PROCEDURE:

- In the first process of test procedure all the material will be collected together and make ready for preparation of clay.
- After the clay prepared, in a place of pit where all the clay materials will be added with water and compacted to form a mud clayee soil like an expansive soil.
- After the well compaction, the clay is considered to form the brick. The standard size of brick that we are going to manufacture here is 9".4"3".
- The clay material is shifted into the brick mould and is made accordingly. After that the sample is sundried and exposed to temperature. The drying time period is nearly 8 to 9 days.
- The sun dried bricks then burned over a temperature of 1100 ^{0} c.
- The burned brick then tested for water absorption test and flexural test.
- In water absorption test we are determining the durability of the brick. So the amount of water absorption of the brick can be identified.
- Take the empty weight of brick and note the value as M1. Then after the brick is completely immersed in water for 24 hours and after that the weight is noted as M2. the overall percentage can be find from the values substituted in formula. W= [(M2-M1)/M1]*100
- The Flexural test can be conducted through the flexural testing machine. The brick kept under flexural testing machine and the load is applied. So when the maximum load falls on the brick it leads to break at a point. The value can be noted for its performance.

$$\text{Flexural strength} = (3P*L)/BD^2$$

VI. RESULTS AND CONCLUSIONS:

The water absorption test got a test result of 14%. It means the brick as a good absorption in nature. The flexural value

is noted as 1.8 N/mm^2. The results obtained from the tests have shown the significant values that can be used further to form eco friendly bricks and can be adopted in construction of walls.

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Experimental and Thermodynamic Analysis of Biomass Based Producer Gas Fuelled Spark Ignition Reciprocating Internal Combustion Engine

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Abstract— This report summarises the results of the research and development of producing gas-fueled reciprocating internal combustion engines. Biomass has been researched for the production of high-octane, ultra-clean, and low-energy-density producing gas. The parametric impacts of compression ratio and ignition timing on power output for two distinct fuels, namely red gram and cotton stalk biomasses, are investigated and their performance is compared for two different fuels, namely red gram and cotton stalk biomasses. The effective use of producer gas fuel has opened the door to converting a commercially accessible gas engine for large-scale power generation, albeit at a 20-30% power loss. To a much greater extent, the reduction in hazardous emissions compensates for the loss of electricity. These techniques produce less dangerous gas (lower NOx and zero SOx) and zero to GHG.

Keywords— gas engine, producer gas, biomass, compression ratio, ignition timing

I. INTRODUCTION

Recent European measures to reduce greenhouse gas emissions and fossil-based fuel dependence have expanded transport and energy use of alternative fuels. Liquid fuels are favored in transport because of their high energy density per unit amount. Liquid fuels are frequently employed in power generation because of the possibility of more pure combustion than liquid and solid fuels. Biomass gasification has been taken more and more into account as a beneficial option to the use of various biowaste from industrial and agricultural activities and a significant decrease in CO2 emissions. A wide variety of bio-residues are transformed into a gas fuel that can be directly used in internal combustion engines (ICEs), gas turbines, and gas cells in a gasification process and is generally referenced as the syngas when the temperature is between 10 to 28 MJ/Nm3, and the producer gas (PG) at heating value between 4 and 7 MJ/Nm3. Downdraft design is the optimum solution if a gasifiers need to be linked with an ICE, due to its low concentration of tar in the PG produced by the gasification process. The variety of gas compositions, as well as certain misconceptions about auto-ignition propensity at high engine compression ratios and significant power de-rating due to the gas's low heating value, have impeded research on the use of PG in ICEs thus far. Furthermore, while low-heating energy sources can be burned in Dual-Fuel Compressive Ignition Engines, only a small percentage of the literature's experimental experiments focus on 100 percent of PG SI engines (CI). Finally, due to the high fuel consumption of PG during operation, testing of small engines is done often.

II. LITERATURE REVIEW

A vast number of studies on biomass were conducted by researchers in many parts of the world to replace internal combustion (IC) engine fuel. The majority of these tests were reported by the United States, Europe, India, Malaysia, China and Germany. The following is a summary of these experimental findings.

Vyarawalla*et al* (1984) have designed and built a 9 kW biomass-based gasifierengine system for lab tests as well as a 1000-hour field trial utilising sawdust and toorstalks as biomass Compression ignition type engines driven by producer gas from gasifiers could save up to 75% on diesel. Rajvanshi and Joshi (1989) tested and constructed a topless wood gasifier for water pumping with a 3.75 kW diesel engine pump set. It was observed that 1 kWh of energy required 1.33 kg of wood and 125 ml of diesel, and an economic assessment revealed that the gasifier system is economically comparable to a diesel-only fuel with a low (60 percent) diesel substitution.

Parikh *et al* (1989) The performance of direct and indirect injected diesel engines running on producer gas from a downdraft biomass gasifier was examined. As a biomass sample, they utilised Subabooltree (Leucaenalecucocephala). By adjusting the capacity of the gas cooling – cleaning system, they were able to obtain a diesel replacement rate of 68 to 80% at 80 percent of rated load. Dual fuel operation has been proven to result in a significant rise in engine exhaust CO content when using a diesel engine in dual fuel mode. It could only replace diesel at a maximum of 31% of the time. According to Krishna and Kumar (1994), this is owing to the development of clinkers and a low biomass density. Rajvanshi & Jorapur (1997) The development of a low density biomass gasification system for thermal usage on a commercial scale (1080 MJ/h) was proposed. For example, sugarcane leaves, bajra stalks, sweet sorghum stalks, and bagasse can all be utilised as fuel in the gasifier. The findings demonstrate that if the cost of biomass is less than Rs.1350

T-1 for a capacity of 1080 MJ/h, a low density biomass gasifier powered by sugarcane leaves or bagasse can be retrofitted to existing oil-fueled furnaces and boilers in metallurgical and other industries.

Availability of eight selected agricultural residues as raw material for biomass gasification in India with due consideration to their seasonal and geographical availability dimensions were discussed by Tripathi*et al* (1998). Arhar stalks, maize stalks, maize cobs, cotton stalks, mustard stalks, jute and mesta sticks, rice husks, and peanut shells were all tested for biomass residues. According to studies, almost eight million tonnes of these wastes were generated last year, with a main energy potential of around 1200 Peta Joules. Depending on the cost of agricultural waste and the distance travelled, the cost of biomass leftovers vary from Rs. 132/tonne to Rs. 628/tonne. These expenses were significantly lower than India's current coal prices. As a result, these agricultural wastes could be a profitable fuel for biomass gasification and briquetting facilities.

Martin et al (1997) The gassification of wood from the mill was explored which is also like fuel synthesis, incorporated into a combined power generation cycle. This blend makes better use of the gasifier since the synthesised gas is frequently utilised to generate extra energy during the winter season when electricity costs are high, but it is rarely used to produce transportation fuels during the rest of the year. Technology, fabric use, energy utilisation, the environment, and cost-cutting were highlighted as fixed bed and fluidized bed gasifier criteria.

III. PRODUCER GAS ENGINES

3.1 SI engines fuelled with PG

When compared to fossil fuels, facility de-rating in PG-fueled engines is mostly caused by a decline in volumetric efficiency and a decrease in energy density per mixture unit volume (15-30% vs. NG). Fuel conversion efficiency also contributes to power degradation. Based on the minimal statistics discovered in the literature, the cost of gasoline operation might be reduced by 10% to 20%. The plant's decryption can range from 30 to 70% depending on gas quality, and can be reduced in part by boosting the CR engine. Indeed, CO2 and N2, which account for more than 60% of a PG volume, act as a knock and explain why there is more methane than NG. The authors demonstrated that PG engines can operate stable in a lean condition, but their performance degrades when the ratio surpasses 1.5 (actual air to fuel ratio/stoichiometric air to fuel ratio, sufficient to 2). This decrease has been attributed to the authors by the flame decrease. Stationary [8] engines have been tested with much leaner mixes and stable operation (up to shut to 3). When compared to fossil fuels, PG generates fewer pollutants when utilised in ICEs. The flammable components of PG are mostly simple (easy to oxidise) molecules with a low combustion temperature, which limits NOx production.

3.2 Synthesis gas in combustion Engine

Mobile and stationary engines are separated into various applications. In fixed applications the motors are both internal and external, while moving motors are only combustion engines. ICE is the most important technological development and plays a vital part in the production of distributed power, especially when a variable output is required. In moving and moving machinery it requires a flexible application. In addition to other combustion technologies, it is assumed to have advantages, such low capital costs, reliability, good part-load performance, high operational efficiency and adaptability. ICE is quite reliable. In comparison to gas, the future of synthesis gas as a fuel in ICE is thought to be very promising and cost competitive.

3.3 Potential of Synthesis gas in Current Engine Technologies

The success of synthesis gas in older ICE engines must be explored in order to reintroduce the fuel in today's engine technology. The percentage composition of constituent gases in synthesis gas produced from biomass gasification is variable. In the literature, there are many different types of gas synthesis products. The synthesis gas standard generated by the gasification process is particularly attached to the gasification agent used in this way. If air is used as the gasifying medium, a coffee calorific value synthesis gas (producer gas) of H2, CO, CH4, CO2, and N2 in various q2 proportions as constituent gases is created. If a medium calorific value synthesis gas is used instead of air by steam or oxygen in different amounts, the H2, CO and CH4 are created as component gases. As a representative of the aforementioned class of synthesis gases within the existing engine technology, the applicability of synthesis gases should be explored for his or her combustion features. Various combustion compositions should be investigated.

IV. EXPERIMENTATION

The following chapter discusses experimental studies on the use of biomass-derived gas engines. Experiments on small power engines (SPE), converted from Diesel, tested at different CRs are described. The experimental work will take place.

4.1 Introduction

The weak information based on biomass motors in literature is taken into consideration in this experiment. However, with the author's perceptions different to those mentioned in the literature on high CR operations, a radical scientific research has started for the first time. The first study takes place at a motor with a nominal capacity of 24 kW. The CR 16 is a commercially available production diesel engine that will be converted to a spark-ignition (SI) engine for this project. Engine operations are found to be challenging in terms of data acquisition of engine cylinder pressure history due to severe electro-magnetic interference from the mechanical ignition, which severely hampered the

working of the computer, a neighbourhood of the information acquisition system in the early stages. This was later addressed via circuit changes.

4.2 Description of the Engine

Experiments were conducted on a petrol (SI) engine that was converted from a CR16's naturally aspirated, three-cylinder, direct injection diesel (RB 33 type). This helps to understand why this particular CR diesel was chosen. Working an interior combustion engine at the highest CR is preferable in order to achieve high overall efficiency, according to fundamental thermodynamics. However, efficiency increases above a certain CR are generally predicted to be limited due to the opposing effects of other factors such as heat loss and friction. However, in the case of a SI engine, the restrictions of CR are due to an additional factor called knock. The knock sensitivity identifies the best useful CR (BUCR) for a large number of fuels. However, it is experimentally shown for higher-octane fuels that the highest limit of CR is 16 over which efficiency falls [Caris et al, 1959].

4.3Engine Configuration Details

Table 1: Engine Configuration Details

Sl.No	Parameter	Specification
1	Make and Model	Kirloskar, RB-33 Coupled to a 25kVA Alternator
2	Engine Type	In-Line, 3 Cylinder, 4-Stroke, Naturally Aspirated
3	Rated Output – Diesel	28 kW @ 1500 rev/min
4	Net Output – Diesel	24 kW (21kWe) @ 1500 rev/min
5	Type of Cooling	Water Cooled with Radiator
6	Bore x Stroke	110 x 116 mm
7	Swept Volume	1.1 Litre
8	CR	17:1
9	Bumping Clearance	1.5 mm
10	Combustion Chamber	Flat Cylinder Head and Hemispherical Bowl-inPiston Type
11	Squish Area	70%
12	Ignition System – Gas	Battery Based Distributor Type with Ignition Advance/Retard Facility
13	Spark Plug Type & Location- Gas Mode	Cold, Offset from the Axis of Cylinder by 8mm
14	Intake Port	Directed Type
15	Valve Timing	Inlet Valve Opening – 26 ° BTC Inlet Valve Closing – 66 ° ABC Exhaust Valve Opening – 64 ° BBC Exhaust Valve Closing – 38 ° ATC
16	Firing Order	1-2-3
17	SFC, g/kWh – Diesel	280 - 290
18	Air-to-Fuel Ratio Diesel Mode at Peak Load	20 to 21:1 at 24 kW
19	Alternator Efficiency	87%

4.4 Experimental Procedure

The 75 kg/hr gas generator consisted of a well investigated, tested and industrial version of the gasifier. The system has been able to meet the industrial criteria for consistent gas quality for lengthy hours of continuous operation. A reactor, gas cooling and cleaning system, flare, and ducting to the gas engine were all part of the system. The reactor and refrigeration system are the same. However, instead of using chilled water for the scrubber in the gas cleaning system, a diesel wash was given.

Once the gas composition had settled, the engine was run at 1500 rev/minunder no-load condition for a few minutes. Further loading procedures at 1500+50rev/min were also carried out. Drops have been obtained utilising manually actuated valves to manage speed and air to fuel provisioning (without carburetor). CRs 10, 12, 14 and 16 were experimented. The CR values are calculated using the cylinders' geometrical measurements. The engine has been tested in various ignition time settings to determine the ideal ignition time, known as MBT (Minimum Advance for Brake Torque), at various CRs. With a set ignition period, the air and fuel were calibrated to maximise power. Measures began 10 to 15 minutes after the surgery had achieved a steady state. The in-cylinder pressure data was gathered on the computer for consecutive cycles with an angle resolution of one degree crank.

V. RESULTS AND DISCUSSIONS:

5.1 Pressure-Crank Angle (P-θ) Diagram for Redgram Producer Gas

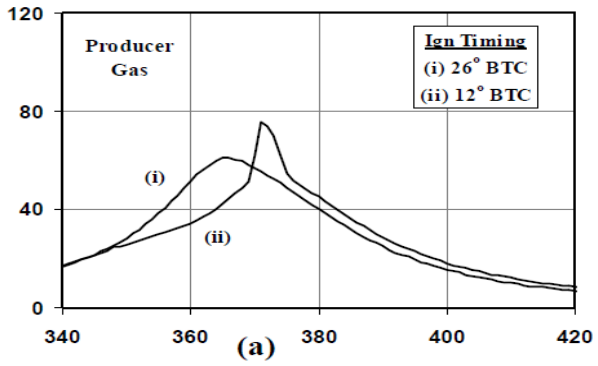

Figure1. Normal Combustion under Wide Open Throttle Condition

With Producer Gas at Different ITs at CR=16

5.2 Maximum Net Engine Output at Varying CR for Redgram Producer Gas

Table 2: Maximum Net Engine Output at Varying CR

CR	INGBTC	Φ	Net Elec. Power(KWe)	Net Brake Power BP (KW)	Mixture Energy Density (m3/Kg)	Efficiency Gas-to-Shaft (%)	Peak pressure (bar)
10	15	1.07	14.2	16.1	2.19	26.3	32.00
12	14	1.06	15.4	17.4	2.18	28.1	44.00
14	10	1.10	15.1	17.2	2.20	28.4	42.30
16	06	1.10	16.3	19.7	2.21	29.6	54.00

5.3 Various Graphs for Redgram Producer Gas

5.3.1 CR versus IT for Redgram Producer Gas

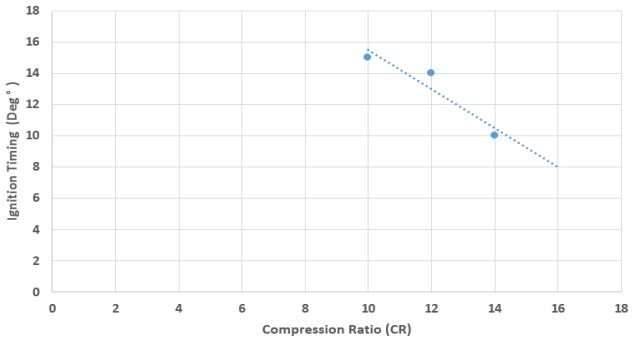

Figure 2. CR versus IT

5.3.2 CR versus Equivalence Ratio for Redgram Producer Gas

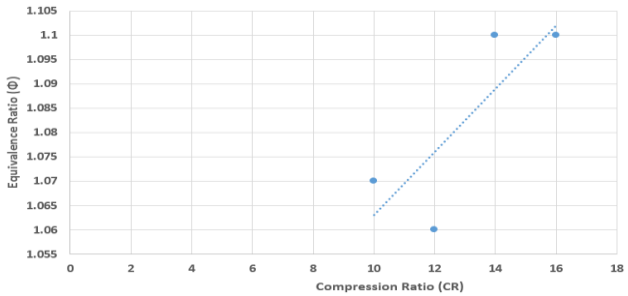

Figure 3. CR versus Equivalence Ratio (Φ)

5.3.3 CR versus Electrical Power for Redgram Producer Gas

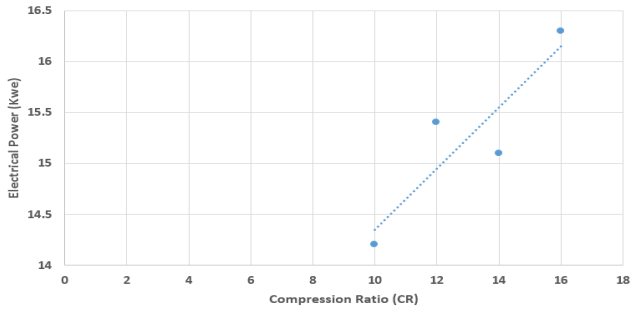

Figure 4. CR versus Electrical Power

5.3.4 CR versus Brake Power for Redgram Producer Gas

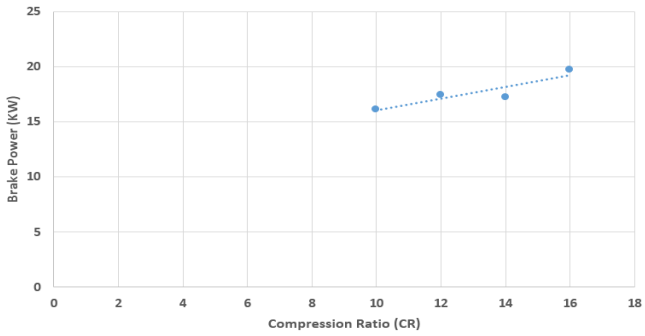

Figure 5. CR versus Brake Power

5.3.5 CR versus Mixture Energy Density for Redgram Producer Gas

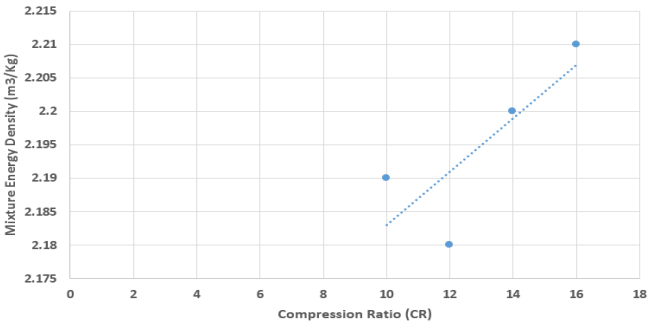

Figure 6. CR versus Mixture Energy Density

5.3.6 CR versus Efficiency Gas-to-Shaft for Redgram Producer Gas

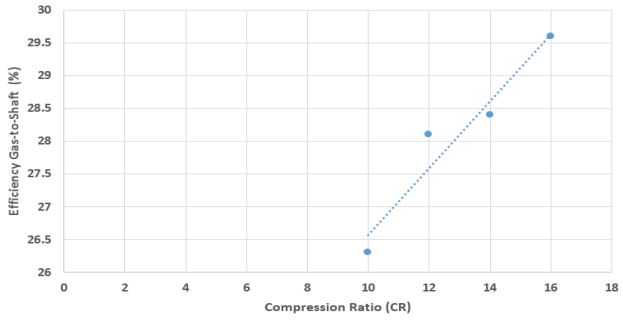

Figure 7. CR versus Efficiency Gas-to-Shaft

5.3.7 CR versus Peak Pressure Redgram Producer Gas

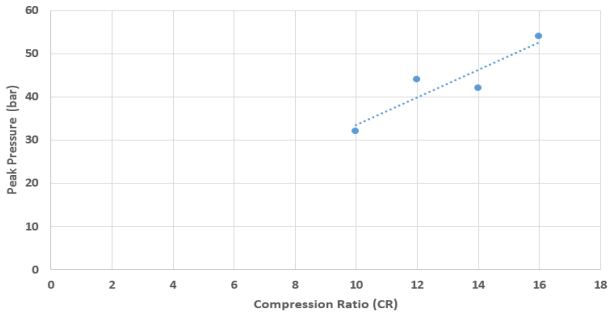

Figure 8. CR versus Peak Pressure

5.4 CR & Mechanical Efficiency for Redgram Producer Gas

Table 3 CR& Mechanical Efficiency

CR	Mechanical Efficiency From Morse Test
10	87
12	85
14	83
16	80

5.4.1 CR versus Mechanical Efficiency for Redgram Producer Gas

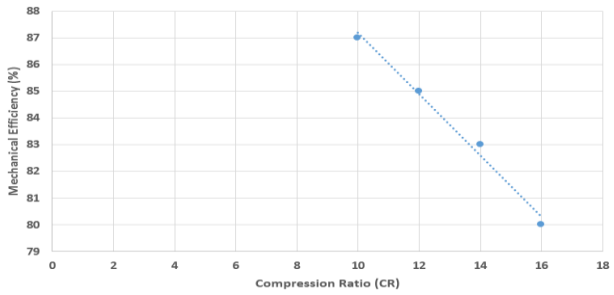

Figure 9. CR versus Mechanical Efficiency

5.5 Pressure-Crank Angle (P-θ) Diagram for Cotton Stalk Producer Gas.

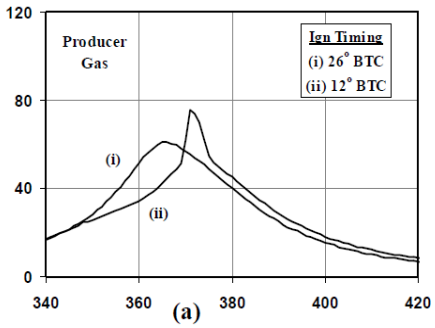

Figure 10. Normal Combustion under Wide Open Throttle Condition

With Producer Gas at Different ITs at CR=16

5.6 Maximum Net Engine Output at Varying CR for Cotton Stalk Producer Gas

Table 4: Maximum Net Engine Output at Varying CR

CR	ING BTC	Φ	Net Elec. Power (KWe)	Net Brake Power BP(KW)	Mixture Energy Density (MJ/Kg)	Efficiency Gas-to-Shaft (%)	Peak pressure (bar)
10	15	1.07	16.3	18.6	2.20	28.5	34.00
12	14	1.06	17.2	19.6	2.10	30.3	46.00
14	10	1.10	17.4	19.8	2.20	30.0	44.30
16	06	1.10	18.5	21.0	2.20	31.7	56.00

5.7 Various Graphs for Cotton Stalk Producer Gas

5.7.1 CR versus IT for Cotton Stalk Producer Gas

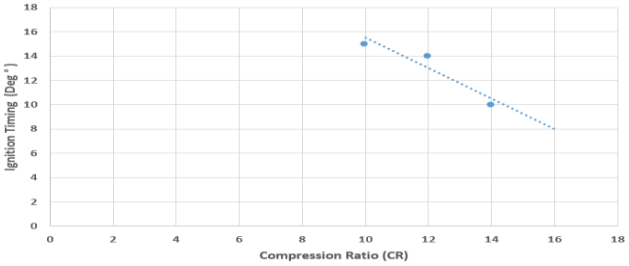

Figure 11. CR versus IT

5.7.2 CR versus Equivalence Ratio for Cotton Stalk Producer Gas

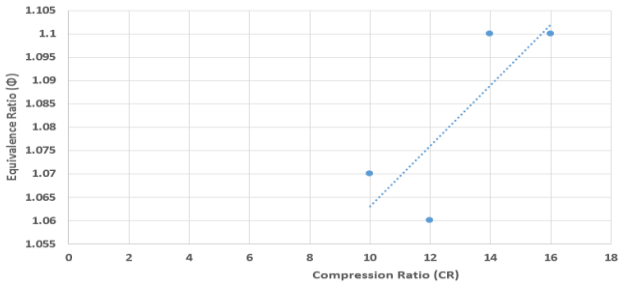

Figure 12. CR versus Equivalence Ratio (Φ)

5.7.3 CR versus Electrical Power for Cotton Stalk Producer Gas

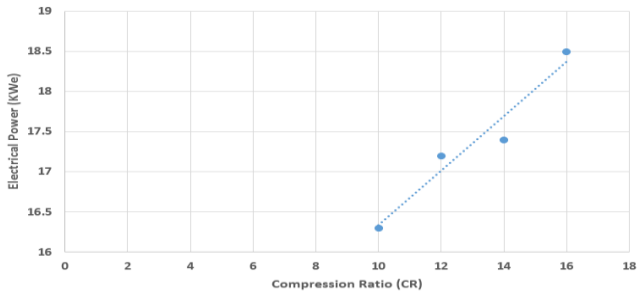

Figure 13. CR versus Electrical Power

5.7.4 CR versus Brake Power for Cotton Stalk Producer Gas

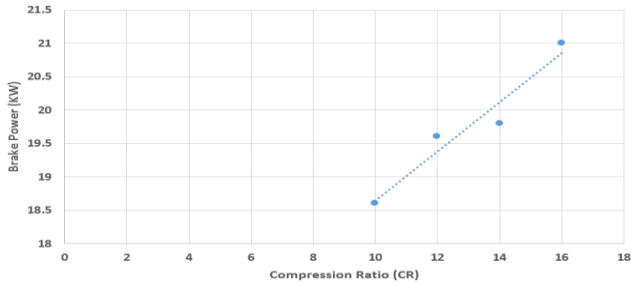

Figure 14. CR versus Brake Power

5.7.5 CR versus Mixture Energy Density for Cotton Stalk Producer Gas

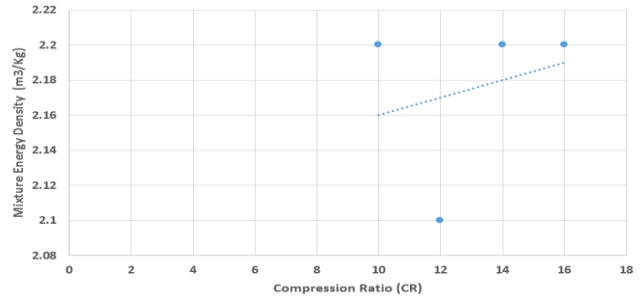

Figure 15. CR versus Mixture Energy Density

5.7.6 CR versus Efficiency Gas-to-Shaft for Cotton Stalk Producer Gas

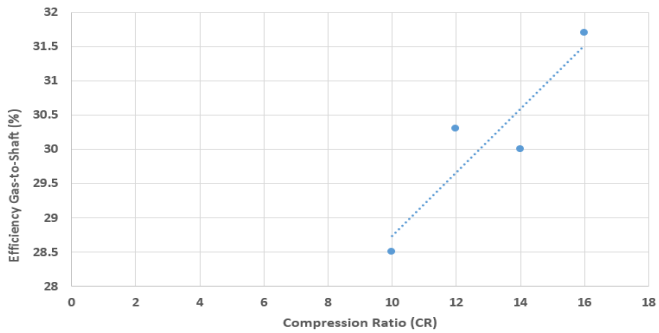

Figure 16. CR versus Efficiency Gas-to-Shaft

5.7.7 CR versus Peak Pressure Cotton Stalk Producer Gas

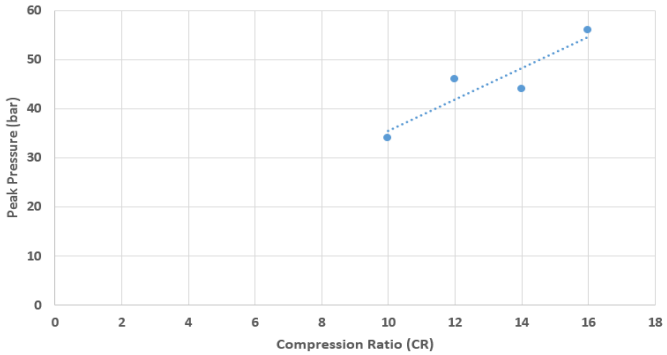

Fig. 17: CR versus Peak Pressure

5.8 CR& Mechanical Efficiency for Cotton Stalk Producer Gas

Table 5 CR& Mechanical Efficiency for Cotton Stalk Producer Gas

CR	Mechanical Efficiency From Morse Test
10	89
12	87
14	85
16	82

5.8.1 CR versus Mechanical Efficiency for Cotton Stalk Producer Gas

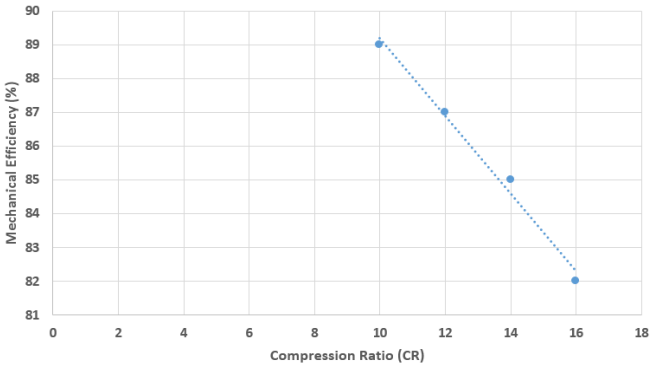

Figure 18. CR versus Mechanical Efficiency

VI. CONCLUSIONS

The engine's performance at greater CR is smooth, and up to 16 CR production gas engines have been shown to be practical. The p-θ curve reveals that the pressure increase is steady and no oscillations are present. A shorter combustion time using producer gas fuel has been reported, which requires delayed IT in order to accomplish MBT. The experiments have been carried out for different fuels namely red gram and cotton stalk biomasses. It has been observed from experiments that power output and efficiency are relatively high for cotton stalk biomass compared to red gram biomass.

The specific fuel consumption (biomass) is the crucial information for biomass gasifiers combined with gas engines. The specific biomass is produced at approximately 1.15 –1.25 kWh of electricity, which is equivalent to a general efficiency (electric biomass) of 21, and 19% respectively at 16 and 10 CR.

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Prediction on Change in Price of Bitcoins Using Machine Learning

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Abstract— Cryptocurrencies like Bitcoin have fascinated technologists and investors alike. Most of the jurisdictions haven't regulated cryptocurrencies. Bitcoin is currently the leading cryptocurrency globally. Cryptocurrency allows users to securely and anonymously use the net to perform digital currency transfers and storage. In recent years, the Bitcoin network has attracted investors, businesses, and corporations while facilitating services and products deals. Moreover, Bitcoin has made itself the dominant source of decentralized cryptocurrency. In this analysis we will classify bitcoin. We use different methods to observe its aspects of behaviour towards: asset classes like derivatives, currencies , technology based products , speculative financial bubbles , possible technology-based products like Ether and also the security SPY. We observed that the behaviour of bitcoin shows more resemblance to technology based product instead of currency or a security. While considerable research has been done on Bitcoin network analysis very limited research has been done on the prediction of the cost of Bitcoin.. The aim of this study is to predict the worth of Bitcoin and changes.

Keywords— Cryptocurrency, Bitcoin, Prediction, Technology diffusion, Technology entrepreneurship, Finance and Banking

I. INTRODUCTION

The biggest thing that hit the worldwide market since the invention of currency is that the concept of "Bitcoin". Bitcoin is an information technology breakthrough that facilitates both a secure, decentralized payment system and a tool for the storage, verification and auditing of data, including digital representations important . A bitcoin is additionally the intangible unit of account that facilitates the decentralized electronic network of Bitcoin users. Bitcoin isn't an organization or a corporation product. Contrary to several news reports, it's not anonymous and wasn't built for bad actors, though bad actors have, at times, brought Bitcoin into the headlines. it's a platform that enables two individuals to transact money without involving a third-party and without mediation costs involved in commerce through the web . There arose the necessity for an innovative electronic payment system supported cryptographic proof rather than trust. Bitcoin may be a decentralized peer to look (P2P) network-based virtual currency note that's not issued by a government or any organization .Bitcoin relies on cryptographic protocol and a distributed network of users, allowing users to mint, store and transact. it absolutely was invented by a bunch of programmer or an unknown programmer under the name Satoshi Nakamoto and released as open source software in 2009. Since then, Bitcoin has emerged because the most trusted and widely used cryptocurrency . in line with the research produced by Cambridge University in 2017, there are 2.8 to 5.8 million unique Bitcoin users . Bitcoin is currently accepted as a payment method among many legitimate retailers. However, this also attracts criminals to use this unique decentralized P2P network-based virtual currency, since there's no centralized authority to observe suspicious activity, allowing user to transfer funds anonymously.

Benefits of Bitcoin:

- Control Against Fraud
- Global Reach
- Cost Efficiency
- Tips and Donations
- Crowdfunding
- Micropayments
- Multi-Signature Accounts
- Trust and Integrity
- Resilience and Decentralization
- Automated Solutions

II. PROBLEMS FACED BY BITCOIN USERS [FERDIANSYAH,2019]

- Danger of Attack :

On the surface, the decentralised nature of the network protects it. Decentralised systems can better protect themselves against attack, and route around damage. Compare this to problems when banking systems go down. Last year, RBS customers suffered when the bank's systems failed. But there are nevertheless theoretical attacks on crypto-currency networks like Bitcoin, and lots of of them are proven practically. One example is that the 51% attack.

Bitcoin measures the amount of computing activity on the network in terms of the hash rate. Should one miner or pool of miners gain control of 51% of the hash rate, then they might theoretically be able to solve their own block of transactions. The 51% attack also ends up in a fork, which is where there are two conflicting blocks vying for addition to the blockchain. Because the bulk of mining power on the network would support the attacker's block, it'd be sent to the blockchain. The attacker's block could include fraudulent transactions, designed for financial benefit. for

instance, if the attacker sends bitcoins to a recipient in exchange for a product or service, it could then record that it had sent the identical bitcoins to a different Bitcoin address that it controls, in its own block. Bitcoin transactions are irreversible, so this lets the attacker spend the bitcoin twice, in what's referred to as a double-spending attack.

- Dust transactions:

These attacks all make it possible to control the network for private gain, but there are other categories, too. Denial of service attacks is accustomed compromise the network. There are several possible attacks. One involves 'dust' transactions – very small transactions that send hardly any bitcoins, but which take up space within the blockchain. The minimum fraction of a bitcoin is one Satoshi, which is 0.00000001 bitcoins. it had been previously possible to send one Satoshi over the network, which is akin to $0.00000112 at the time of writing. it had been therefore possible to send large numbers of those transactions, which is able to replenish blocks within the blockchain. Because each block increases the length of the blockchain, it can find yourself bloating the chain, which is already becoming increasingly unwieldy. In June 2013, the blockchain reached 8GB in size.7 The core development team's answer to the present was a patch that limited the scale of transactions within the network. due to a brand new version of the client, a minimum of 5,430 Satoshis can now be sent. At current values, that's still around six-tenths of a cent in US Dollar terms, but it still makes it far harder to mount a successful dust spam attack on the blockchain.

- Code-based attacks:

The other potential attack lies within the client's code itself. per core developers that spoke with him via online forums, Nakamoto spent a minimum of a year thinking conceptually about the network before coding it. The ASCII text file for the network, Bitcoin, is thought because the 'Satoshi client'. it's still in use today, and is maintained by a set of open source developers via Github. "The developers are adding features to the Satoshi client, and a bug may slip that would be accustomed attack the network," says Sergio Lerner, a cryptography expert who searches out vulnerabilities in Bitcoin. "Many people read the ASCII text file before a release, but security vulnerabilities are sometimes harsh to identify." we've seen a number of these attacks surfacing already. An attack on the voluntary Bitcoin nodes on the network – those which relay transaction information round the network but which don't necessarily mine coins – surfaced in late June 2013. The core development team had to issue a patch to unravel the matter, and therefore the attack ceased.9 "Bitcoin may be a mechanism for money, rather the services that are layered on top of cash to create it useful. As these begin to emerge, the Bitcoin community will have even more to influence" during this case, the attack exploited an incomplete feature within the ASCII text file. The software is stuffed with these stubs, which are vestiges of Satoshi's original ideas and plans for Bitcoin. These even include an Ebay-like Bitcoin market that was never implemented. Garzik says that such semi-coded features are being 'walled off ' within the ASCII text file. Nevertheless, they evidently still expand the client's attack extent. There are some steps that may be taken to form the code – and so the network – safer, argues Lerner. "They should pay security researchers to review each new patch, or a minimum of clearly document which developers with knowledge in computer security have reviewed each patch." Bitcoin has already shown many promise. However, the core developers face challenges because the size of the network increases. The concept is just just beginning, too. Bitcoin could be a mechanism for money, rather the services that are layered on top of cash to create it useful. These include credit structures, the issuing of bonds, futures and options trading, and structured financial instruments. As these begin to emerge (and there are already proposals for them), the Bitcoin community will have even more to contend with.

III. DIFFERENT METHODS [FERDIANSYAH,2019] [McNALLY , 2018]

The most important tool required for the prediction of bitcoins is that the graphs of previous years representing the price fluctuations of the bitcoin. Bitcoin securities market Prediction Tools supported previous research have increased from 2014 until 2019 many tools produces from authors that proposed using machine learning algorithm.

- From Alex Greaves et al. 2015 , their research propose prediction strategy utilizing exchange chart to foresee the cost of bitcoin, their collected information from CS224 Website, and utilizing feature Extraction and utilizing SVM algorithm and Linear Regression to give the outcomes.

Classification Model Accuracy

Logistic Regression 54.3%

Baseline 53.4%

Neural Network 55.1%.

SVM 53.7%

Table 1 Classification results

Based on different results provided by the author on the primary regression model, the baseline shows good result behind. Linear or SVM, and for classifications the accuracy reached by the Neural Network is 55.1% by percentage.

- Hiusu jung et al. 2017, provided an empirical study and a method to predict the price of bitcoin using Bayesian neural network, and therefore the results of BNN provide an accurate prediction.

Based on the results, we can say that Bayesain NN shows smart results and are highly applied for the Bitcoin prediction whereas time series analysis and support vector

regression do not show smart results in coaching as well as testing phases.

- Arief Radityo et al. 2017, the author provided a prediction method for the bitcoin exchange rate by combinig Artificial neural network and technical analysis.

From the results we can say that GABPNN offers most accuracy with an average mean absolute percentage error (MAPE) of 1.883%. GANN has the worst accuracy with average MAPE of 4.461% and GABPNN has the longest training time.

- Sean Mcnally in 2018 came up with a method for prediction of bitcoin in with he used Bayesian optimised recurrent neural network (RNN) and long short term memory (LSTM).LSTM gains the highest classification accuracy above 52% and a Root Mean Square Error (RSME) of 8%.

Model Length Precision Accuracy RMSE

RNN 20 39.08% 50.25% 5.45%

LSTM 100 35.50% 52.78% 6.78%

ARIMA 170 100% 50.05% 53.74%

LSTM achieves the very best classification accuracy above 52% and a RSME of 8%.

IV. IMPLEMENTATION AND RESULT

Comparing the numbers provided by these different methods LTSM proves to be the one with the highest accuracy above 52% and a RSME of 8%. So we have prepared our own LSTM model and here are the results of the prepared model:

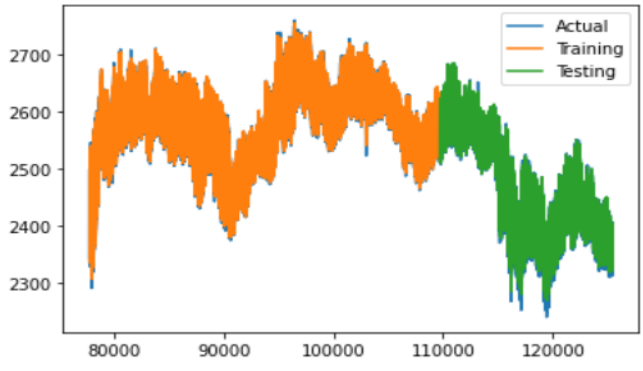
Data Set:

https://drive.google.com/file/d/1Xoq1D3Q64xjHe0NyEVN9QILrjiv_vb5z/view?usp=sharing

Implementation of the Code :

https://colab.research.google.com/drive/1QSrbL5mj-laQoRhFcb3vTGTH4zhtcLWi?usp=sharing

This particular model contains 4 LSTM units and 1 dense unit. After running the model these were the results obtained:



The ratio of the figures from dataset and the figures predicted is 67% and 33% respectively.

```
regression_results(trainY[0], trainPredict[:, 0])
regression_results(testY[0], testPredict[:, 0])

explained_variance:  0.9964
mean_squared_log_error:  0.0
r2:  0.9962
MAE:  3.1283
MSE:  22.5627
RMSE:  4.75
explained_variance:  0.9969
mean_squared_log_error:  0.0
r2:  0.9965
MAE:  3.9658
MSE:  34.6977
RMSE:  5.8905
```

These are the r2 values of the training and testing of our model.

V. CONCLUSION

Deep learning models like the RNN and LSTM are evidently effective for Bitcoin prediction with the LSTM more capable for recognising longer-term dependencies. However, a high variance task of this nature makes it difficult to transpire this into impressive validation results. As a result it remains a difficult task. there's a fine line between overfitting a model and preventing it from learning sufficiently. On Hiusu jang BNN can give good prediction but not enough results, future directions is try and adopting extended machine learning methods. On Arief Radtiyo et al, their suggest about combine with fuzzy or SVM algorithm and optimize the dataset, or optimize the algoritym because worst accuracy and longest training time. From the suggestion above, we will make conclusion on the long run direction are going to be optimize the dataset shrouded the noise, use some feature, and make shorter training time, combine with some technique and algorithm (Hybrid methods) to supply new best result.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Voice-Based Email System

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Abstract— Many industries have been substantially transformed since the Internet's birth. The internet is an essential luxury for everyday life. Everyone uses the internet to find facts and information. Communication is one of the most important sectors that the Internet has altered with the growth of several communication tools, such as the internet. Communication has become quite simple in today's society. When we think of Internet communication, the first thing that springs to mind is E- mail. There are a variety of situations in which the user is unable to type or text. Using voice assistants is one of the most efficient solutions to these types of challenges. One of the most efficient solutions to this type of problem is using voice assistants. So, our voice-based e-mail application is used to send voice-based email message.

Keywords— Communication, E-Mail, Internet, and Voice Assistant

I. INTRODUCTION

We have seen how the emergence of the Internet has transformed several areas. People's lives have been so simplified as a result of the Internet, and they now have quick access to whatever information they choose. It is quite important in today's communication environment [1]. The internet is the foundation of today's world. No task can be completed without the usage of the internet.

Communication is one of the primary areas in which the Internet has had a significant impact. When we think of Internet communication, the first thing that springs to mind is E-mail. E-mail, or electronic mail, is the most vital component of daily living. It is the most trustworthy method of Internet connection for delivering and receiving crucial information.

However, some people in today's society are unaware of how to utilize the internet. As a result, they have a tough time adjusting to life in the digital age. Screen readers, ASR (Automated Speech Recognition), Speech to Text, Text to Speech, HCI and other technologies are now accessible throughout the globe [2]. However, these are inefficient for them. We need to provide them with internet access so they can use it. As a result, we developed our project Voice-based email system for the people, which would greatly assist them in sending emails.

II. ORIGIN OF THE PROBLEM

According to a new report, elderly people are increasingly becoming ostracized as a result of digital illiteracy. The Agewell Foundation claims. According to the Agewell Foundation Survey, roughly 79.4% of respondents are digitally and computer illiterate. According to the poll, 67.9 percent of digitally illiterate respondents claimed that a lack of computer skills and digital illiteracy were negatively influencing their lives in old age [3]. We went to a few groups to learn about the people's difficulties. Taking all of the concerns into account, the biggest issue that people encounter is a lack of use of mobile devices such as Phones, PC's, and so on. People are taking an inordinate amount of time to compose an email. In addition, based on the results of the aforementioned poll, we decided to launch a project that would benefit those who wish to make their work easier. Our project is an android-based application that uses IVR (Interactive voice response) to connect with humans via speech and DTMF (Dual-tone multi-frequency) tones input [4]. This software saves time by allowing users to send emails using voice commands.

III. MODULE DESCRIPTION

A. Registration

Any user who wishes to use this system must first register in order to receive his or her own username and password. The registration module will acquire all of the information about the user provided to the system via voice commands.

B. Login

This is the system's second module. After completing the registration process, the user will be able to access the system. The login module will prompt the user for a username and password. In this case, the procedure involves a user's speech to text dialogue. The user will be prompted to check whether or not the information entered is correct. If the information is valid, the user is approved and will be sent to the main page.

C. App Page

When the user successfully logs in, he or she is brought to this page. The user can now do the operations that he or she want from this page. There are several options available: Inbox, compose, Sent, Sign-out.

D. Inbox

Inbox is the module where if the user wants to see what ever mails, he has got. The mails are displayed in the list view with the username, subject and body of the message. The date in which the mail has arrived will also be displayed.

E. Compose

Compose is the module where if the user wants to send an email, he can use it. The user needs to speak out "To" address, "Subject" and "Body of the message". Then he needs to click on compose button so that the other person can receive the mail.

F. Sent

In the sent module the user can view the list of emails in which he has sent to the various other users. He also can view the email along with the date on which he has sent.

IV. RELATED WORK

Voice-based Email System enables individuals to access email by voice [5]. This system is based on the voice mail architecture and allows for quick and easy access to e-mail. This approach will assist in overcoming some of the issues that individuals previously had while accessing emails. People must have easy access to email service, which is the most widely used method of communication in today's world [6]. This approach helps to eliminate the difficulties encountered when accessing emails, such as memorizing and using keyboard shortcuts and mouse clicks. We have implemented a new security feature, voice verification, in addition to standard login and password protection. When a user hits a button, IVR

[7] specifies the function that the button does. Another advantage of the method is that the user must provide verbal inputs. They are not required to memorize keyboard shortcuts. As we can see in [8], have built a system that allows visually impaired persons to conveniently utilize email services. This technology aids in removing some of the barriers that blind individuals previously experienced while accessing emails. The system will issue voice commands to the user to accomplish a certain task, and the user will react [9]. The fundamental advantage of this systems is that it does not need the use of a keyboard; instead, the user must answer solely by speech and mouse clicks. The system in [10] describes email services based on audio communication via which it may read and send messages on their own using their Gmail accounts. Users must utilize certain keywords to do specific operations, such as Read, Send, and Compose Mail, among others. Previously, blind persons did not use the technology to send email. The range of email types, together with the ability setting, enables their use in various everyday situations [11]. These emails, however, are not useful in audio-based emails, which are solely favored by blind people. It is quite unusual in this system. As a result, there is a lower likelihood that this audio-based email will be available to blind persons. As a result, there is a lesser chance that this audio-based email will be accessible to blind people. This mostly aids people who are physically handicapped, such as the disabled and the blind.

V. PROPOSED METHOD

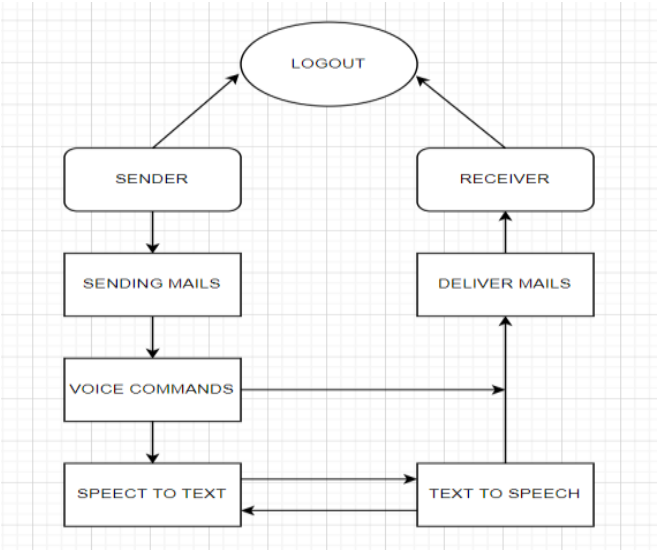

Figure 1. Model Architecture

A. Retrofit Instance

Retrofit is a type-safe REST client for Android and Java that attempts to simplify the consumption of restful web services [12]. Retrofit serializes the JSON response automatically using a POJO (Plain Old Java Object) that must be specified in advance for the JSON Structure. To connect to the server, use BASE URL. Retrofit gives networking features to your Android application [13]. In our model, to get back the data, we use those networking features and also used to connect HTTP API service.

B. Speech Recognizer

This class allows you to use the speech recognition service. Access to the speech recognizer is provided via this service. It is expected that the implementation of this API will send audio to distant servers for speech recognition [14]. When recognition-related events occur, the Recognition Listener receives alerts from the Speech Recognizer. The following are some of the functions accessible in the Recognition Listener class:

- onBeginningOfSpeech (): The user has begun speaking.
- onEndOfSpeech (): Called when the user finishes speaking.
- onError (int error): An error in the network or recognition occurred.
- onRmsChanged (float rmsdB): The audio stream's volume has change

C. Speech to Text

At runtime, the system captures voice through a microphone and analyses the sampled audio to recognize the said text. Our voice-to-text technology collects and transforms speech directly [15]. It can enhance bigger

systems by providing users with a new option for data entry. Speech-to-text converts

spoken-word audio into brief "samples" that are associated with basic phonemes or units of pronunciation. The data are then sorted by complicated algorithms in an attempt to guess the word or phrase that was stated.

D. IVR (Interactive Voice Response)

IVR (interactive voice response) is a technique that allows a computer to connect with humans by using speech and DTMF tones entered into a keypad. To further advise users on how to continue, IVR systems can answer with pre-recorded or dynamically created voice. Because IVR systems are more sophisticated than many predictive dialer systems, they are sized to handle high call volumes and are also utilized for outbound dialing.

VI. EXPERIMENTAL RESULTS

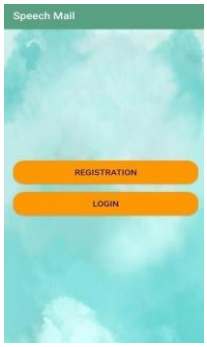

Figure 2. Welcome

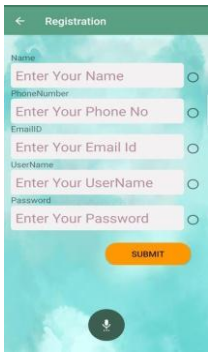

Figure 3. Registration

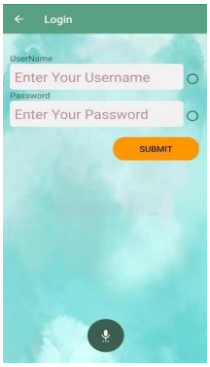

Figure 4. Login

Figure 5. Home

Figure 6. Compose

Figure 7. Inbox

Figure 8. Sent

VII. CONCLUSION

We developed an Android-based application without the usage of any complicated algorithms. In comparison to the other system, it is simple to use and comprehend. Taking into mind all of these implementation strategies, this system becomes user friendly, interactive, and secure. Because the use of smart phones is becoming more popular, our application will be more valuable to consumers today. There are several languages in the globe. We're implementing this system in English because the majority of people are already familiar with it. IVR is the innovative technology that we deployed here. To further advise users on how to continue, IVR systems can answer with pre-recorded or dynamically created voice. Many predictive dialer solutions are less intelligent than IVR systems. The fundamental advantage of this system is that it does not need the use of a keyboard; instead, the user must answer solely by speech. In our model, to get back the data, we use those networking features and also used to connect HTTP API service.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

15th-16th July, 2021 – Virtual Conference

Fragility Analysis of Building Structures: A Review

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Abstract— Building structure is prone to damage towards a sudden seismic event. Functionality of different type of building varies in post-earthquake scenario. Extent of damage of the building structure depends on the magnitude of the seismic event or the epicenter of the earthquake. Fragility analysis of building allow us to predict the probable damage that may occur, which helps in lessening the damage of property or prevent total collapse, therefore saving the lives of occupants residing in the structure. Several possible parameters include the ground motion intensity, peak ground acceleration, inter-story drift, etc., for the fragility curves to be derived. These fragility curves will help in estimating the fragility of the building structure. The method of analysis adopted in most of the research are pushover analysis, dynamic time history analysis, incremental dynamic analysis, etc. This study focuses on a brief review of fragility analysis of various types of building structure such as residential, industrial pre-cast, high-rise buildings, buildings residing in hilly areas, etc. This study will help in providing a better knowledge on seismic risk assessment of building structure towards a sudden seismic event. Area of vulnerability within the structure during an earthquake can also be estimated through this review study.

Keywords— Buildings, deformation, ground shaking, fragility analysis

I. INTRODUCTION

Damages caused by earthquake is catastrophic. The sudden seismic event eventually leads to disturbance to the mankind and its surroundings. The damage of an earthquake begins with a strong shaking of the earth. Harmful effects of a large earthquake can be felt hundreds of kilometers away. Shaking of ground or ground movement are the primary cause of earthquake damage to man-made structures. Many factors will affect the strength of seismic shaking, which also includes the earthquake intensity or magnitude, the proximity of the location to damage, local geological conditions, and the type of soil. Earthquake vibrations can cause the earth to shift and tear its surface. Destroying surfaces can cause other hazards, damage roads and buildings. Earthquakes of different strengths affect buildings to different degrees. Natural hazard can never be avoided but damages caused by natural hazards can be prevented to a certain extent if precautionary measures are taken. Similarly, if the probable damages that may occur against a certain magnitude of earthquake can be predicted, thousands of lives can be saved by avoiding the collapse of structure.

For the structure to enable to resist the shocks and vibration due to earthquake, the property of ductility plays primary role in determining the performance of the building. The earthquake resistant design helps to predict the probable damage area and imparts good detailing at these parts to ensure the structure's ductility. Therefore, earthquake resistant buildings that are more economical than earthquake proof building, must be provided to ensure the safety of people and their contents so as to avoid disasters.

An earthquake design philosophy is discussed further. With slight and frequent shocks, the main elements of the building which carry the vertical and horizontal forces must not be damaged. However, components that do not hold the load can cause irreparable damage. Moderate, but occasional shaking can damage major elements in an irreparable way, as well as damage other parts of the building that may even need to be replaced after an earthquake. Strong but infrequent shocks can cause serious (even irreparable) damage to major elements, but the building must not collapse. This way, after slight shocks, the building is fully functional in a short time and repair costs are low. In case of moderate shaking, after completion of repair and reinforcement of the main damaged elements, the building will be put into operation. But, after a strong earthquake, the building may become inoperable for further use, but will be positioned so that people can be evacuated, and property can be restored [11].

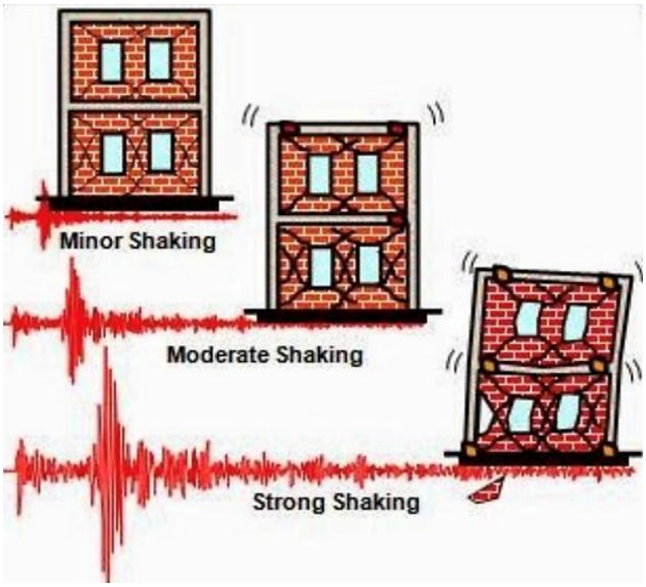

Fig 1: Performance objectives under different intensities of earthquake shaking (Murty 2005)

II. FRAGILITY ANALYSIS

Fragility analysis is an analysis that is used to estimate losses of seismic in built-up areas. It shows the probability of exceeding a damage limit state for a given structure type subjected to a seismic excitation [9]. In seismic fragility, soil pile interaction might also have a negative or positive effect for various structural components and various damage states [13]. A fragility function obtained for non-compliant and compliant Low-rise, (SMRF) Special moment resisting frames indicate that they have alike seismic properties under mild to moderate damage conditions, but non-compliant SMRFs outweigh the severe and critical damage conditions prior to compliance SMRF [1]. For assessing seismic losses and managing city risk, analysis of the seismic fragility of structures is the basis. This analysis type is useful for the response to understand a structure to earthquakes and determining damage of structure correlating to a particular intensity level of earthquake. Therefore, deciders can consider analysis of fragility as an important reference for mitigating the impact of an earthquake.

III. METHODS FOR ANALYSIS

Non-linear Static Pushover Analysis.

Pushover analysis, also known as nonlinear static analysis, is a valuable method for evaluating the inelastic strength and deformation requirements of structures as well as exposing structural design flaws. Its key benefit is that it makes it easier for structural engineers to identify important seismic response values and use engineering considerations to precisely adjust the power, capacity, and deformation quantities that govern seismic response near damage. It should be noted that this analysis is approximate and does not account for complex properties such as hysteresis, higher participation mode, and so on. It's well-known for producing good results in normal structures (without torsional irregularity).

Pushover analysis offers a tool that is reliable for classifying destruction status. Also, it does not only have the ability to identify which pile stacks of pile supported wharf structures have percentage of vulnerability to fail or get damaged during a seismic event or operation, but it is also effective in obtaining seismic bound demands [13].

Dynamic Time History Analysis

Dynamic time history analysis provides a linear or non-linear assessment of complex structural behavior under load, which can vary based on a specific time feature. The time history of the input force or acceleration is used in time history analysis, which is then combined to produce a response. The complete time history shows how structures react over time, both during and after loads are applied. In time history analysis, the systemic response is measured at many points in time. It can be also said that the input of structural response time history is the output.

Incremental Dynamic Analysis

Incremental dynamic analysis (IDA) is a computer-assisted earthquake analysis technique for determining the behavior of structures under the loads of seismic. Its aim is to develop the results of a seismic hazard study in order to determine a structure's seismic risk. This can be compared to static displacement analysis in terms of dynamics. This method is very useful which includes running a sequence of nonlinear dynamic analyses on a set of scaled ground motion records, the sensitivity of which should preferably cover the whole range of elasticity to complete dynamic instability.

The results of IDA-based analysis of fragility suggest that by expanding the Engineering Demand Parameter (EDP) limit in a particular direction by a factor of 12 + 2, which is the ratio of Peak ground Acceleration (PGA)s of input of records of seismic in the principal directions of two structure, one can conduct fragility analysis using combined EDPs and combined IMs (Intensity Measures) while getting exceedingly probabilities approximating to results from analysis [5].

Fragility Curves

The curves of fragility of buildings are function of lognormal that elaborates the possibility of exceeding or reaching, non-structural and structural states of the damage with the given median estimates of spectral response. Fig 2 shows variations in probabilities of sate of damage particularly for main three stage of response of spectrum corresponding to mild, medium, and powerful seismic ground motion, as well as examples of curves of fragility for the four states of damage used in the FEMA/NIBS technique [4].

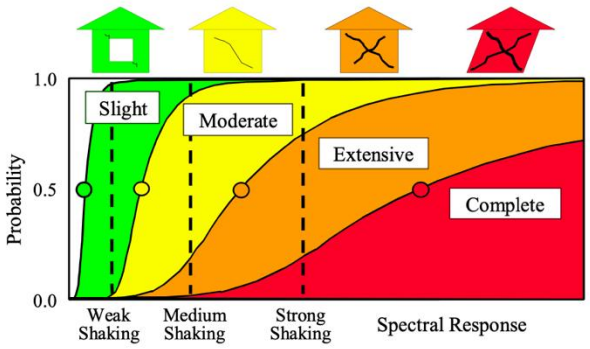

Fig.2: Example for the Fragility Curves for "Slight, Moderate, Extensive and Complete Damage" (Engineering n.d.)

The fragility curves of a reinforced concrete moment frame structure that has three story and a HAZUS low-code structure's level of design of mid-rise RC moment frame were found to be in reasonable agreement. Also, the curves are found useful for calculating the existing structure's vulnerability in the United States [7]. From the risk index of seismic, the curves of fragility can represent the likelihood of exceeding specified states of limit when given to a varying intensity of seismic event, and peak inter-story drift

ratios showed a similar pattern [16]. It was discovered that the fragility curves derived by explicitly addressing the ground motion intensity uncertainty were flatter than those generated without the uncertainty [17]. The contrast between the required curves of fragility without & with soil pile interaction becomes more pronounced from slight to immense damage states, revealing the modelers that the effect of soil pile interaction should be considered when evaluating the fragility of seismic of the pile supported wharf structures under extended hazard status [13]. The curves of fragility reveal that the angle of slope has a significant impact on efficiency of seismic. At the same output level, the probability exceedance increases as the slope angle increases [14].

IV. CASE STUDY

With the MR dampers application based on the approach of Direct Performance-Based Design (DPDB), the fragilities of seismic are significantly lower than those of the structures that are not controlled under two different levels of danger using 41 earthquakes and structures having low level performance targets have much lower vulnerabilities of seismic than those with greater performance, within that of the similar seismic hazard category [3]. In the case of precast building classes of industrial, in which a configuration of structure with type 2 and low-code architecture, if infills of masonry were used in buildings with the acceleration median peak ground triggering collapse was reduced by 35% [2]. Drift-based assessment results are cautious, whereas material harm index results are risky. The results obtained for seismic risk assessments of structures with steel reinforced concrete frame based on the damage index of component, on the other hand, it is said to be cost-efficient, realistic and reliable overall [16]. In the special moment resisting frame, due to the involvement of the confinement ties within the joint area for tensile strength, in addition to the structural strength of the concrete, which slows the breakdown of joints under side loads and thereby increases the deformability of the structure [1]. Probabilities of exceedance obtained from analysis of fragility indicates that buildings of tall height would have lower probabilities of exceedance when viscous dampers are installed in the structure's lower part and BRBs are mounted in the structure's upper part [5]. The models of the fragility that are proposed can be inculcated for the vulnerability to assess and, as a result, the risk of RC frame buildings that are non-ductile in Southern Europe are prone to liquefaction and ground shaking. Also, it was discovered that the extreme soil's non-linear behavior caused by liquefaction of the soil causes the motion of the seismic event at the surface of the ground to be attenuated not in terms of velocity but in acceleration [8]. Columns that are flexible, seem to oscillate as the slope angle increases, the short column resists almost all story shear. As the slope angle tends to increase, a hinge mechanism forms near the shorter column zone and is damaged sooner [12].

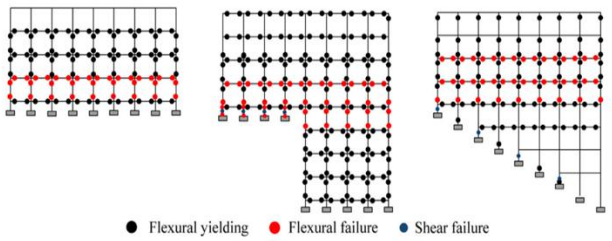

Fig 3: Hinge patterns at collapse for the four-story buildings (Surana et al 2018): (a) Flat land, (b) Split-foundation building, and (c) Step-back building

In fig 3, the hinge pattern at collapse in the hillside buildings of Step-back (SB) and Split-foundation (SF) suggest that the floor just above the uppermost level of foundation is the most vulnerable position, which is consistent with what was noticed after the Sikkim earthquake happened in 2011, in the case of an SF building [15]. The building built for load of gravity has a very low lateral load potential and fails at spectral accelerations which is very low, according to research. The building of SMRF with columns of short height has a higher resistance of seismic, but the columns that are short draw all of the story shear and fail under shear, while it remains well within the elastic limit for the other members.

Also, for the earthquakes that is mild with an effective PGA of 0.18 g, the probability of collapse for a building built for load of gravity is 99 percent [14]. With the uneven heights of ground column, the overall inter-story drift of buildings on hill or slope with ground column heights that are not even is vulnerable at the story that is on the ground. As the slope angle increases, the probability of exceedance at same performance level increases [6].

V. DISCUSSION

The discussion based on the review study are as follows:

In seismic fragility, soil pile interaction might have a negative or positive effect for various structural components and various damage states.

The overall height of the building has a substantial impact on its susceptibility to liquefaction of soil and shaking of the ground.

In the design of buildings, components of non-structure should not be ignored, nor when evaluating their seismic efficiency or risk.

From the collapse probability of buildings inculcating various configuration of structure in hillside, it was shown that the existing code requirements are appropriate in case of mid-rise and low-rise buildings in zone of seismic IV (moderate magnitude), but they were found to be insufficient for tall buildings for the zone of seismic IV and buildings in Zone of seismic V i.e., existing design codes of seismic (India) and from other countries are inadequate for building structure that are on the hill slopes.

It was also observed that slope has significant impact on efficiency of seismic, therefore a control method to decide the best configuration could need to be established further.

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Bandwidth Enhancement of Micro Strip Square Patch Antenna with Partial Ground Plane for Wide Band Applications

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Abstract— This paper focused to resolve two issues, which are to construct an antenna with wide bandwidth and an antenna, which can be used for distinct wireless technologies that can operate at different frequencies. Bandwidth is the most import factor in designing micro strip patch antennas. Inherently patch antennas are narrow-band but in today's scenario high data rates are quite common in wireless communication technology. To handle these high data rates wide bandwidth is required. In this paper partial ground plane, technique is used to enhance the bandwidth of antenna. A square patch antenna for wide band applications operating at a frequency band of 2 to 8 GHz has been designed using CST Microwave Studio and fabricated. Measured and simulated results are compared and they are in good agreement. Proposed Antenna covers various wireless standards such as Bluetooth (2.4 GHz), WLAN (2.4, 5.1-5.8 GHz), WiMAX (2.3-5.7 GHz), X-band satellite applications (7.1-7.76 GHz). The proposed antenna is modeled with gl=27.9 mm and pl=pw=17 mm is exhibiting wide bandwidth of 5.5 GHz and fractional Bandwidth of 111% and return loss is well below -10dB for the entire frequency range.

Keywords— Wireless Local Area Network, Worldwide Interoperability for Microwave Access, Return Loss, Wireless Personal Area Networks, Wireless Applications

I. INTRODUCTION

Compact size of the antenna is the most demanding factor in modern communication systems because of their multi and wideband characteristics [1], [2]. Compact size antenna requirement made the designers to select the Micro Strip Antennas (MSA's) because of their features like low cost, small size, less weight, low profile and conformal shape [3], [4]. These features make MSA's highly desirable and extremely required for development. The demand for multi band and wideband antennas [5]-[8] is increasing in present day scenario because various wireless applications operating at different frequencies can be supported by modern communication systems. Due to advances in wireless technologies the need for wideband antennas is increasing, since single device can be used for different applications such as text, audio, video, multimedia streaming [9]. The demand for high data rate and channel bandwidth is always a primary area of concern in modern wireless communications, which caused the FCC to release unlicensed radio communication band (3.1GHz-10.6GHz) [10]. Wireless Personal Area Networks [WPAN] uses this unlicensed band [11]. The bandwidth of the antenna should be greater than 1.5 GHz to meet UWB operation [12]. A lot of research has been going on by the researchers in the field of wideband antennas. Many techniques are used to achieve wideband characteristics such as partial ground plane; defected ground plane, monopole patch, fractal patch and micro strip patch [9-11], [13-15], [17-25].

II. DESIGN CONCEPT

The conventional construction of MSA is shown in Figure1. It mainly consists of top, substrate and bottom layers. The top layer mainly comprises two parts; the first one is called patch that may take any possible geometric shape and the second one is called micro strip feed line. This layer is photo engraved on substrate. The most common used type of substrate layer is FR4 since it is widely available in the market and has low value of loss tangent. The performance of antenna can be improved by controlling the thickness of substrate *h*, so that it is considered as principal factor for determining antenna performance. To improve the antenna parameters low permittivity thicker substrate can be used which leads increase in antenna size. Therefore, a tradeoff should be made between antenna dimensions and antenna performance [16]. To increase the bandwidth of MSA ground plane layer or bottom layer also called as last layer is used. Shape of the ground plane can affect the operating parameters of the antenna it can be full or partial.

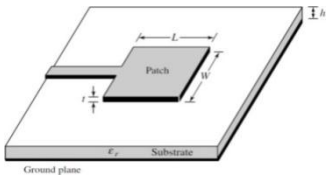


Fig. 1. Physical Structure of MSA

III. ANTENNA GEOMETRY

The proposed model is based on the partial ground plane concept of changing the length of the ground plane to enhance the bandwidth. A micro strip square patch antenna is designed and modeled by using CST Microwave Studio software. Fig. 2 shows the geometry of the proposed antenna. FR-4 substrate with thickness of 1.6 mm, loss tangent of 0.02 and relative permittivity of 4.4 is used .The dimension of substrate is 42×50 mm^2 for designing of

square patch antenna. The square patch antenna width (pw) =17 mm, length (pl) =17 mm and Feed line width 2.6 mm and length 29.91 mm. The 50Ω micro strip line was used as a feeding technique. Table I lists the dimensions of the proposed antenna.

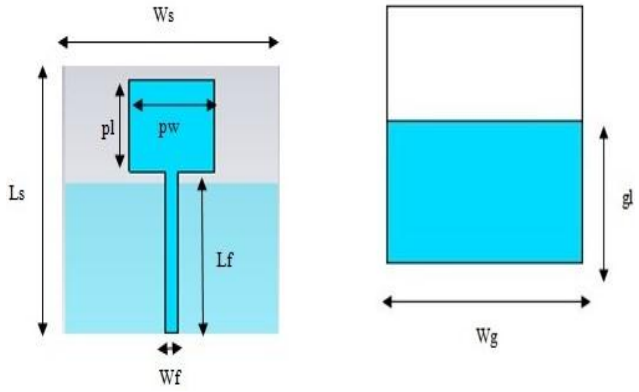


Fig. 2 .Geometry of square patch antenna with Partial Ground Plane (a) front view (b) back view

TABLE I: Proposed antenna dimensions

S.No	Parameter	Values(mm)
1	Ws	42
2	Ls	50
3	Pl	17
4	Pw	17
5	Lf	29.91
6	Wf	2.6
7	gl	27.9

IV. PARAMETRIC ANALYSIS OF THE PROPOSED ANTENNA

Various design parameters like ground length, patch length and patch width are studied to identify their effect on return loss and fractional bandwidth of the proposed antenna.

From Fig. 3. we can see for gl=26.9 mm and pl=pw=16 mm multiple resonances are occurring at 3.14 GHz, 5.95 GHz and the antenna is operating in the band 2.19-7.29 GHz resulting in a bandwidth of 5 GHz. for gl=26.9 mm and pl=pw=17 mm multiple resonances are occurring at

3.12 GHz, 5.63 GHz and there is slight change in the lower cut off frequency of the antenna but upper cut off frequency is decreased to 6.34 GHz and bandwidth is decreased to 4.19 GHz. for gl=26.9 mm and pl=pw=18 mm multiple resonances are occurring at 2.5 GHz, 3.1GHz ,5.2 GHz and there is slight change in the lower cut off frequency of the antenna but upper cut off frequency is decreased to 6GHz and bandwidth is reduced further to 3.9 GHz.

From Fig. 4. by increasing the gl=27.9 mm and pl=pw=16 mm we can see lower cutoff frequency is raised to 2.39 GHz and upper cutoff frequency raised to 7.79 GHz and bandwidth is 5.43 GHz. By increasing the pl=pw=17 mm we can see lower cutoff frequency is dropped to 2.2 GHz and upper cutoff frequency not much changed ,so increase in the bandwidth is observed which is equal to 5.5GHz. By still increasing the pl=pw=18 mm we can see no change in lower cutoff frequency but cutoff frequency is dropped to 7.5 GHz upper resulting in a bandwidth of 5.38 GHZ.

From Fig. 5. by increasing the gl=28.9 mm and pl=pw=16 mm we can see lower cutoff frequency is raised to 3.28 GHz and upper cutoff frequency raised to 8 GHz and bandwidth is dropped to4.72 GHz. By increasing the pl=pw=17 mm we can see the same behavior as above. By still increasing the pl=pw=18 mm we can see lower cutoff frequency is dropped to 2.5 GHz but upper cutoff frequency is same resulting in a bandwidth of 5.5 GHZ.

Table II summarizes the effect of length of ground plane and patch width and lengths on the operating parameters of the antenna like resonant frequency, returns loss, bandwidth, and fractional bandwidth etc.

Gain versus frequency for different values of ground lengths and patch lengths and patch widths are shown in fig. 6. to fig. 9. For gl=26.9 mm and for different values of pl and pw the gain is varying between 1.4 to 3.9 dB. For gl=27.9 mm and for different values of pl and pw the gain is varying between 1.4 to 4 dB. For gl=28.9 mm and for different values of pl and pw the gain is varying between 1.2 to 4 dB.

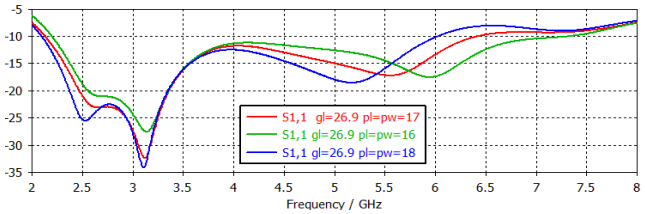


Fig. 3. Parametric plot of Return Loss for gl=26.9 for different values of pl and pw

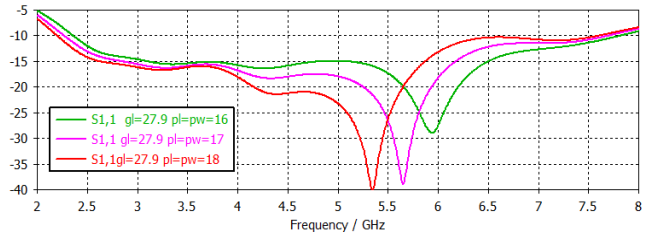


Fig. 4. Parametric plot of Return Loss for gl=27.9 for different values of pl and pw

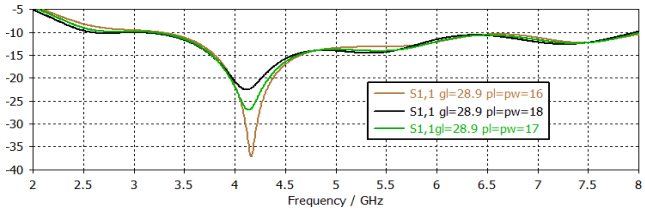


Fig. 5. Parametric plot of Return Loss for gl=28.9 for different values of pl and pw

TABLE 1I: PARAMETRIC ANALYSIS RESULTS

Length of ground (*gl*)	Patch Length(pl)= Patch Width (pw)	Resonances	S11(dB) Return Loss	Bandwidth	Fractional Bandwidth (%)
26.9	16	3.14GHz 5.95 GHz	-27.53 -17.51	5GHz	105.3
26.9	17	3.12GHz 5.63 GHz	-32.32 -17.18	4.2 GHz	98.8
26.9	18	2.5 1GHz 3.11 GHz 5.23 GHz	-25.40 -34.05 -18.42	3.9 GHz	96.2
27.9	16	5.93 GHz	-28.92	5.43 GHz	106.9
27.9	17	5.6 GHz	-38.86	5.5 GHz	111
27.9	18	5.3 GHz	-39.96	5.38 GHz	97.7
28.9	16	4.16 GHz	-37.15	4.72 GHz	78.3
28.9	17	4.72 GHz	-27.01	4.72 GHz	85.7
28.9	18	4.11 GHz	-22.58	5.5 GHz	104.7

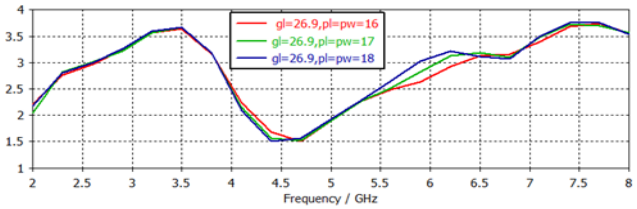


Fig. 6. Gain versus frequency for gl=27.9

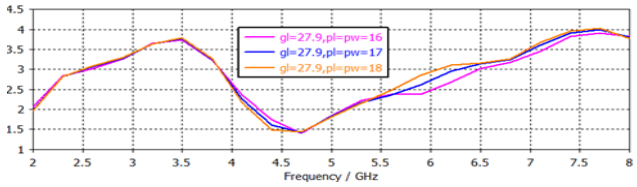


Fig. 7. Gain versus frequency for gl=27.9

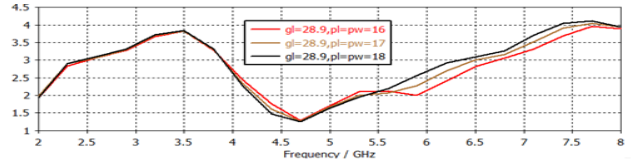
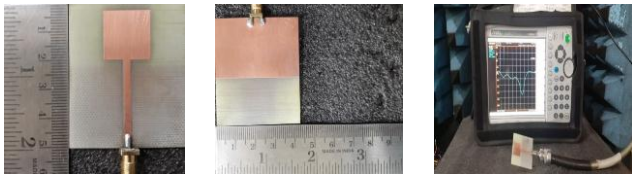


Fig. 8. Gain versus frequency for gl=28.9



(a) (b) (c)

Fig. 9. Geometry of the fabricated square patch antenna with Partial Ground Plane (a) front view (b) back view (c) S11 measurement setup

TABLE III

ANTENNA COMPARISON WITH EARLIER REPORTED RESULTS

References	Frequency band (GHz)	Dimensions (mm3)	Bandwidth ratio
[17]	2.2 (3.4–5.6)	70 X 70 X1.6	1.6:1
[18]	2.46 (2.71–5.17)	35 X 35 X 1.5	1.9:1
[19]	1.8 (2.4–4.2)	90X 40 X 0.79	1.8:1
[20]	3.13 (2.23–5.36)	37 X37 X 1.6	2.4:1
[21]	0.62 (1.9–2.52) and 1.2 (5.0–6.2)	58 X 62 X 2.0	1.3:1 and 1.2:1
[22]	5.76 (2.94–8.7)	26 X 26 X 1.6	3.0:1
[23]	4.8 (2.0–6.8)	50 X 55 X 1.5	3.4:1
[24]	0.41 (2.26–2.67) and 3.78 (3.0–6.78)	24 X 35 X 1.6	1.2:1 and 2.3:1
Proposed Antenna	5.5(2.2-7)	42 X 50 X 1.6	3.1:1

V. ANTENNA FABRICATION AND MEASURED RESULTS

Fig. 9 shows the top and bottom view of the fabricated prototype antenna. The antenna is fabricated on a FR-4 substrate with thickness of 1.6 mm, loss tangent of 0.02 and relative permittivity of 4.4. The dimension of substrate is 42×50 mm^2. The return loss of the proposed antenna is measured using Anritsu MS2037C combinational Analyzer and compared with the simulated results. Fig. 10 shows the simulated and measured return loss values. Figure 11 illustrates the radiation pattern of the proposed antenna.

The measured and simulated antenna bandwidths are 5.5 GHz (2.2-7.7 GHz) and 5.3GHz (2.2-7.5GHz) respectively which are in good agreements. The proposed antenna can be used for Bluetooth (2.4GHz), WLAN (2.4, 5.1-5.8 GHz), WiMAX (2.3-5.7 GHz), X-band satellite applications (7.1-7.76GHz). In Table III a comparison of proposed antenna structure with other earlier reported results in terms of antenna dimensions, bandwidth ratio, frequency bands is tabulated [17]-[24].It can be clearly stated from the table that proposed antenna is wideband and simple, small, compact in overall dimensions compared to most of the presented structures.

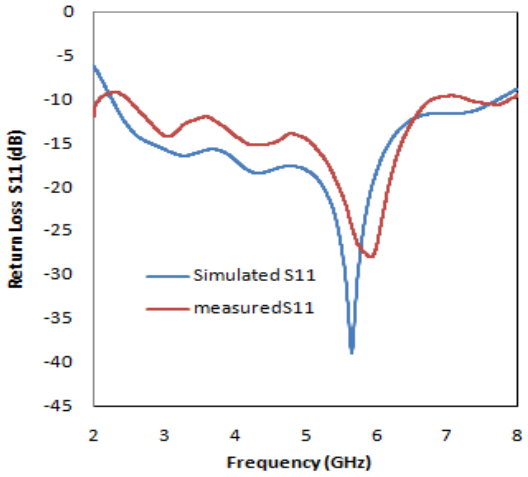
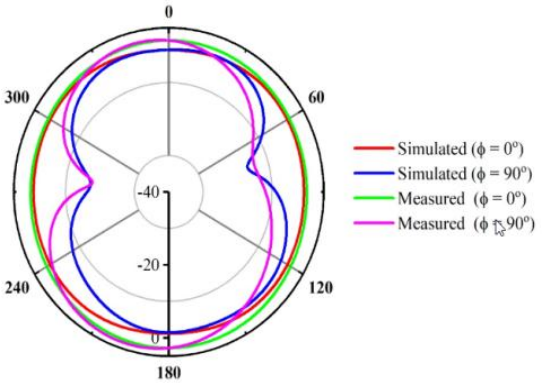
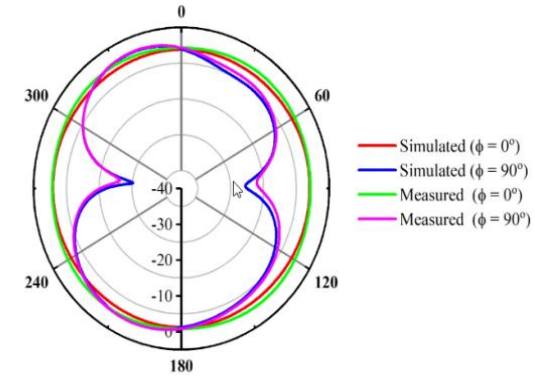


Fig. 10. Simulated and measured return loss of the proposed antenna

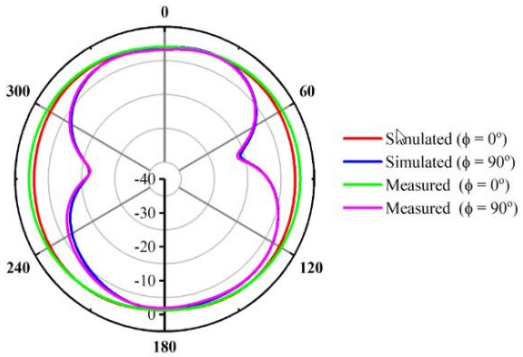
Radiation patterns



(a)



(b)



(c)

Fig. 11. Radiation patterns at a) 2.9 GHz b) 5.5 GHz c) 7.5 GHz

VI. CONCLUSION

An antenna for wideband applications operating in the frequency range 2-8 GHz has been designed, simulated using CST Microwave Studio and fabricated. This square patch micro strip antenna with partial ground plane exhibited more bandwidth. The antenna exhibits the return loss well below -10dB for the frequency range mentioned for the ground lengths varying in the range between 26.9 mm and 28.9 mm. The proposed antenna model of gl=27.9 mm and pl=pw=17 mm is exhibiting wide bandwidth of 5.5 GHz and Impedance Bandwidth of 111%. From the simulation and measured results obtained, it is observed that this proposed square patch antenna can be used for various wireless standards such as Bluetooth (2.4GHz), WLAN (2.4, 5.1-5.8 GHz), WiMAX (2.3-5.7 GHz), X-band satellite applications (7.1-7.76GHz).

VII. ABBREVIATION AND ACRONYMS

UWB: Ultra-Wide Band

WLAN: Wireless Local Area Networks

Wi-Max: Worldwide Interoperability for Microwave Access

WPAN: Wireless Personal Area Networks

FR4: Florent Resonator

FCC: Federal Communication Commission

DGS: Defected Ground Structure

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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Image Classification Using TensorFlow

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Abstract— We developed and trained our models using two popular Deep Learning Libraries which are TensorFlow and KERAS. These two popular libraries are mostly used in industries because of their flexibility and lucidity. Here we will be talking/using TensorFlow. For this, we need to use Python to work with TensorFlow.

Keywords— TensorFlow, Keras, Convolutional Neural Network, Activation Functions, Loss Functions, Optimizers, Supervised Learning

I. INTRODUCTION

Image classification has been on the rise and is becoming a trend among technology developers, particularly with data growth in different sectors of industry such as e-commerce, auto, healthcare, and gambling. The most obvious example of this technology is applied to Google Photos. Google Photos can now detect up to 82% accuracy to identify your face with just a few marked and classified pictures in your photo album. The technology itself almost surpasses the human ability to classify or recognize an image.

Machine Vision has a different context when it comes to image classification. The capability of this technology is to recognize people, objects, locations, action and writing in images. The combination of artificial intelligence software and machine vision technologies allows for the exceptional result of image classification.

Deeper neural networks are more difficult to train. We present a residual learning framework to facilitate the formation of networks which are far deeper than those used before. We explicitly rephrase layers as residual learning functions by referring to layer inputs, rather than learning non-state functions.

II. RELATED WORKS

In this project, we will use Convolutional Neural Network for classifying images, since Convolutional Neural Network (CNN) won the image classification competition 202 (ILSVRC12), a lot of attention has been paid to deep layer CNN study. CNN's success is attributed to its superior multi-scale high-level image depictions rather than its low-level manual engineering features.

According to , the journal discussed on image classification system based on a structure of a Convolutional Neural Network (CNN). The training was performed such that a balanced number of face images and non-face images were used for training by deriving additional face images from the face images data. The image classification system employs the bi-scale CNN with 120 trained data and the auto-stage training achieves 81.6% detection rate with only six false positives on Face Detection Data Set and Benchmark (FDDB), where the current state of the art achieves about 80% detection rate with 50 false positives.

From the research used Decision Tree (DT) as the techniques in image classification. The DT has multiple datasets that are located under each of Hierarchical classifier. It must be done in order to calculate membership for each of the classes. The classifier allowed some rejection of the class on the intermediary stages. This method also required three parts as the first is to find terminal nodes and the second in placing the class in it. The third is the segmentation of the nodes. This approach is considered to be very simple and effective.

The experiment results prove that the proposed solution will be the greatest tool for dealing with practical problems which are related to use deep CNNs on a small dataset. Our approach not only considerably reduces the need for important training data, but also effectively expands the training data set. The most commonly used parametric classifier is the maximum likelihood classifier (MLC). Contrary to parametric classification, non-parametric classification is not based on statistical hypotheses or parameters.

On the basis of the review, he suggested a rapid classification of images by stimulating fuzzy classifiers. It was a simple way to differentiate between known and unknown category. This method is simply to boost Meta knowledge where local features can be found mainly. It has been tested with a few big image data and compared with the bag-of-features image template. The result gave much better classification accuracy as it was a testing process that gave a short period of time where it produced 30% shorter compared to the previous one.

Name/Year	Title of project	Purpose	Method Used
Gregor, Danihelka, Graves, Rezende, & Wierstra (2015)	DRAW: A Recurrent Neural Network for Image Generation	➢ Train neural network for image classification ➢ Trained complex images with MNIST models	Artificial Neural Network (ANN)
Rastegari, Ordonez, Redmon, & Farhadi (2016)	XNOR-Net: ImageNet Classification Using Binary Convolutional Neural Networks	➢ Balanced number of face images and non-face images are used for training ➢ Employing the bi-scale CNN 120 trained with the auto-stage training	Convolutional Neural Network
Kamavisdar, Saluja, & Agrawal (2013)	A Survey On Image Classification Application Techniques	➢ Multiple dataset that being located under each of Hierarchical classifier ➢ Rejection of the class on the intermediary stage	Decision Tree
Pasolli, Melgani, Tuia, Pacifici, & Emery (2014)	SVM Active Learning Approach for Image Classification Using Spatial Information	➢ Combining spatial information from sequential process of trial process with spectral	Support Vector Machine (SVM)
Korytkowski, Rutkowski, & Scherer (2016)	Fast Image Classication by Boosting Fuzzy Classifiers	➢ Simply boosting Meta knowledge where local characteristic can be mostly found	Fuzzy Classifiers

Table 1. Related works of classification systems

III. METHOD

Based on figure 1, it is the image classification framework in which deep neural networks are also applied. The process is divided into four (4) phases, each of which will be discussed. Every phase is included on TensorFlow as an open source software and Python as a programming language. Then, the process goes on to collect some of the images (inputs), apply CNN and finally all the images will be classified in their groups.

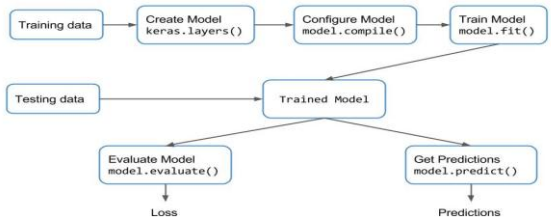


Figure 1. Block diagram for image classification systems

Image Training

In this paper , training set is what it sounds like. It's the set of data used to train the model. During each epoch, our model will be trained over and over again on this same data in our training set, and it will continue to learn about the features of this data. One of the major reasons we need a validation set is to ensure that our model is not overfitting to the data in the training set. During training, if we're also validating the model on the validation set and see that the results it's giving for the validation data are just as good as the results it's giving for the training data, then we can be more confident that our model is not overfitting.

The input data from this article mostly use thousands of images. All these pictures are extracted from Image Net. ImageNet was also known as the Large Scale Visual Recognition Challenge where it is a competition about detection and classified thousands of objects in its categories. This is a yearly competition from 2010 to the present.

Figure 2. Images of horse from dataset

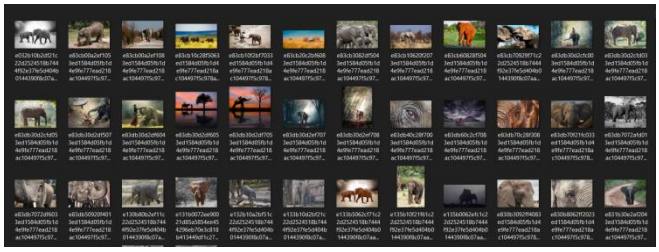


Figure 3. Images of elephant from dataset

Implementation of Convolutional Neural Network

As shown in Figure, it consists of five (8) data inputs (eight type of different animals) and undergoes training with multiple hidden layers. The inputs are also set with fixed-size of the 224x224 RGB image. The convolution process is configured with MobileNet as it produces an efficient convolution neural networks.

Table 2. Number of images to the type of animals

No.	Type of Animal	No of Images
1.	Butterfly	2112
2.	Chicken	3098
3.	Cow	1866
4.	Elephant	1446
5.	Horse	2623
6.	Sheep	1820
7.	Spider	4821
8.	Squirrel	1862
	TOTAL	19658

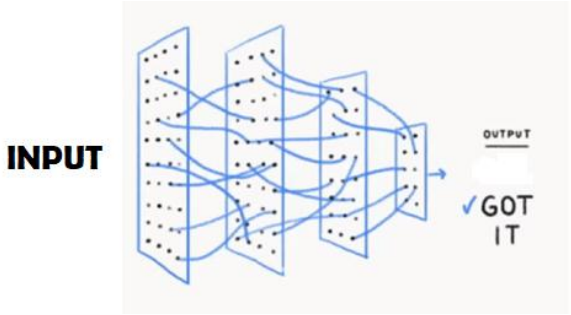


Figure 4. CNN process towards animal images.

V.I Classification of System

Image classification twill be implemented using TensorFlow.

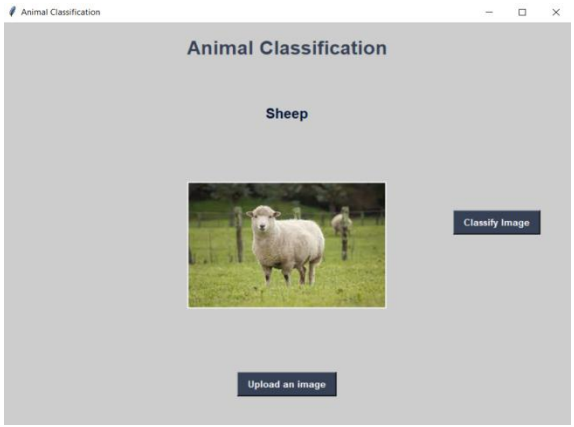
Python language is used in the programming language. System starts collecting images of animals from the data set. Then ,CNN is applied to train the model. Running for validation or testing and if it is not the image of a particular flower that is supposed to act as output then it should start over from CNN. The process ends when the output is categorized in the right kind of animal. It has five (8) types of the animals which are Butterfly, Chicken, Cow, Elephant, Horse, Sheep, Spider, Squirrel. After that, all of these input images undergo 'training' with the convolutional neural network (CNN).

The convolutional neural network (CNN) had to train all of these sets of data until the systems recognize each of these 19658 images. Then, each of the classifications occurred when one of the images being tested whether it belongs to any of these eight (8) types of animals.

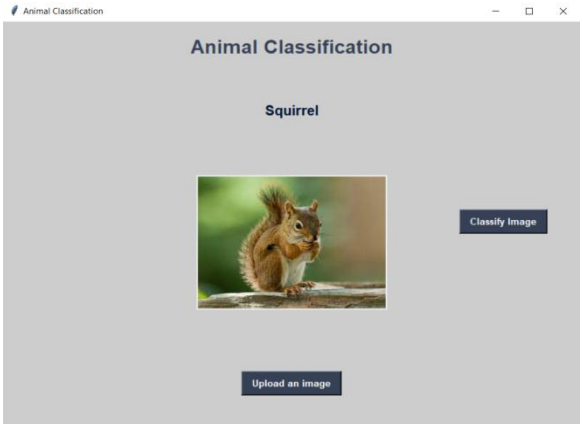
IV. RESULT

When an image is given as input, the model which was trained through Neural Networks detects the feature from the input image and then it predicts the output of the image. the model trained on neural networks in this project is animal classifier which predicts the output with an accuracy of 80%.

A sheep picture is uploaded and then make computer to recognize/categorize the output. The result is categorized according to the model that formed and have a better understanding of the exact appearance of sheep. Then processing takes place and finally the output is predicted.



A squirrel picture is uploaded and then make computer to recognize/categorize the output. The result is categorized according to the model that formed and have a better understanding of the exact appearance of squirrel. Then processing takes place and finally the output is predicted.



V. CONCLUSION

To conclude, this research focuses on the classification of images using deep learning through the TensorFlow framework. Three (3) objectives were achieved as part of this research. The objectives are linked directly with conclusions because it can determine whether all objectives are successfully achieved or not. . It can be concluded that all results that have been obtained, showed quite impressive outcomes. The convolutional neural network (CNN) becomes the main agenda for this research, especially in image classification technology. CNN technique was studied in more details starting from assembling, training model and to classify images into categories.

TensorFlow also gave good results as it is able to simulate, train and classified with up to 90% percent of accuracy towards eight (8) different types of animals. TensorFlow framework which leads to designing of the system involved Python from start until ends.

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International Conference on Technological Advancement in Science, Engineering, Management & Pharmaceutics

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A Review on People Perception and Adaptability of E-Banking in India

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Abstract— The 21st century is fast moving century. Banking has never been more essential to us than it is today. But now the products and service provided by bank branches are not adequate to meet the customer needs. Clients are progressively requesting more values and services modified to their accurate necessities, at discounted cost and as fast as could be expected. The demands of the customers have been shifted from time bound baking to anytime-anywhere banking. The discoveries exhibit that banks are developing e-banking platforms to remain competitive, to manage services with technology advancement and to gain profit. E-banking has proven itself a less costly method for banking transactions.

Present financial business specially banking sector depends on the utilization of information technology. E banking services can not only offers wide range of products and services but also it have the potential to cater the need of existing as well as new prospective customers. This utility of E-banking technology motivates banks to design and develop their own e-banking products. Banks are operating different E-banking platforms to cater the different needs of the customers. The aim of current paper is to cover reviews of the past studies towards Customers perception and adaptability on E-banking services and its effects. The principle findings of this paper are perception of E-Banking for Bank as well as clients. On one way is describes the serious issues bank faces i.e. the low response rate from clients and the implementation of security and information assurance systems and on the other hand the moderately low Internet use and speed, lesser financial literacy and technical literacy and use of new updates in financial products or services and security and protection of data and information and lack of personal contact are the primary factors that affect the adaption of E-banking services by clients. However convenience and any time banking attracts them to adopt it.

Keywords— Adaptability, E-banking Services, Mobile Banking, People Perception, Satisfaction

I. INTRODUCTION

Information Technology has become an important tool for easy access in the present fast moving world. The use of data innovation (IT) and extensive use of computers or mobile has seen colossal development in the service sector in recent past. The banking industry is the best example of it. Banks today work in an exceptionally globalized, liberalized, privatized and a competitive environment. The use of IT has introduced an entirely new and previously unexplored paradigm for the banking business. Indian financial industry has seen gigantic advancements because of developments that are occurring in the Information technology. IT in Banking or Banking Technology is progressively contributing a critical part in improving the services in the financial business. The expression "Banking Technology" refers to the utilization of complex data and information and customization of products and services using the new updated technology empower banks to offer better services to its clients in a safe, dependable and affordable manner and sustain competitive advantage over other banks.

Banking is very important and crucial part of our day to day life. . The development of technology, information system, equipment and the accessibility of the mobile services and internet have provided basic infrastructure required for E-banking platforms. Most of the people now has access to banking facilities from anywhere and they do not need the bank branch to be available nearby. E-banking has broken the boundaries of branch banking.

E-banking is a generic term for utilizing electronic channels through Personal computers, Mobile phones, Internet cafe etc. for delivering of banking services and products. Studies have proven that the increase use of E-banking services has improved customer service level of banks and also has created stronger relationship among them. E banking platforms has provided all financial power related to their account and money in the hand of the customer itself. They can presently take care of bills, can transfer money to other accounts, can check account history, can download account statement and can perform other financial activities quickly and easily. The idea and extent of E-banking is as yet in the transitional stage. Many things have been introduced and many are in development phase. E-banking services have the potential to make financial services at the fingertips of the customers where customer can feel himself as true king.

II. REVIEW OF PAST STUDIES

“Consumer acceptance of online banking: an extension of the technology acceptance model” by Pikkarainen, T., Pikkarainen, K., Karjaluoto, H., & Pahnila, S. in Internet research, 14(3), 224- 235 (2004) suggested that time accessibility; updated data, reminders to make installment and so on are the excellent explanations behind advancing e banking channels.

“Internet banking acceptance model: Cross-market examination” By Alsajjan, B. and Dennis, C. (2010)

published in Journal of Business Research, pp. 957-963 proposed a model to quantify shoppers' acknowledgment of Internet banking, the Internet banking acknowledgment model (IBAM).

"E-banking: challenges and opportunities in the Greek banking sector" by Georgios Angelakopoulos and Athanassios Mihiotis published in Electron Commer Res (2011) 11:297–319 suggest that E-banking has changed the manner in which banks have been leading their business for a long time. Since new innovative advancements are arising each day, E-banking has still a great deal to bring to the table to banks and their clients.

"The rise of customer-oriented banking - electronic markets are paving the way for change in the financial industry" by Rainer Alt & Thomas Puschmann published in Electron Markets (2012) 22:203–215, this paper represents that how change in technology and behavior of the customers are driving banks to develop and offer more customer oriented E-banking services to sustain and remain competitive in the future.

"New approach to study of factors affecting adoption of electronic banking services with emphasis on the role of positive word of mouth" by Ashtiani, P.G. and Iranmanesh, A. published in African Journal of Business Management, 2012, Vol. 6, No. 11, pp. 4328 presumed that positive verbal publicity has positively affected electronic financial adoption and the trust in bank, while negative verbal publicity is apparently dangerous towards E Banking services.

"E-Banking Services-In Indian Scenario" by Shaik, Shakir, and Noor Basha Abdul published in International Journal of Management Research and Reviews 3.9 (2013): 3545 analyzed and informed that Numerous money related developments like ATMs, MasterCard's, RTGS, charge cards, versatile banking and so on have completely changed the way Indian Banks works.

"Customer Satisfaction in Commercial Banks- A case study of Bank of Baroda" by Sharma, B.S. and Aggarwal, P. published in International Research Journal of Management and Commerce, 2014 Vol. 1, Issue 9, pp. 8-18 assessed the awareness level of clients about electronic financial services and level of acceptance of e-banking services by Bank of Baroda's clients. They tracked down that adaptability of electronic banking by clients is expanding and it helping banks with increased consumer loyalty. These variables; curtsey, exactness and speed are a significant factor for a Bank of Baroda for improving consumer loyalty towards electronic financial Services.

"A Study on Impact of Information Technology in Banking Sector with Reference to Southern Tamilnadu" by Rajesh, R. and Palpandi, A. published in International Conference on Inter Disciplinary Research in Engineering and Technology, 2015 pp. 17-22. Analyzed the perception of clients utilizing e-banking services in Southern Tamilnadu and clarified the effect of information technology in the financial services offered by banks. They inferred that E Banking services increased customer satisfaction and at the same time E-Services needs to be improved according to changing innovation tendency.

"Factors Affecting Mobile Banking Adoption Behavior in India" by Amit Shankar and Pooja Kumari, IIT, Kharagpur published in Journal of Internet Banking and Commerce April 2016, vol. 21, no. 1. This paper suggests that the bank should consider various factors while developing M-banking application and services. The use of available information and further research need to be carried out to make any strategies for developing E-banking services for existing or prospective clients. Bank should also ensure that proper information and training to be imparted for users of E–Banking products.

"Usage of Alternate Banking Channels as an Effective Tool for CRM Enhancement- An Empirical Study" by Sunil C V and Dr. Ashok Kumar M published in IJSTE - International Journal of Science Technology & Engineering | Volume 3 | Issue 06 | December 2016 states that Branchless Banking is the future and E Banking channels are used for delivering financial services without relying on the bank branches.

"Study of E-Banking Scenario in India" by Shubhara Jindal published in International Journal of Science and Research (IJSR) Volume 5 Issue 12, December 2016 suggests that E-banking is need of the hour and it can never be neglected. Only those banks will sustain in future which will get along with the changes according to technology advancement and develop services as per client requirements because eventual fate of the banks will stay in the possession of clients.

"Digital Payment Sector: The Sunrise Industry in India: A Review," by Hyma Goparaju published in The IUP Journal of Business Strategy, Vol. XIV, No. 2, 2017 suggests that Technological advancements in Cell phones and Bank mobile applications (apps) will promote and drive the adoption of E-Banking channels.

"Impact of Demonetization on E-Banking Services - A Study with Reference to Banks in Erode District" by Mrs. S. Vanitha Dr. S. Maheskumar published in International Journal of Trend in Scientific Research and Development Volume – 2, Issue 1, Nov-Dec 2017 states that Due to demonetization, Alternative payment methods, such as E-wallets, Internet-banking, Mobile Banking, Use of Debit and Credit Card has been increased and this will shift an efficient cashless infrastructure.

"A Comparative Study on Pre and Post Demonetization on E-Banking Services" by Dr. T.Lata Sujata published in IOSR Journal of Business and Management, e-ISSN: 2278-487X, p-ISSN: 2319-7668 PP 12-17 addresses Banks that they should be worried about the adaptability issues of clients regards acceptance of web based banking. More awareness about E banking products and services and Customer's data and money security concerns should be taken care of by Banks.

"Impact of Demonetization on Indian Banking Sector: A Step towards Governance" by Nahas Sha A.A published in EPRA International Journal of Economic and Business Review Volume - 6, Issue- 4, April 2018 | e-ISSN : 2347 - 9671| p- ISSN : 2349 – 0187. This paper examines impression of Kerala individuals toward e-banking. It concludes that Technology has affected the bank customers and encouraging them to use alternative banking services.

"Trends and turning points of banking: a timespan view" by Payam Hanafizadeh and Seyedali Marjaie published in Review of Managerial Science 12 March 2019 finds out that financial crisis and competition are two important factors that will fundamentally affect the launch of future exploration roads in banking studies.

"Adaptation of Digital Banking Channel by Indian Consumers" by Agarwal, M. K. published in Journal of The Gujrat Research Society, Vol. 21, No. 16, pp. 110-118. This study is focused over age wise behavior and their respective acceptances level of E-banking Services. It also analyses their opinion and adaptability level of E-banking services. Online saving, investment plans and online bill payments are the significant factor which impacts the clients to adopt E- banking.

"Security perception of E-banking users in India: an analytical hierarchy process" by Mahesh Kumar and Sanjay Gupta published in Banks and Bank Systems, Volume 15, Issue 1, 2020, this paper expresses that among the variables considered, security is considered most important by E-Banking users.

"Trends and Challenges in Adoption of E-Payment Services in India" by S.Karunakaran, A.Sivakumar, J.Balaji, D.Kumaresan, D.Muralidhar published in International Journal of Engineering and Advanced Technology, Volume 9, Issue 4, April 2020, this article reveals that E-Payment options have been accepted and proven to be most important payment method worldwide.

"Customer Awareness Towards E Banking Services In India- A Comparative Study Of Public And Private Sector Banks" By Shilpa Arora & Dr. Priyanka Singh published in International Journal Of Mechanical And Production Engineering Research And Development, Vol 10, Issue 3, Jun 2020, 6821–6826 suggests that banks needs to adopt new methods and ways to make their customers aware about the E banking products and services offered by them.

"Comprehensive review of the effects of electronic banking on the performance and profitability in the banking sector" by Sweety Gupta Dr. Anshu Yadav Dr. Broto Bhardwaj published in International Journal of Advanced Research in Engineering and Technology (IJARET) Volume 11, Issue 12, December 2020, pp.427-437, This paper informs that E-banking has showed a positive impact on customer service and satisfaction but bank also has to improve connectivity, digital infrastructure and customers awareness. Bank should also enhance the knowledge and skills about E-banking to its staff.

"Banking on the Future: Vision 2020" by Confederation of Indian Industry -Deloitte state that information management and data security is very important factors and should be properly taken care of by banks against any possible cyber threats. This article suggests technology oriented banking system which uses automated processes, complex data alalyses and artificial intelligence to provide cost effective better product and services.

"Retail Banking 2020 Evolution or Revolution?" www.pwc.com/banking, this articles states that Banks must not only work on today's requirements, but also deeply innovate and transform themselves for the future. They should focus on developing a customer-centric simplified business and operating model. Banks should focus on obtaining an information advantage by Enabling innovation, and the capabilities.

"Recent Trends in Indian Banks: An Overview" by Anuj Kumar Solanki published in AIMS Journal Of Management, Vol. 6, No. 1, July 2020, This paper is an attempt to feature the new and arising patterns under challenging conditions faced by Indian banking sector particularly concerning to the digital era.

III. FINDING AND SUGGESTIONS

The following tables summarize the findings of various studies referred and provide positive and negative perceptions of customers and also advantages and challenges for banks. These findings together provide the Perception and adaptability of E-Banking services among stakeholders.

Table 1: FOR BANKS

Advantages	Challenges
➢ Through Branch Banking, Banks has limited customer base and can provide services to limited number of people in a specific area or location however through E-Banking, Banks can get to the mass at several location and can serve all of them together. ➢ By the use of E-banking by customers, Banks can reduce their operational Expenses significantly. ➢ By increase of the use of E-banking channels by customers, the workload in the branches could be reduced	➢ Development of suitable and customized E-baking services takes time and money costs is also incudes. This Time and money cost need to be properly imagined and managed before it loos its competitive and technological advancement. ➢ E-banking uses Technology which comes with some cost and this cost is not small. An investment for establishing, maintaining and replacing the technological infrastructure for E-banking is costly. ➢ Development of E-banking products and services also

➢ With reduced cost and workload, Banks can develop and deliver quality services. ➢ The E-banking channels not only provide alternative way for banking but also provide better and effective platform to inform and deliver several initiatives and offerings of banks effectively and hence may improve its public image. ➢ The increase use of E-banking collects a massive database for several demographical, behavioral, financial and attitudinal data which can be used to understand and provide better and customized services and also help in acquisition of knowledge. ➢ E banking helps banks to reach the mass and to provide cost effective services which in turns increase the volume of business and thus increase the overall income. ➢ E banking are emerging with new technology and with effective use of technology and data interpretation opens new business horizons and creates new business opportunities. ➢ As the E-Banking is growing, more banks are using this platform to attract more customers and thus an intense and healthy competition has been started. This competition encourages bank to keep providing better and customize services.	need proper Training for all stakeholders to understand and use it. Thus training cost is also involve and is a major challenge. ➢ Data Security and maintenance also is very crucial and tedious task for banks to reduce cyber security and for safeguards of the interest of all stakeholders

Table 2: FOR CUSTOMERS

Positive Perceptions	Negative Perceptions
➢ E Banking Provides 24x7 Banking services hence customer does not feel bound in any time limit to do banking transaction. ➢ E-banking helps customers to use better time organisations and priorities the others things along with banking. It also reduced transaction times and thus in returns help to receive goods and services form other industries in time as well. ➢ E-banking does not bound customers to any geographical boundaries. It provides them the platforms to use banking services from anywhere around the world. ➢ E-banking is less costly affair then branch banking for customers. ➢ E-baking channels also have twenty four hour support system to provide timely help and guidance in case of any need. ➢ E-banking also helpful for specially abled people so that they can also utilize banking service as per there convenient. ➢ Change and advancement of technology allows customer to use several banking services under one platform. This can not only save lots of time but also money of customers. ➢ The increasing competitiveness among banks to provide better E-banking services is advantage for customers where they can get better offers and services.	➢ Increasing cybercrime and fear of security of Data and personal or financial information are still the major concerns among many customers and somewhere drags back them from better utilization of E-banking services. ➢ Technology is complex and without proper training or awareness, it's become difficult to adapt it. This is major concern for less adaptability of E-banking services. ➢ E-banking services required proper infrastructure like internet, data and mobile coverage etc. and also specialized equipment like ATM/ Cash Recycler/ Banking Kiosk/ Smart phones/ Laptop/ Desktop etc. to use it properly. Lacking of required infrastructure and specialized equipment also concern for less penetration of E-banking services. ➢ Banking is among essential service and involvement of specialized person is required to understand many bank related things or service. So many people still prefer branch banking so that this personal touch can be ensured. Lack of personal contact is another major concern for E-banking adaptation.

The study proves that the use of E banking has several advantages for banks as well as customers. Yet, Advantages do come together with difficulties and all partners (Banks as well as customers) need to stay on track and mindful towards it so that all are get benefited in full and it doesn't transforms into disaster.

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Data Privacy in Cloud Computing, Implementation by Django, A Python-Based Free and Open-Source Web Framework

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Abstract— Cyber insurance is a viable method for cyber risk transfer. However, it has been shown that depending on the features of the underlying environment, it may or may not improve the state of network security. In this paper, we consider a single profit-maximizing insurer (principal) with voluntarily participating insureds/clients (agents). We are particularly interested in two distinct features of cyber security and their impact on the contract design problem. The first is the interdependent nature of cyber security, whereby one entity's state of security depends not only on its own investment and effort, but also the efforts of others' in the same eco-system (i.e. externalities). The second is the fact that recent advances in Internet measurement combined with machine learning techniques now allow us to perform accurate quantitative assessments of security posture at a firm level. This can be used as a tool to perform an initial security audit, or prescreening, of a prospective client to better enable premium discrimination and the design of customized policies. We show that security interdependency leads to a "profit opportunity" for the insurer, created by the inefficient effort levels exerted by interdependent agents who do not account for the risk externalities when insurance is not available; this is in addition to risk transfer that an insurer typically profits from. Security pre-screening then allows the insurer to take advantage of this additional profit opportunity by designing the appropriate contracts which incentivize agents to increase their effort levels, allowing the insurer to "sell commitment" to interdependent agents, in addition to insuring their risks. We identify conditions under which this type of contracts leads to not only increased profit for the principal, but also an improved state of network security.
Cloud computing providers offer shoppers the opportunity to transfer a native management system to a cloud to network with other information management systems. This makes it possible for resources to be utilized effectively and therefore reduces the cost of manufacturers. The disadvantage of cloud providers is that information in the cloud is safe and affordable. You must encrypt the data before transferring them into the cloud to protect the privacy. The providers have found a cryptographic storage system that shares secure and economic data using the following method, which divides the files and encrypts them in groups in a file block key. These file block keys have been updated and requested to be shared by users. Alternative programs for information sharing with untrusted servers are complicated. The revocation in these schemes extends the suppliers' data and also calls back users. A collusion protection information sharing system provides consumers with secure private keys to add or repeal a customer. The new customers are able to receive the keys from team managers through certified authorities and safe channels. Thus, even when they are using the cloud, a customer revoked will not be able to retrieve common data documents.

Keywords— Native management system, Cloud services, Crypto graphical storage, File-block keys, Cloud Computing, Cloud Security, Secure private keys, Un-trusted cloud

I. INTRODUCTION

The Existing works consider competitive insurance markets under compulsory insurance, and analyze the effect of insurance on agents' security expenditures. The authors of consider a competitive market with homogeneous agents, and show that insurance often deteriorates the state of network security as compared to the no-insurance scenario. The existing studies a network of heterogeneous agents and show that the introduction of insurance cannot improve the state of network security. Study the impact of the degree of agents' interdependence, and show that agents' investments decrease as the degree of interdependence increases. Study a competitive market under the assumption of voluntary participation by agents, with and without moral hazard. In the absence of moral hazard, the insurer can observe agents' investments in security, and hence premium discriminates based on the observed investments. They show that such a market can provide incentives for agents to increase their investments in self-protection. However, they show that under moral hazard, the market will not provide an incentive for improving agents' investments. The impact of insurance on the state of network security in the presence of a monopolistic welfare maximizing insurer has been studied in existing system. In these models, as the insurer's goal is to maximize social welfare, assuming compulsory insurance, agents are incentivized through premium discrimination, i.e., agents with higher investments in security pay lower premiums. As a result, these studies show that insurance can lead to improvement of network security. An insurance market with a monopolistic profit maximizing insurer, under the assumption of voluntary participation, has been studied in existing work, which shows that in the presence of moral hazard, insurance cannot improve network security as compared to the no-insurance scenario.

II. LITERATUER REVIEW

To build trust and confidence among the service providers and data owners a secured network is structured with

various resources in different locations as clouds. Data coloring and watermarking method provide authenticated data, single cloud based on demand, strong access control for data cloud in public and private. Due to increased growth in cloud computing the business is also evolving with the model that delivers security as a service (SECaaS) and data protection as a service (DPaaS) [1].

The cloud computing services are debated for the security challenges which stresses on storage layer and data layer. The paper also discusses about the Map Reduce in Hadoop security in processing large data which are divided and presented parallel with independent tasks. Lastly, the XACML application for Hadoop is discussed and it provides fine access to data control and created safe cloud computing using trusted applications from non-trustworthy server [2].

The data security is well managed by RSA algorithm where the concern user can only access the data. The encryption is performed by the cloud service provider and decryption is safely done by the cloud user only. Thus, data security is provided by implementing the RSA algorithm [3].

The data is protected before storing in the cloud by a new encrypted technique method as explains; it compares 3xAES with AES and T-DES algorithms by calculating encryption, decryption time and key generation time. The security of data is higher based on the key length, i.e. 3xAES has a refined security than AES and 3DES because it encrypts the data 3 times with new key for each encrypt and decrypt [4].

A framework is implemented to show the security levels by performing risk assessment, analysis and mitigation, by covering all cloud service models and cloud deployment models. The reason for accepting this framework is because of the successful secured information execution or alteration of data for cloud computing environment. It is implemented in the logistics Software as a Service (SaaS) is developed and applied to Infrastructure as a Service (IaaS) environment and Platform as a Service (IaaS) to testing this framework [5].

The consumers have accepted the cloud computing services mainly for data storage and privacy safety measures. A brief discussion about the cloud computing process particularly safety issues with few solutions are discussed. The current scope of cloud computing in sharing data lays far behind expectation and the future research work on privacy and security challenges in the cloud are discussed [6].

A cohesive security system offers “Security as a Service” to the organizers as a single-tier or multi-tier based on their need. The safety of the data is evaluated in the cloud at each macro and micro level. This provides an effective solution to the cloud application and to the consumers with similar goals or requirements [7].

The system holds different methods and specific action to present the data from start to the end that is structured based on three cryptographic constraints provided by the user, such as, Confidentiality (C), Availability (A) and Integrity (I). The data in cloud storage are guarded by procedure like the SSL (Secure Socket Layer) 128-bit encryption and also uplifted upto 256-bit encryption on requirement, the authenticity of the data is verified by MAC (Message Authentication Code), searchable encryption and data is divided into three segments in the cloud. Hence, the consumer is provided with a login identity and password to access the data that is secured after data conversion in Section 1, Section 2, and Section 3 [8].

Scholars have conducted numerous surveys about data safety and privacy from software and hardware where data are stored in clouds at different locations. They have also suggested many methods to achieve the highest level of data security in the cloud which has created trust between cloud service provider and users [9].

At present users are concerned about data security issues, mainly virtualization security and data security have been the major problem, thus cloud computing is facing challenges with regard to security issues. Users have stored their information in a cloud and keep transferring from one cloud to another cloud which risks the security of the data. The elliptic curve cryptography technique is used for a faster and more efficient cryptographic key to offer better security, privacy and quality of data in the clouds [10].

The data safety process for cloud computing is improvised by studying the cloud architecture and three solutions are presented. The software is applied to boost the security for cloud computing and recently used in the Amazon EC2 Micro instance [11].

Many studies are conducted to analyse the performance and quality of data processing, secured data storage, data recovery and data collection in IIoT. An efficient and secured data storage and recovery in IIoT is suggested by a structured framework to provide solutions after studying the fog computing and cloud computing. Based on the latency need the data are transferred and stored by the edge server or the cloud server [12].

Two algorithms AES (Advanced Encryption Algorithm) and Blowfish Algorithms are studied which provided double security for the data in the cloud. It mainly offers safety against unauthorised data access. This research paper discusses only about the early proposal and the technical details and data analysis are not briefed [13].

A productive and secured access control environment is created for cloud computing using Attribute Based Encryption (ABE), Distributed Hash Table (DHT) network, and Identity Based Timed Release Encryption (IDTRE). Based on the consumer needs the data is encrypted, segregated and compressed into ciphertext and extracted ciphertext. IDTRE algorithm is installed to encrypt the decryption key. Ciphertext key and extracted ciphertext are clubbed to generate ciphertext shares, that are distributed

into DHT network and the compressed ciphertext are stored in the cloud servers [14].

The cloud data are audited using a public key based on homomorphic authenticator with arbitrary camouflaging. It mainly results in privacy-preserving of data in the cloud and focuses on multiple auditing with a method of bilinear aggregate signature resulting in multiple user setting. For this action TPA is applied to conduct countless auditing tasks simultaneously. Thus, a study revealed that this technique is highly secured and effective [15].

A new approach is presented to the resource users, who trust the cloud services for storage of data efficiently and secured deletion of data. The method includes All-Or-Nothing Transform for strong, secure resource storage and securely divides the resources to finally decentralize the data allocated in the storage network. The resource owners use this model to control their settings that are available and secured [16].

The recent evolving technology is cloud computing, which offers many advantages to the users. But this technology challenges security issues and many solutions are presented to develop secured cloud services. Creative or supported encryption methods along with suitable management systems can be implemented to attain safe data storage and recovery from the cloud. This would allow data access only by enrolled users [17].

A classification technique is presented which describes numerous scopes for data safety at different levels. It provides required safety to the data at each stage that are segregated and stored. Its success is analyses with the sample data stored in the cloud [18].

Ciphertext-Policy Attribute-Based Hierarchical document collection Encryption scheme called CP-ABHE is a combination and construction of access tress. This tree is at regular rise and rose by merging the smaller ones. Each leaf on the tree has a similar secret number that is used for encryption of data, resulting in the enhanced performance. CP-ABHE expressed his work effectively with regard to safety and storage size of the ciphertext [19].

A superior control measure and privacy protection in a multi-authority cloud storage structure is provided by PMDAC-ABSC data access control system which is built on Cipher text Policy ABSC. The authorities and cloud servers are aware of the characteristics of the signcryptor and de-sign Cryptor. Hence this method is confirmed to be safe for normal model by delivering privacy, unidentified validation and public verification [20].

A classified multi-authority attribute-based encryption has a multi-centre attribute authorization arrangement along with a combined attribute index. This method is presented on larger group and identified by its characteristic to structure a dual tree. Based on the child node in an attribute access tree the value of the parent node is identified. In this study the attribute based encryption calculatedly decreases the volume for decryption and compresses the unwanted data in the ciphertext at a greater extend. This encryption method has a hypothetical and real-world significance in the system of “large universe” constructions [21].

Mediated Constant Ciphertext-Policy ABE (MCCP-ABE) and a mediated revocation are constructed to give solutions for storage and deletion. A third-party server are designed using these methods for enabling file transmission in semi trusted pattern for access control. The performance is evaluated that resulted in holding a constant-length numeric ABE ciphertext and limited duration in conducting selective and partial revocation [22].

III. CLOUD COMPUTING TYPES

2.1. Private Cloud Private cloud is cloud infrastructure operated solely for a single organization, whether managed internally or by a third-party, and hosted either internally or externally. Undertaking a private cloud project requires a significant level and degree of engagement to virtualize the business environment, and requires the organization to reevaluate decisions about existing resources. Self-run data centers are generally capital intensive. They have a significant physical footprint, requiring allocations of space, hardware and environmental controls.

2.2. Public Cloud A cloud is called a "public cloud" when the services are rendered over a network that is open for public use. Public cloud services may be free or offered on a pay-per-usage model. However, security consideration may be substantially different for services (applications, storage, and other resources) that are made available by a service provider for a public audience and when communication is effected over a non-trusted network. Generally, public cloud service providers like Amazon AWS, Microsoft and Google own and operate the infrastructure at their data center and access is generally via the Internet. AWS and Microsoft also offer direct connect services called "AWS Direct Connect" and "Azure Express Route" respectively, such connections require customers to purchase or lease a private connection to a peering point offered by the cloud provider. 2.3. Hybrid Cloud Hybrid Cloud is an integrated cloud service utilizing both private and public clouds to perform distinct functions within the same organization. All cloud computing services should offer certain efficiencies to differing degrees but public cloud services are likely to be more cost efficient and scalable than private clouds. • Separate cloud providers team up to provide both private and public services as an integrated service • Individual cloud providers offer a complete hybrid package • Organizations who manage their private clouds themselves sign up to a public cloud service which they then integrate into their infrastructure Features of Hybrid Cloud ♣ Scalability ♣ Cost efficiencies ♣ Security ♣ Flexibility 2.4 Cloud Services Although a cloud is a remotely accessible environment, not all IT resources residing within a cloud can be made available for remote access. For example, a database or a physical server deployed within a cloud may only be accessible by other IT resources that are within the same cloud. A software

program with a published API may be deployed specifically to enable access by remote clients. Network Cloud Services What you may not have thought about is that every one of these consumer application cloud services uses network cloud services. In fact, the word “cloud” comes from the fact that many years ago those of us who built and sold client server applications, software and hardware used to draw a picture with the PC connected to a network and the network connected to a server. Since none of us actually understood how the network worked, we drew a cloud and labeled it “network” and left it at that. In those days companies built their own networks, but today consumers and businesses use network cloud services delivered by companies like AT&T, Verizon, Masergy and Sprint. Application Cloud Services So far we‟ve focused on consumer application cloud services, but for the past ten years the fastest-growing business applications have all been delivered as cloud services. Since 1999, fifteen companies that deliver business application cloud services have become public companies. Some of these companies have been acquisition targets. An informal analysis of forty of the Fortune 100 showed only two companies that did not have at least one of these applications running. Of course today, nearly all traditional application software companies like Oracle and JDA offer to manage their applications as a service.

Platform Cloud Services This brings us to the last group of cloud services. Platform cloud services are used by software developers to build new applications and by operations managers to manage their application, compute and storage cloud services. Horizontal platforms offer a great deal of flexibility, but if you know you want to leverage NetSuite‟s schema to build an MRP application, like Rootstock did, then choosing a particular vertical app can significantly speed the development and reduce the cost to build new applications. Platform cloud services also provide the operations management specialists with a range of services. Bandwidth Requirements If you are going to adopt the cloud framework, bandwidth and the potential bandwidth bottleneck must be evaluated in your strategy. Virtualization implementers found that the key bottleneck to virtual machine density is memory capacity; now there's a whole new slew of servers coming out with much larger memory footprints, removing memory as a system bottleneck. Cloud computing negates that bottleneck by removing the issue of machine density from the equation sorting that out becomes the responsibility of the cloud provider, freeing the cloud user from worrying about it. For cloud computing, bandwidth to and from the cloud provider is a bottleneck. A blade server is a server that has been optimized to minimize the use of physical space and energy. One of the huge advantages of the blade server for cloud computing use is bandwidth speed improvement. For example, the IBM BladeCenter is designed to accelerate the high-performance computing workloads both quickly and efficiently. Just as the memory issue had to be overcome to effectively alleviate the bottleneck of virtual high machine density, the bottleneck of cloud computing bandwidth must also be overcome, so look to the capabilities of your provider to determine if the bandwidth bottleneck will be a major performance issue. Advantages The pros of cloud computing are obvious and compelling. Do you really want them cluttering your expensive computers with their personal emails, illegally shared MP3 files, and naughty YouTube videos when you could leave that responsibility to someone else? Cloud computing allows you to buy in only the services you want, when you want them, cutting the upfront capital costs of computers and peripherals. You avoid equipment going out of date and other familiar IT problems like ensuring system security and reliability. You can add extra services at a moment's notice as your business needs change. It's really quick and easy to add new applications or services to your business without waiting weeks or months for the new computer (and its software) to arrive.

IV. PROBLEM DEFINITION

The existing system maintained by the cloud service providers, provides storage space for hosting data files in a pay-as you-go manner. However, the cloud is un-trusted since the cloud service providers are easily to become untrusted. Therefore, the cloud will try to learn the content of the stored data. Group manager takes charge of system parameters generation, user registration, and user revocation. In the existing applications, the group manager usually is the leader of the group. Therefore, the research assumes that the group manager is fully trusted by the other parties. Group members (users) are a set of registered users that will store their own data into the cloud and share them with others. In the scheme, the group membership is dynamically changed, due to the new user registration and user revocation. However, this existing scheme is not secure because of the weak protection of commitment in the phase of identity token issuance. The private keys of the other users do need to be recomputed and updated. In general, scheme cannot achieve secure key distribution, fine access control and secure user revocation in the dynamic cloud group environment.

V. AUTOMATIC CODING

1. Automatic coding via Bayesian classifier (Germany)

In a poster session at the Statistics Canada’s 2014 International Methodology Symposium, Bethmann et al. (of Intitut für Arbeitsmarkt-und Berufsforschung) have reported on research on applying two types of probabilistic supervised machine learning algorithms -- Naïve Bayes (NB) and conjugate Bayesian analysis based on multinomial distributions (BMN) -- for automatic occupation coding for German panel surveys. The authors used a large volume (approximately 300,000) of manually coded occupation text strings from recent surveys as training data. The rate of agreement between automatic coding and manual coding was used as a metric to evaluate the algorithms. Although both methods exhibited good agreement rates by common machine learning standards, the authors cautioned that they might not be sufficiently

satisfactory given the considerably higher accuracy requirements of occupation coding in production settings (the authors suggested a minimum agreement rate of 95%). On the other hand, the authors pointed out that when the target variable was changed to "social-economic status" or "occupational prestige" (more precisely, ISEI-08 and SIOPS-08 scores, both derived from occupation codes), both methods yielded dramatically improved results. The authors concluded that the current versions of their methods may be sufficient for production of socio-economic status or occupational prestige predictions, but further improvements are required for production of reliable occupation coding. Possibilities for improvement include the addition of a preprocessing step (to "clean up" input text strings, thereby reduce noise in training data), incorporation of a certain distance measure in the existing models, as well as different machine learning methods altogether (such as random forests or support vector machines). The authors project that their methods will be ready for release as an open-source R package in several years.

2. Automatic occupation coding via CASCOT (United Kingdom).

Computed-assisted Structured Coding Tool is an automatic occupation coding software tool developed by the Institute for Employment Research at the University of Warwick, a partner in the Eur-Occupations project. The objective of the project is to construct a publicly available database of the most frequent occupations to facilitate multi-country data collection. Since 2009, CASCOT has been able to perform automated coding into the ISCO'08 classification of occupational texts in any of the seven languages of the eight Eur-Occupations partner countries. CASCOT is available for online use for free and a desktop version is available for purchase should high-volume processing be required. However, CASCOT's underlying methodology has not been published.

3. Automatic coding via open-source indexing utility (Ireland)

The Central Statistics Office of Ireland has reported they are developing an automatic coding system for Classification of Individual Consumption by Purpose (COICOP) assignment for their Household Budget Survey, using previously coded records as training data. Their method is based on the open-source indexing and searching tool Apache Lucene (http://lucene.apache.org). 4. Automatic coding of census variables via Support Vector Machines (New Zealand)

Statistics New Zealand investigated the potential of using Support Vector Machines (SVM) to improve coding of item responses in their Census. They applied SVM to code the variables Occupation and Post-school Qualification, using two disjoint sets of observations, each of size 10,000, from Census 2013 data for training and testing. They reported 50% correctness rate on testing data for both variables, and concluded that further investigations would be necessary to further evaluate SVM as an automatic coding methodology.

VI. DJANGO:

Django is a Python-based free and open-source web framework that follows the model-template-views (MTV) architectural pattern. It is maintained by the Django Software Foundation (DSF), an . American independent organization established as anon profit.

Django's primary goal is to ease the creation of complex, database-driven websites. The framework emphasizes reusability and "pluggability" of components, less code, low coupling, rapid development, and the principle of don't repeat yourself.[11] Python is used throughout, even for settings, files, and data models. Django also provides an optional administrative create, read, update and delete interface that is generated dynamically through introspection and configured via admin models.

Django is a high-level Python Web framework that encourages rapid development and clean, pragmatic design. Built by experienced developers, it takes care of much of the hassle of Web development, so you can focus on writing your app without needing to reinvent the wheel. It's free and open source.

Ridiculously fast.

Django was designed to help developers take applications from concept to completion as quickly as possible.

Reassuringly secure.

Django takes security seriously and helps developers avoid many common security mistakes.

Exceedingly scalable.

Some of the busiest sites on the Web leverage Django's ability to quickly and flexibly scale.

With Django, you can take Web applications from concept to launch in a matter of hours. Django takes care of much of the hassle of Web development, so you can focus on writing your app without needing to reinvent the wheel. It's free and open source.

Django includes dozens of extras you can use to handle common Web development tasks. Django takes care of user authentication, content administration, site maps, RSS feeds, and many more tasks — right out of the box.

Because Django was developed in a fast-paced newsroom environment, it was designed to make common Web-development tasks fast and easy. Here's an informal overview of how to write a database-driven Web app with Django.

The goal of this document is to give you enough technical specifics to understand how Django works, but this isn't intended to be a tutorial or reference – but we've got both! When you're ready to start a project, you can start with the tutorial or dive right into more detailed documentation.

Although you can use Django without a database, it comes with an object-relational mapper in which you describe your database layout in Python code.

The data-model syntax offers many rich ways of representing your models – so far, it's been solving many years' worth of database-schema problems.

The model layer

Django provides an abstraction layer (the "models") for structuring and manipulating the data of your Web application. Learn more about it below:

- **Models:** Introduction to models | Field types | Indexes | Meta options | Model class
- **QuerySets:** Making queries | QuerySet method reference | Lookup expressions
- **Model instances:** Instance methods | Accessing related objects
- **Migrations:** Introduction to Migrations | Operations reference | SchemaEditor | Writing migrations
- **Advanced:** Managers | Raw SQL | Transactions | Aggregation | Search | Custom fields | Multiple databases | Custom lookups | Query Expressions | Conditional Expressions | Database Functions
- **Other:** Supported databases | Legacy databases | Providing initial data | Optimize database access | PostgreSQL specific features

The view layers

Django has the concept of "views" to encapsulate the logic responsible for processing a user's request and for returning the response. Find all you need to know about views via the links below:

- **The basics:** URLconfs | View functions | Shortcuts | Decorators | Asynchronous Support
- **Reference:** Built-in Views | Request/response objects | TemplateResponse objects
- **File uploads:** Overview | File objects | Storage API | Managing files | Custom storage
- **Class-based views:** Overview | Built-in display views | Built-in editing views | Using mixins | API reference | Flattened index
- **Advanced:** Generating CSV | Generating PDF
- **Middleware:** Overview | Built-in middleware classes

The template layers

The template layer provides a designer-friendly syntax for rendering the information to be presented to the user. Learn how this syntax can be used by designers and how it can be extended by programmers:

- **The basics:** Overview
- **For designers:** Language overview | Built-in tags and filters | Humanization
- **For programmers:** Template API | Custom tags and filters | Custom template backend

Forms

Django provides a rich framework to facilitate the creation of forms and the manipulation of form data.

- **The basics:** Overview | Form API | Built-in fields | Built-in widgets
- **Advanced:** Forms for models | Integrating media | Formsets | Customizing validation

The development processes

Learn about the various components and tools to help you in the development and testing of Django applications:

- **Settings:** Overview | Full list of settings
- **Applications:** Overview
- **Exceptions:** Overview
- **django-admin and manage.py:** Overview | Adding custom commands
- **Testing:** Introduction | Writing and running tests | Included testing tools | Advanced topics
- **Deployment:** Overview | WSGI servers | ASGI servers | Deploying static files | Tracking code errors by email | Deployment checklist

The admin

Find all you need to know about the automated admin interface, one of Django's most popular features:

- Admin site
- Admin actions
- Admin documentation generator

Security

Security is a topic of paramount importance in the development of Web applications and Django provides multiple protection tools and mechanisms:

- Security overview
- Disclosed security issues in Django
- Clickjacking protection
- Cross Site Request Forgery protection
- Cryptographic signing
- Security Middleware

Internationalization and localization

Django offers a robust internationalization and localization framework to assist you in the development of applications for multiple languages and world regions:

- Overview | Internationalization | Localization | Localized Web UI formatting and form input
- Time zones

Performance and optimization

There are a variety of techniques and tools that can help get your code running more efficiently - faster, and using fewer system resources.

- Performance and optimization overview

Geographic framework

GeoDjango intends to be a world-class geographic Web framework. Its goal is to make it as easy as possible to build GIS Web applications and harness the power of spatially enabled data.

Common Web application tools

Django offers multiple tools commonly needed in the development of Web applications:

- **Authentication:** Overview | Using the authentication system | Password management | Customizing authentication | API Reference
- Caching
- Logging
- Sending emails
- Syndication feeds (RSS/Atom)
- Pagination
- Messages framework
- Serialization
- Sessions
- Sitemaps
- Static files management
- Data validation

Other core functionalities

Learn about some other core functionalities of the Django framework:

- Conditional content processing
- Content types and generic relations
- Flatpages
- Redirects
- Signals
- System check framework
- The sites framework
- Unicode in Django

The Django open-source project

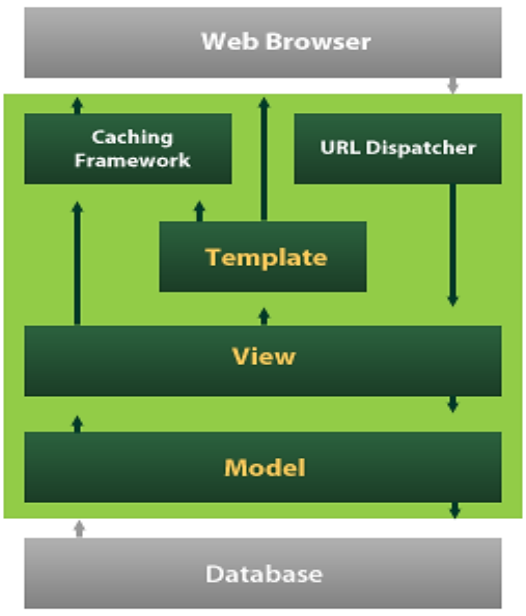
Learn about the development process for the Django project itself and about how you can contribute:

- **Community:** How to get involved | The release process | Team organization | The Django source code repository | Security policies | Mailing lists
- **Design philosophies:** Overview
- **Documentation:** About this documentation
- **Third-party distributions:** Overview
- **Django over time:** API stability | Release notes and upgrading instructions | Deprecation Timeline

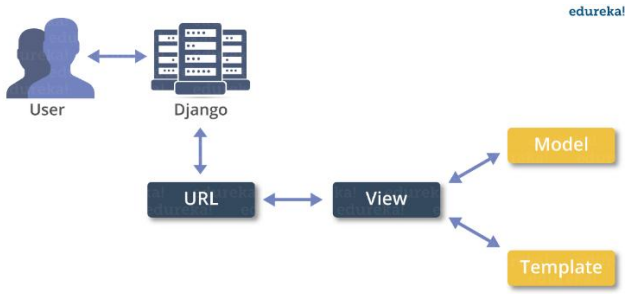
VII. DJANGO ENVIRONMENT

Django is a high-level Python Web framework that encourages rapid development and clean, pragmatic design. Built by experienced developers, it takes care of much of the hassle of Web development, so you can focus on writing your app without needing to reinvent the wheel. It's free and open source.

Django's primary goal is to ease the creation of complex, database-driven websites. Django emphasizes reusability and "pluggability" of components, rapid development, and the principle of don't repeat yourself. Python is used throughout, even for settings files and data models.



Django also provides an optional administrative create ,read ,update and delete interface that is generateddynamicallythroughintrospectionandconfiguredviaadminmodels.



VIII. EXISTING SYSTEM:

- Kallahalla et al presented a cryptographic storage system that enables secure data sharing on untrustworthy servers based on the techniques that dividing files into file groups and encrypting each file group with a file-block key.
- Yu et al exploited and combined techniques of key policy attribute-based encryption, proxy re-encryption and lazy re-encryption to achieve fine-grained data access control without disclosing data contents.

DISADVANTAGES OF EXISTING SYSTEM:

The file-block keys need to be updated and distributed for a user revocation; therefore, the system had a heavy key distribution overhead.

- The complexities of user participation and revocation in these schemes are linearly increasing with the number of data owners and the revoked users.
- The single-owner manner may hinder the implementation of applications, where any member in the group can use the cloud service to store and share data files with others.

IX. PROPOSED SYSTEM:

- In this paper, we propose a secure data sharing scheme, which can achieve secure key distribution and data sharing for dynamic group.
- We provide a secure way for key distribution without any secure communication channels. The users can securely obtain their private keys from group manager without any Certificate Authorities due to the verification for the public key of the user.
- Our scheme can achieve fine-grained access control, with the help of the group user list, any user in the group can use the source in the cloud and revoked users cannot access the cloud again after they are revoked.
- We propose a secure data sharing scheme which can be protected from collusion attack. The revoked users can not be able to get the original data files once they are revoked even if they conspire with the untrusted cloud. Our scheme can achieve secure user revocation with the help of polynomial function.
- Our scheme is able to support dynamic groups efficiently, when a new user joins in the group or a user is revoked from the group, the private keys of the other users do not need to be recomputed and updated.
- We provide security analysis to prove the security of our scheme.

ADVANTAGES OF PROPOSED SYSTEM:

- The computation cost is irrelevant to the number of revoked users in RBAC scheme. The reason is that no matter how many users are revoked, the operations for members to decrypt the data files almost remain the same.
- The cost is irrelevant to the number of the revoked users. The reason is that the computation cost of the cloud for file upload in our scheme consists of two verifications for signature, which is irrelevant to the number of the revoked users. The reason for the small computation cost of the cloud in the phase of file upload in RBAC scheme is that the verifications between communication entities are not concerned in this scheme.
- In our scheme, the users can securely obtain their private keys from group manager Certificate Authorities and secure communication channels. Also, our scheme is able to support dynamic groups efficiently, when a new user joins in the group or a user is revoked from the group, the private keys of the other users do not need to be recomputed and updated.

X. IMPLEMENTATION STATUS MODULES:

1. Member or User Module

2. Manager Module

3. Cloud or Admin Module

I. Member or User Module:

1. Every user needs to register with corresponding group for getting access permission using signature key.

2. The group admin consists of all the information such as vendor list and the list of revoked users. 3. The client that wants to register to the group requests to the admin. They can get access permission they can upload files to cloud. Members from same group can view the content of file over simultaneously they can download the file as well.

II. Manager Module:

1. Responsible for providing and denying access permission to the members of various groups.

2. Manager has the main access permission for maintaining the files over cloud. Manager can navigate through the group as well.

3. Manager can view the log details of activities carried on cloud file storage.

4. Manager achieve able to support dynamic groups efficiently, when a new user joins in the group or a user is revoked from the group, the private keys of the other users do not need to be recomputed and updated.

III.Cloud or Admin Module:

1. Responsible for providing and denying access activities related to manager module and user module.

2. Admin have the rights to maintain the all the permission.

3. Admin Can efficient user revocation can be achieved through a public revocation list without updating the private keys of the remaining users, and new users can directly decrypt.

XI. PROPOSED SYSTEM ARCHITECTURE

This system provides a very secure way for distributing the private keys without using secure communication channels. The users can get their private keys from group manager securely without any Certificate Authorities due to the verified for the public key of the user. As shown in the above fig.1. there are three actors in the architecture i.e. Group user, group manager and the group admin. The group admin consists of all the information such as vendor list and the list of revoked users. The client that wants to register to the group requests to the admin. After the registration the admin sends the admin secret key to its mail id. Then after the verification the client can upload or download the data. The files that are stored in the group are fragmented into blocks and those blocks are encrypted and then stored in the cloud. Previously, the data was encrypted completely and were not fragmented. This block encryption increases the security of the data. This process is during the uploading of a file. While downloading the data file, the blocks of the files are decrypted and then combined and given to the user to download the file. It uses two level security using OTP. In the first level is simply a text-based password and at the level 2, after the successful clearance of level 1, security system will generate a onetime password that would be valid for just one session. The authentic user will be informed by the OTP on its email id. System supports active groups efficiently, when a new user joins in the group or a user is deleted from the group, the private keys of the other needs to be recomputed and updated.

PROPOSEDMODULES:

1. **PRESCREENING**
2. **THREAT DETECTION**
3. **LIMIT RESOURCES**
4. **ANALYSIS**

1. PRESCREENING

Normally the screening process of the system can be done by login system but with this system username and password alone not enough to authenticate the system. The security questions will be set to each user separately in order to make sure the correct user logged in or not. It sets the limit the access of users from threats. The class can be limited by admin while registering and admin alone approve the user's entry to system.

2. THREAT DETECTION

The threat can be detected with the help of prescreening technique. Threats can be illegal access to system with more than five times trying to access the particular account with different act. The Insurance policies can be set to different users. According to policies users can be access. Within certain number of attempts goes wrong the user can be blocked and need to request admin to unblock again.

3. LIMIT RESOURCES

Admin is the authorized person to control polices and rules breaches. The wrong access of particular document more than certain number of time that is described in the policy can be blocked by admin and gets the intimation of breaches to admin. Then according to request by admin to user can be block or unblock the resources which are uploaded by admin/user.

4. ANALYSIS

The analysis of the system is done in this module. The proposed algorithm's efficiency is calculated here. The comparison of various factors can be handy to calculate and visualize in the graphs such as pie chart, bar chart, line chart. The data to plot the graph is taken from the system which is done.

INPUT DESIGN

The input design is the link between the information system and the user. It comprises the developing specification and procedures for data preparation and those steps are necessary to put transaction data in to a usable form for processing can be achieved by inspecting the computer to read data from a written or printed document or it can occur by having people keying the data directly into the system. The design of input focuses on controlling the amount of input required, controlling the errors, avoiding delay, avoiding extra steps and keeping the process simple. The input is designed in such a way so that it provides security and ease of use with retaining the privacy. Input Design considered the following things:

- What data should be given as input?
- How the data should be arranged or coded?
- The dialog to guide the operating personnel in providing input.
- Methods for preparing input validations and steps to follow when error occur.

OBJECTIVES

1.Input Design is the process of converting a user-oriented description of the input into a computer-based system. This design is important to avoid errors in the data input process

and show the correct direction to the management for getting correct information from the computerized system.

2.It is achieved by creating user-friendly screens for the data entry to handle large volume of data. The goal of designing input is to make data entry easier and to be free from errors. The data entry screen is designed in such a way that all the data manipulates can be performed. It also provides record viewing facilities.

3.When the data is entered it will check for its validity. Data can be entered with the help of screens. Appropriate messages are provided as when needed so that the user will not be in maize of instant. Thus, the objective of input design is to create an input layout that is easy to follow

OUTPUT DESIGN

A quality output is one, which meets the requirements of the end user and presents the information clearly. In any system results of processing are communicated to the users and to other system through outputs. In output design it is determined how the information is to be displaced for immediate need and also the hard copy output. It is the most important and direct source information to the user. Efficient and intelligent output design improves the system's relationship to help user decision-making.

1. Designing computer output should proceed in an organized, well thought out manner; the right output must be developed while ensuring that each output element is designed so that people will find the system can use easily and effectively. When analysis design computer output, they should Identify the specific output that is needed to meet the requirements.

2.Select methods for presenting information.

3.Create document, report, or other formats that contain information produced by the system.

The output form of an information system should accomplish one or more of the following objectives.

- Convey information about past activities, current status or projections of the
- Future.
- Signal important events, opportunities, problems, or warnings.
- Trigger an action.
- Confirm an action

XII. RESULTS

Unit testing

Unit testing involves the design of test cases that validate that the internal program logic is functioning properly, and that program inputs produce valid outputs. All decision branches and internal code flow should be validated. It is the testing of individual software units of the application.it is done after the completion of an individual unit before integration. This is a structural testing, that relies on knowledge of its construction and is invasive. Unit tests perform basic tests at component level and test a specific business process, application, and/or system configuration. Unit tests ensure that each unique path of a business process performs accurately to the documented specifications and contains clearly defined inputs and expected results.

Integration testing

Integration tests are designed to test integrated software components to determine if they actually run as one program. Testing is event driven and is more concerned with the basic outcome of screens or fields. Integration tests demonstrate that although the components were individually satisfaction, as shown by successfully unit testing, the combination of components is correct and consistent. Integration testing is specifically aimed at exposing the problems that arise from the combination of components.

Functional test

Functional tests provide systematic demonstrations that functions tested are available as specified by the business and technical requirements, system documentation, and user manuals.

Functional testing is centered on the following items:

Valid Input: identified classes of valid input must be accepted.

Invalid Input: identified classes of invalid input must be rejected.

Functions: identified functions must be exercised.

Output: identified classes of application outputs must be exercised.

Systems/Procedures: interfacing systems or procedures must be invoked.

Organization and preparation of functional tests is focused on requirements, key functions, or special test cases. In addition, systematic coverage pertaining to identify Business process flows; data fields, predefined processes, and successive processes must be considered for testing. Before functional testing is complete, additional tests are identified and the effective value of current tests is determined.

System Test

System testing ensures that the entire integrated software system meets requirements. It tests a configuration to ensure known and predictable results. An example of system testing is the configuration-oriented system integration test. System testing is based on process descriptions and flows, emphasizing pre-driven process links and integration points.

White Box Testing

White Box Testing is a testing in which in which the software tester has knowledge of the inner workings, structure and language of the software, or at least its purpose. It is purpose. It is used to test areas that cannot be reached from a black box level.

Black Box Testing

Black Box Testing is testing the software without any knowledge of the inner workings, structure or language of the module being tested. Black box tests, as most other kinds of tests, must be written from a definitive source document, such as specification or requirements document, such as specification or requirements document. It is a testing in which the software under test is treated, as a black box. you cannot "see" into it. The test provides inputs and responds to outputs without considering how the software works.

Unit Testing

Unit testing is usually conducted as part of a combined code and unit test phase of the software lifecycle, although it is not uncommon for coding and unit testing to be conducted as two distinct phases.

Test strategy and approach

Field testing will be performed manually and functional tests will be written in detail.

Test objectives

- All field entries must work properly.
- Pages must be activated from the identified link.
- The entry screen, messages and responses must not be delayed.

Features to be tested

- Verify that the entries are of the correct format
- No duplicate entries should be allowed
- All links should take the user to the correct page.

Integration Testing

Software integration testing is the incremental integration testing of two or more integrated software components on a single platform to produce failures caused by interface defects.

The task of the integration test is to check that components or software applications, e.g. components in a software system or – one step up – software applications at the company level – interact without error.

Test Results: All the test cases mentioned above passed successfully. No defects encountered.

Acceptance Testing

User Acceptance Testing is a critical phase of any project and requires significant participation by the end user. It also ensures that the system meets the functional requirements.

Test Results: All the test cases mentioned above passed successfully. No defects encountered.

XIII. CONCLUSION:

We studied the problem of designing cyber insurance contracts by a single profit-maximizing insurer, for both risk-neutral and risk-averse agents. While the introduction of insurance worsens network security in a network of independent agents, we showed that the result could be different in a network of interdependent agents. Specifically, we showed that security interdependency leads to a profit opportunity for the insurer, created by the inefficient effort levels exerted by free-riding agents when insurance is not available but interdependency is present; this is in addition to risk transfer that an insurer typically profits from. We showed that security prescreening then allows the insurer to take advantage of this additional profit opportunity by designing the right contracts to incentivize the agents to increase their effort levels and essentially selling commitment to interdependent agents. We show under what conditions this type of contracts leads to not only increased profit for the principal and utility for the agents, but also improved state of network security. The Information sharing on un-trusted servers is planned to use alternative schemes. But there are challenges for the user involvement and revocation in the schemes. The quantity of information about the owners and the revoked users are increasing progressively. The cloud with an Anti-Collusion Information Sharing Scheme for dynamic companies had secured private keys for the users, obtained from the team managers through certified authorities and secured communication channels. When a new user is registers or a user is revoked from the group, the scheme is equipped to support powerful companies by providing secured private keys, which are not required to be recomputed or updated in this process. The scheme also protects the data effectively, when a revoked user cannot retrieve the data even if they try to process using an un-trusted cloud, as a result this scheme handles revoked user at ease.

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DLAU: A Scalable Deep Learning Accelerator Unit on FPGA

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I. INTRODUCTION

1.1 Introduction to FPGA:

In the past few years, machine learning has become pervasive in various research fields and commercial applications, and achieved satisfactory products. The emergence of deep learning speeded up the development of machine learning and artificial intelligence. Consequently, deep learning has become a research hot spot in research organizations [1]. In general, deep learning uses a multilayer neural network model to extract high-level features which are a combination of low-level abstractions to find the distributed data features, in order to solve complex problems in machine learning. Currently, the most widely used neural models of deep learning are deep neural networks (DNNs) [2] and convolution neural networks (CNNs) [3], which have been proved to have excellent capability in solving picture recognition, voice recognition, and other complex machine learning tasks.

However, with the increasing accuracy requirements and complexity for the practical applications, the size of the neural networks becomes explosively large scale, such as the Baidu Brain with 100 billion neuronal connections, and the Google cat-recognizing system with one billion neuronal connections. The explosive volume of data makes the data centers quite power consuming. In particular, the electricity consumption of data centers in U.S. are projected to increase to roughly 140 billion kilowatt-hours annually by 2020 [4]. Therefore, it poses significant challenges to implement high performance deep learning networks with low power cost, especially for large-scale deep learning neural network models. So far, the state-of-the-art means for accelerating deep learning algorithms are field-programmable gate array (FPGA), application specific integrated circuit (ASIC), and graphic processing unit (GPU). They created dedicated hardware processing cores which are optimized for the RBM algorithm. Similarly, Kim et al. [7] also developed an FPGA-based accelerator for the RBM. They use multiple RBM processing modules in parallel, with each module responsible for a relatively small number of nodes. Other similar works also present FPGA-based neural network accelerators [9]. Yu et al. [8] presented an FPGA-based accelerator, but it cannot accommodate changing network size and network topologies. To sum up, these studies focus on implementing a particular deep learning algorithm efficiently, but how to increase the size of the neural networks with scalable and flexible hardware architecture has not been properly solved.

To tackle these problems, we present a scalable deep learning accelerator unit named DLAU to speed up the kernel computational parts of deep learning algorithms. In particular, we utilize the tile techniques, FIFO buffers, and pipelines to minimize memory transfer operations, and reuse the computing units to implement the largesize neural networks. This approach distinguishes itself from previous literatures with following contributions

1. In order to explore the locality of the deep learning application, we employ tile techniques to partition the large scale input data. The DLAU architecture can be configured to operate different sizes of tile data to leverage the tradeoffs between speedup and hardware costs. Consequently, the FPGA-based accelerator is more scalable to accommodate different machine learning applications
2. The DLAU accelerator is composed of three fully pipelined processing units, including tiled matrix multiplication unit (TMMU), part sum accumulation unit (PSAU), and activation function acceleration unit (AFAU). Different network topologies such as CNN, DNN, or even emerging neural networks can be composed from these basic modules. Consequently, the scalability of FPGA-based accelerator is higher than ASIC-based accelerator.

1.2 Introduction to VLSI:

Large-scale combination (VLSI) is the procedure of combining so as to make coordinated circuits a huge number of transistor-based circuits into a solitary chip. VLSI started in the 1970s when complex semiconductor and correspondence advancements were being produced. The chip is a VLSI gadget. The term is no more as normal as it once seemed to be, as chips have expanded in multifaceted nature into the countless transistors.

1.2.1 Overview:

The principal semiconductor chips held one transistor each. Ensuing advances included more transistors, and, as a result, more individual capacities or frameworks were incorporated after some time. The initially incorporated circuits held just a couple of gadgets, maybe upwards of ten

diodes, transistors, resistors and capacitors, making it conceivable to manufacture one or more rationale doors on a solitary gadget. Presently referred to reflectively as "little scale joining" (SSI), upgrades in procedure prompted gadgets with several rationale entryways, known as huge scale incorporation (LSI), i.e. frameworks with no less than a thousand rationale doors. Current technology has moved far past this imprint and today's chip have numerous a large number of entryways and countless individual transistors.

At one time, there was a push to name and adjust different levels of huge scale joining above VLSI. Terms like Ultra-substantial scale Integration (ULSI) were utilized. In any case, the gigantic number of entryways and transistors accessible on regular gadgets has rendered such fine refinements debatable.

Terms recommending more prominent than VLSI levels of combination are no more in boundless use. Indeed, even VLSI is presently to some degree interesting, given the regular suspicion that all chip are VLSI or better.

Starting mid 2008, billion-transistor processors are economically accessible, an illustration of which is Intel's Montecito Itanium chip. This is relied upon to wind up more typical as semiconductor manufacture moves from the present era of 65 nm procedures to the following 45 nm eras (while encountering new difficulties, for example, expanded variety crosswise over procedure corners). Another outstanding case is NVIDIA's 280 arrangement GPU.

This microchip is one of a kind in the way that its 1.4 Billion transistor check, equipped for a teraflop of execution, is totally devoted to rationale (Itanium's transistor tally is to a great extent because of the 24MB L3 store). Current plans, rather than the most punctual gadgets, use broad outline mechanization and computerized rationale combination to lay out the transistors, empowering more elevated amounts of unpredictability in the subsequent rationale usefulness. Certain elite rationale pieces like the SRAM cell, on the other hand, are still composed by hand to guarantee the most noteworthy proficiency (some of the time by bowing or breaking set up outline standards to acquire the last piece of execution by exchanging security).

1.2.2 What is VLSI?

VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas.

VLSI

- Simply we say Integrated circuit is many transistors on one chip.
- Design/manufacturing of extremely small, complex circuitry using modified semiconductor material
- Integrated circuit (IC) may contain millions of transistors, each a few mm in size
- Applications wide ranging: most electronic logic devices

1.2.3 History of Scale Integration:

- late 40s Transistor invented at Bell Labs
- late 50s First IC (JK-FF by Jack Kilby at TI)
- early 60s Small Scale Integration (SSI)
  - 10s of transistors on a chip
- late 60s Medium Scale Integration (MSI)
  - 100s of transistors on a chip
- early 70s Large Scale Integration (LSI)
  - 1000s of transistor on a chip
- early 80s VLSI 10,000s of transistors on a
  - chip (later 100,000s & now 1,000,000s)
- Ultra LSI is sometimes used for 1,000,000s
  - SSI - Small-Scale Integration (0-102)
  - MSI - Medium-Scale Integration (102-103)
  - LSI - Large-Scale Integration (103-105)
  - VLSI - Very Large-Scale Integration (105-107)
  - ULSI - Ultra Large-Scale Integration (>=107)

1.2.4 Advantages of ICs over discrete components:

While we will concentrate on integrated circuits , the properties of integrated circuits-what we can and cannot efficiently put in an integrated circuit-largely determine the architecture of the entire system. Integrated circuits improve system characteristics in several critical ways. ICs have three key advantages over digital circuits built from discrete components:

- Size. Integrated circuits are much smaller-both transistors and wires are shrunk to micrometer sizes, compared to the millimeter or centimeter scales of discrete components. Small size leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances.
- Speed. Signals can be switched between logic 0 and logic 1 much quicker within a chip than they can between chips. Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board. The high speed of circuits on-chip is due to their small size-smaller components and wires have smaller parasitic capacitances to slow down the signal.
- Power consumption. Logic operations within a chip also take much less power. Once again, lower power consumption is largely due to the small size of circuits on the chip-smaller parasitic capacitances and resistances require less power to drive them.

1.2.5 VLSI and systems:

These advantages of integrated circuits translate into advantages at the system level:

- Smaller physical size. Smallness is often an advantage in itself-consider portable televisions or handheld cellular telephones.
- Lower power consumption. Replacing a handful of standard parts with a single chip reduces total power consumption. Reducing power consumption has a ripple effect on the rest of the system: a smaller, cheaper power supply can be used; since less power consumption means less heat, a fan may no longer be necessary; a simpler cabinet with less shielding for electromagnetic shielding may be feasible, too.
- Reduced cost. Reducing the number of components, the power supply requirements, cabinet costs, and so on, will inevitably reduce system cost. The ripple effect of integration is such that the cost of a system built from custom ICs can be less, even though the individual ICs cost more than the standard parts they replace.

Understanding why integrated circuit technology has such profound influence on the design of digital systems requires understanding both the technology of IC manufacturing and the economics of ICs and digital systems.

Applications

- Electronic system in cars.
- Digital electronics control VCRs
- Transaction processing system, ATM
- Personal computers and Workstations
- Medical electronic systems.
- Etc….

1.2.6 Applications of VLSI:

Electronic systems now perform a wide variety of tasks in daily life. Electronic systems in some cases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics are usually smaller, more flexible, and easier to service. In other cases electronic systems have created totally new applications. Electronic systems perform a variety of tasks, some of them visible, some more hidden:

- Personal entertainment systems such as portable MP3 players and DVD players perform sophisticated algorithms with remarkably little energy.
- Electronic systems in cars operate stereo systems and displays; they also control fuel injection systems, adjust suspensions to varying terrain, and perform the control functions required for anti-lock braking (ABS) systems.
- Digital electronics compress and decompress video, even at high-definition data rates, on-the-fly in consumer electronics.
- Low-cost terminals for Web browsing still require sophisticated electronics, despite their dedicated function.
- Personal computers and workstations provide word-processing, financial analysis, and games. Computers include both central processing units (CPUs) and special-purpose hardware for disk access, faster screen display, etc.
- Medical electronic systems measure bodily functions and perform complex processing algorithms to warn about unusual conditions. The availability of these complex systems, far from overwhelming consumers, only creates demand for even more complex systems.

The growing sophistication of applications continually pushes the design and manufacturing of integrated circuits and electronic systems to new levels of complexity. And perhaps the most amazing characteristic of this collection of systems is its variety-as systems become more complex, we build not a few general-purpose computers but an ever wider range of special-purpose systems. Our ability to do so is a testament to our growing mastery of both integrated circuit manufacturing and design, but the increasing demands of customers continue to test the limits of design and manufacturing

1.2.7 ASIC:

An Application-Specific Integrated Circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. For example, a chip designed solely to run a cell phone is an ASIC. Intermediate between ASICs and industry standard integrated circuits, like the 7400 or the 4000 series, are application specific standard products (ASSPs).

As feature sizes have shrunk and design tools improved over the years, the maximum complexity (and hence functionality) possible in an ASIC has grown from 5,000 gates to over 100 million. Modern ASICs often include entire 32-bit processors, memory blocks including ROM, RAM, EEPROM, Flash and other large building blocks. Such an ASIC is often termed a SoC (system-on-a-chip). Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

Field-programmable gate arrays (FPGA) are the modern-day technology for building a breadboard or prototype from standard parts; programmable logic blocks and programmable interconnects allow the same FPGA to be used in many different applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design even in production.

- An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use.
- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC

- Structured ASIC's are used mainly for mid-volume level design. The design task for structured ASIC's is to map the circuit into a fixed arrangement of known cells.

II. LITERATURE SURVEY

Deng, Li,Gong [1]: survey describe that deep learning is becoming a mainstream technology for speech recognition at industrial scale. In this paper, we provide an overview of the work by Microsoft speech researchers since 2009 in this area focusing on more recent advances which shed light to the basic capabilities and limitations of the current deep learning technology. We organize this view along with feature-domain and model-domain dimensions according to the conventional approach to analyzing speech systems. Selected experiments results, including speech recognition and related applications such as spoken dialogue and language modeling are presented to demonstrate and analyze the strengths and weakness of the techniques described in the paper.

Deng, Platt[2]: survey presents that deep learning systems have dramatically improved the accuracy of speech recognition and various deep architectures and learning techniques have been developed with distinct strengths and weaknesses in recent years. How can ensemble learning be applied to the various deep learning systems to achieve greater recognition accuracy is the focus of this paper. We develop and report linear stacking methods for ensembling learning with applications specifically to speech-class and long-linear stacking methods for ensemble learning with applications connected deep neural networks.

Gravier, Garg[3,10] : survey presents Visual speech information from the speaker‟s moth region has been successfully shown to improve noise robustness of automatic speech recognizers , thus promising to extend their usability into the uman computer interface. In this paper, we review the main components of audio-visual automatic speech recognition and present novel contributions in two main areas: first, the visual front end design and later, we discuss new work on features and design fusion combination , the modeling of audio-visual speech asynchrony and incorporating modality reliability estimates to the bimodal recognition process.

Das[4]: presents a brief survey on speech is the primary and the most convenient means of communication between people. The communication among human computer interaction is called human computer interface. Speech has potential of being important mode of interaction with computer. This paper gives an overview of major technological perspective and appreciation of the fundamental progress of speech recognition and also gives overview technique developed in each stage of speech recognition. This paper helps in choosing the technique along with their relative merits and demerits. A comparative study of different techniques is done. This paper concludes with the decision on feature direction for developing technique in human computer interface system in different mother tongue and it also gives the various technique used in each step of a speech recognition process and attempts to analyze an approach for designing an efficient system for speech recognition . The objective of this review paper is to summarize and compare different speech recognition systems and identify research topics and applications where are at the front end of this exciting and challenging field.

Dhameliya, Desai[7,8]: survey presents speech is the most natural form of human communication and speech processing has been one of the most inspiring expanses of signal processing . Speech recognition is the process of automatically recognizing the spoken words of person based on information in speech signal. Automatic Speech Recognition(ASR) system takes a human speech utterances as an input and requires a string of words as output. This paper introduces a brief survey on Automatic Speech Recognition and discusses the major subjects and improvements made in the past 60 years of research , that provides technological outlook and a respect of fundamental achievements that have been accomplished in the important areas of speech recognition. Definition of various types of speech classes , feature extraction techniques, speech classifiers and performance evaluation are issues that require attention in designing of speech recognition system. The objective of this review paper is to summarize some of the well-known methods used in several stages of speech recognition system.

Gaikwad, Gawali and Yannawar [6,9] : The speech is most prominent and primary mode of communication among human beings. The communication among human computer interaction is called human computer interface. Speech has potential of being important mode of interaction with computer. This paper gives an overview of major technological perspective and appreciation of fundamental progress of speech recognition and also gives an overview technique developed in each stage of speech recognition. This paper helps in choosing the technique along with their merits and demerits. A comparative study of different techniques is done. This paper concludes with the decision on feature direction for developing technique in human computer interface system in Marathi language. Therese, Lingam [5,11]: Says that speech has evolved as a primary form of communication between humans. The advent of digital technology gave us highly versatile digital processors with high speed, low cost and high power, which enable researchers to transform the analog speech signals into digital speech signals that can be significantly studied. Achieving higher recognition accuracy, low word error rate and addressing the issue of resources of variability are the major consideration for developing an effective automatic Speech Recognition System. . In speech recognition, feature extraction requires much attention because recognition performance depends heavily on this phase. In this paper, an effort has been made to highlight the progress made so far in the feature extraction phase of spec recognition system and an overview of technological

perspective of Automatic Speech Recognition System is discussed.

Deep learning algorithms

Restricted Boltzmann Machines

In RBMs, the gradient used in training is an approximation formed by a taking small number of Gibbs sampling steps. Given the biased nature of the gradient and intractability of the objective function, it is difficult to use any optimization methods other than plain SGDs.

Auto encoders and denoising auto encoders

Here, we use the L2 norm to penalize the difference between the reconstruction and the input. Typically, we set the activation function _ to be the sigmoid or hyperbolic tangent function. Unlike RBMs, the gradient of the auto encoder objective can be computed exactly and this gives rise to an opportunity to use more advanced optimization methods, such as L-BFGS and CG, to train the networks.

Sparse RBMs and Auto encoders

Sparsity regularization typically leads to more interpretable features that perform well for classification. Sparse coding was first proposed by (Olshausen & Field, 1996) as a model of simple cells in the visual cortex. The key idea in this approach is to penalize the deviation between the expected value of the hidden representations and preferred target activation _. By setting _ to be close to zero, the hidden unit will be sparsely activated. Sparse representations have been employed successfully in many applications such as object recognition, speech recognition and activity recognition.

A common practice to train sparse RBMs is to use a running estimate and penalizing only the bias. This further complicates the optimization procedure and makes it hard to debug the learning algorithm. Moreover, it is important to tune the learning rates correctly for the different parameters W, b and c. Consequently, it can be difficult to train sparse RBMs.

In our experience, it is often faster and simpler to obtain sparse representations via auto encoders with the proposed sparsity penalties, especially when batch or large mini batch optimization methods are used.

In detail, we consider sparse auto encoders with a target activation of _ and penalize it using the KL divergence. To train sparse auto encoders, we need to estimate the expected activation value for each hidden unit. However, we will not be able to compute this statistic unless we run the optimization method in batch mode. In practice, if we have a small dataset, it is better to use a batch method to train a sparse auto encoder because we do not have to tweak optimization parameters, such as mini batch size, _ as described below.

Tiled and locally connected networks

RBMs and auto encoders have densely-connected network architectures which do not scale well to large images. For large images, the most common approach is to use convolutional neural networks. Convolutional neural networks have local receptive field architectures: each hidden unit can only connect to a small region of the image. Translational invariance is usually hardwired by weight tying. Recent approaches try to relax this constraint.

It shows that local architectures, such as tiled convolutional or convolutional architectures, can be efficiently trained with a computer cluster using the MapReduce framework. With local architectures, the cost of communicating the gradient over the network is often smaller than the cost of computing it (e.g., cases considered in the experiments).

III. PROJECT DESCRIPTION

The large-scale DNNs include iterative computations which have few conditional branch operations, therefore, they are suitable for parallel optimization in hardware. In this paper, we first explore the hot spot using the profiler. Results in Fig. 1 illustrates the percentage of running time including matrix multiplication (MM), activation, and vector operations. For the representative three key operations: 1) feed forward; 2) RBM; and 3) BP, MM play a significant role of the overall execution. In particular, it takes 98.6%, 98.2%, and 99.1% of the feed forward, RBM, and BP operations. In comparison, the activation function only takes 1.40%, 1.48%, and 0.42% of the three operations. Experimental results on profiling demonstrate that the design and implementation of MM accelerators is able to improve the overall speedup of the system significantly

However, considerable memory bandwidth and computing resources are needed to support the parallel processing, consequently it poses a significant challenge to FPGA implementations compared with GPU and CPU optimization measures. In order to tackle the problem, in this paper we employ tile techniques to partition the massive input data set into tiled subsets. Each designed hardware accelerator is able to buffer the tiled subset of data for processing. In order to support the large-scale neural networks, the accelerator architecture are reused. Moreover, the data access for each tiled subset can run in parallel to the computation of the hardware accelerators.

In particular, for each iteration, output neurons are reused as the input neurons in next iteration. To generate the output neurons for each iteration, we need to multiply the input neurons by each column in weights matrix. As illustrated in Algorithm 1, the input data are partitioned into tiles and then multiplied by the corresponding weights. Thereafter the calculated part sum are accumulated to get the result. Besides the input/output neurons, we also divided the weight matrix into tiles corresponding to the tile size. As a consequence, the hardware cost of the accelerator only depends on the tile size, which saves significant number of hardware resources. The tiled technique is able to solve the problem by implementing large networks with limited hardware. Moreover, the pipelined hardware implementation is another advantage of FPGA technology compared to GPU architecture, which uses massive parallel

SIMD architectures to improve the overall performance and throughput. According to the profiling results depicted in Table I, during the prediction process and the training process in deep learning algorithms, the common but important computational parts are MM and activation functions, consequently in this paper we implement the specialized accelerator to speed up the MM and activation functions.

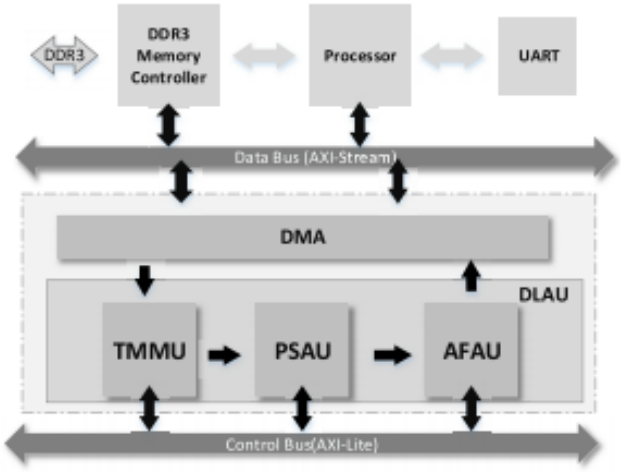

Fig. 1. DLAU accelerator architecture

Fig. 1 describes the DLAU system architecture which contains an embedded processor, a DDR3 memory controller, a DMA module, and the DLAU accelerator. The embedded processor is responsible for providing programming interface to the users and communicating with DLAU via JTAG-UART. In particular it transfers the input data and the weight matrix to internal BRAM blocks, activates the DLAU accelerator, and returns the results to the user after execution. The DLAU is integrated as a standalone unit which is flexible and adaptive to accommodate different applications with configurations. The DLAU consists of three processing units organized in a pipeline manner: 1) TMMU; 2) PSAU; and 3) AFAU. For execution, DLAU reads the tiled data from the memory by DMA, computes with all the three processing units in turn, and then writes the results back to the memory.

In particular, the DLAU accelerator architecture has the following key features.

FIFO Buffer: Each processing unit in DLAU has an input buffer and an output buffer to receive or send the data in FIFO. These buffers are employed to prevent the data loss caused by the inconsistent throughput between each processing unit.

Tiled Techniques: Different machine learning applications may require specific neural network sizes. The tile technique is employed to divide the large volume of data into small tiles that can be cached on chip, therefore the accelerator can be adopted to different neural network size. Consequently, the FPGA-based accelerator is more scalable to accommodate different machine learning applications.

Pipeline Accelerator: We use stream-like data passing mechanism (e.g., AXI-Stream for demonstration) to transfer data between the adjacent processing units, therefore, TMMU, PSAU, and AFAU can compute in streaming-like manner. Of these three computational modules, TMMU is the primary computational unit, which reads the total weights and tiled nodes data through DMA, performs the calculations, and then transfers the intermediate part sum results to PSAU. PSAU collects part sums and performs accumulation. When the accumulation is completed, results will be passed to AFAU. AFAU performs the activation function using piecewise linear interpolation methods. In the rest of this section, we will detail the implementation of these three processing units, respectively

TMMU Architecture

TMMU is in charge of multiplication and accumulation operations. TMMU is specially designed to exploit the data locality of the weights and is responsible for calculating the part sums. TMMU employs an input FIFO buffer which receives the data transferred from DMA and an output FIFO buffer to send part sums to PSAU. Fig. 2 illustrates the TMMU schematic diagram, in which we set tile size = 32 as an example. TMMU first reads the weight matrix data from input buffer into different BRAMs in 32 by the row number of the weight matrix (n = i%32 where n refers to the number of BRAM, and i is the row number of weight matrix). Then, TMMU begins to buffer the tiled node data. In the first time, TMMU reads the tiled 32 values to registers Reg_a and starts execution. In parallel to the computation at every cycle, TMMU reads the next node from input buffer and saves to the registers Reg_b. Consequently, the registers Reg_a and Reg_b can be used alternately

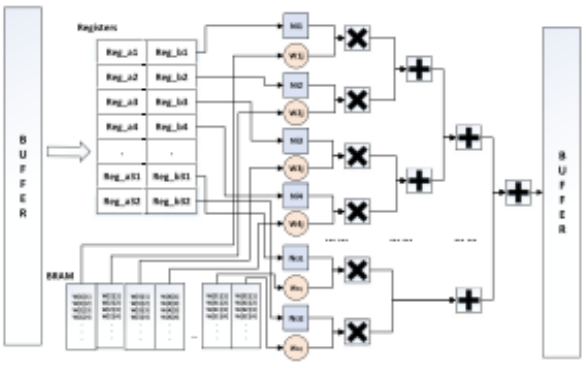

Fig. 2. TMMU schematic

For the calculation, we use pipelined binary adder tree structure to optimize the performance. As depicted in Fig. 2, the weight data and the node data are saved in BRAMs and registers. The pipeline takes advantage of time-sharing the coarse-grained accelerators. As a consequence, this implementation enables the TMMU unit to produce a part sum result every clock cycle.

PSAU Architecture

PSAU is responsible for the accumulation operation. Fig. 3 presents the PSAU architecture, which accumulates the part sum produced by TMMU. If the part sum is the final result, PSAU will write the value to output buffer and send results to AFAU in a pipeline manner. PSAU can accumulate one part sum every clock cycle, therefore the throughput of PSAU accumulation matches the generation of the part sum in TMMU.

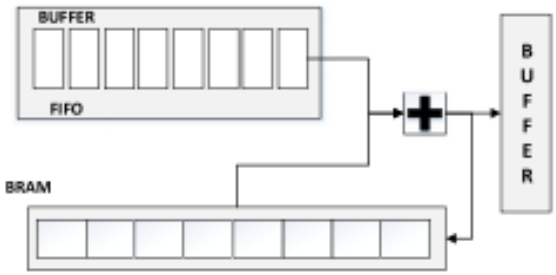

Fig. 3. PSAU schematic.

AFAU Architecture

Finally, AFAU implements the activation function using piecewise linear interpolation ($y = ai * x + bi$, $x \in [x1, xi+1]$). This method has been widely applied to implement activation functions with negligible accuracy loss when the interval between xi and xi+1 is insignifi- cant. Equation (1) shows the implementation of sigmoid function. For $x > 8$ and $x \leq -8$, the results are sufficiently close to the bounds of 1 and 0, respectively. For the cases in $-8 < x \leq 0$ and $0 < x \leq 8$, different functions are configured. In total, we divide the sigmoid function into four segments. Similar to PSAU, AFAU also has both input buffer and output buffer to maintain the throughput with other processing units. In particular, we use two separate BRAMs to store the values of a and b. The computation of AFAU is pipelined to operate sigmoid function every clock cycle. As a consequence, all the three processing units are fully pipelined to ensure the peak throughput of the DLAU accelerator architecture.

IV. TOOLS XILINX

4.1 Migrating Projects from Previous ISE Software Releases:

When you open a project file from a previous release, the ISE® software prompts you to migrate your project. If you click Backup and Migrate or Migrate Only, the software automatically converts your project file to the current release. If you click Cancel, the software does not convert your project and, instead, opens Project Navigator with no project loaded.

Note: After you convert your project, you cannot open it in previous versions of the ISE software, such as the ISE 11 software. However, you can optionally create a backup of the original project as part of project migration, as described below.

To Migrate a Project

1. In the ISE 12 Project Navigator, select **File > Open Project**.
2. In the Open Project dialog box, select the .xise file to migrate.

Note You may need to change the extension in the Files of type field to display .npl (ISE 5 and ISE 6 software) or .ise (ISE 7 through ISE 10 software) project files.

3. In the dialog box that appears, select **Backup and Migrate** or **Migrate Only**.
4. The ISE software automatically converts your project to an ISE 12 project.

Note If you chose to Backup and Migrate, a backup of the original project is created at project_name_ise12migration.zip.

5. Implement the design using the new version of the software.

Note Implementation status is not maintained after migration.

4.2 Properties:

For information on properties that have changed in the ISE 12 software, see ISE 11 to ISE 12 Properties Conversion.

4.3 IP Modules:

If your design includes IP modules that were created using CORE Generator™ software or Xilinx® Platform Studio (XPS) and you need to modify these modules, you may be required to update the core. However, if the core netlist is present and you do not need to modify the core, updates are not required and the existing netlist is used during implementation.

4.4 Obsolete Source File Types:

The ISE 12 programming backings the greater part of the source sorts that were upheld in the ISE 11 programming.

On the off chance that you are working with undertakings from past discharges, state graph source documents (.dia), ABEL source records (.abl), and test seat waveform source documents (.tbw) are no more upheld. For state outline and ABEL source records, the product discovers a related HDL document and adds it to the task, if conceivable. For test seat waveform documents, the product consequently changes over the TBW record to a HDL test seat and adds it to the venture. To change over a TBW record after task relocation, see Converting a TBW File to a HDL Test Bench.

4.5 Using ISE Example Projects:

To help familiarize you with the ISE® software and with FPGA and CPLD designs, a set of example designs is provided with Project Navigator. The examples show different design techniques and source types, such as

VHDL, Verilog, schematic, or EDIF, and include different constraints and IP.

To Open an Example

1. Select **File > Open Example**.
2. In the Open Example dialog box, select the Sample Project Name.

Note To help you choose an example project, the Project Description field describes each project. In addition, you can scroll to the right to see additional fields, which provide details about the project.

3. In the Destination Directory field, enter a directory name or browse to the directory.
4. Click **OK**.

The example project is extracted to the directory you specified in the Destination Directory field and is automatically opened in Project Navigator. You can then run processes on the example project and save any changes.

Note If you modified an example project and want to overwrite it with the original example project, select **File > Open Example**, select the Sample Project Name, and specify the same Destination Directory you originally used. In the dialog box that appears, select **Overwrite the existing project** and click **OK**.

4.6 Creating a Project:

Venture Navigator permits you to deal with your FPGA and CPLD plans utilizing an ISE® venture, which contains all the source records and settings particular to your outline. To begin with, you must make a task and after that, include source documents, and set procedure properties. After you make an undertaking, you can run procedures to execute, compel, and break down your configuration. Venture Navigator gives a wizard to offer you some assistance with creating an undertaking as takes after.

Note If you incline toward, you can make an undertaking utilizing the New Project dialog box rather than the New Project Wizard. To utilize the New Project dialog box, deselect the Use New Project wizard alternative in the ISE General page of the Preferences dialog box

To Create a Project

1. Select **File > New Project** to launch the New Project Wizard.
2. In the **Create New Project page,** set the name, location, and project type, and click **Next**.
3. For EDIF or NGC/NGO projects only: In the **Import EDIF/NGC Project page**, select the input and constraint file for the project, and click **Next**.
4. In the **Project Settings page**, set the device and project properties, and click **Next**.
5. In the **Project Summary page**, review the information, and click **Finish** to create the project

Project Navigator creates the project file (project_name.xise) in the directory you specified. After you add source files to the project, the files appear in the Hierarchy pane of the

4.7 Design panel:

Project Navigator manages your project based on the design properties (top-level module type, device type, synthesis tool, and language) you selected when you created the project. It organizes all the parts of your design and keeps track of the processes necessary to move the design from design entry through implementation to programming the targeted Xilinx® device.

Note For information on changing design properties, see **Changing Design Properties.**

You can now perform any of the following:

- Create new source files for your project.
- Add existing source files to your project.
- Run processes on your source files.

Modify process properties.

4.8 Creating a Copy of a Project:

You can create a copy of a project to experiment with different source options and implementations. Depending on your needs, the design source files for the copied project and their location can vary as follows:

- Design source files are left in their existing location, and the copied project points to these files.
- Design source files, including generated files, are copied and placed in a specified directory.
- Design source files, excluding generated files, are copied and placed in a specified directory.

Copied projects are the same as other projects in both form and function. For example, you can do the following with copied projects:

- Open the copied project using the File > Open Project menu command.
- View, modify, and implement the copied project.
- Use the Project Browser to view key summary data for the copied project and then, open the copied project for further analysis and implementation, as described in

4.9 Using the Project Browser:

Alternatively, you can create an archive of your project, which puts all of the project contents into a ZIP file. Archived projects must be unzipped before being opened in Project Navigator. For information on archiving, see **Creating a Project Archive.**

To Create a Copy of a Project

1. Select **File > Copy Project**.
2. In the Copy Project dialog box, enter the **Name** for the copy.

Note The name for the copy can be the same as the name for the project, as long as you specify a different location.

3. Enter a directory **Location** to store the copied project.
4. Optionally, enter a **Working directory**.

By default, this is blank, and the working directory is the same as the project directory. However, you can specify a working directory if you want to keep your ISE® project file (.xise extension) separate from your working area.

5. Optionally, enter a **Description** for the copy.

The description can be useful in identifying key traits of the project for reference later.

6. In the Source options area, do the following:

Select one of the following options:

- **Keep sources in their current locations -** to leave the design source files in their existing location.

If you select this option, the copied project points to the files in their existing location. If you edit the files in the copied project, the changes also appear in the original project, because the source files are shared between the two projects.

- **Copy sources to the new location -** to make a copy of all the design source files and place them in the specified Location directory.

On the off chance that you select this choice, the replicated task focuses to the records in the predefined registry. In the event that you alter the documents in the replicated venture, the progressions don't show up in the first venture, in light of the fact that the source records are not shared between the two undertakings.

Alternatively, select Copy documents from Macro Search Path indexes to duplicate records from the registries you indicate in the Macro Search Path property in the Translate Properties dialog box. All records from the predetermined registries are replicated, not only the documents utilized by the configuration.

Note: If you included a net rundown source document specifically to the undertaking as depicted in Working with Net rundown Based IP, the record is consequently replicated as a component of Copy Project in light of the fact that it is a task source document. Adding net rundown source documents to the venture is the favored system for consolidating net rundown modules into your outline, in light of the fact that the records are overseen naturally by Project Navigator.

Alternatively, snap Copy Additional Files to duplicate records that were excluded in the first venture. In the Copy Additional Files dialog box, utilize the Add Files and Remove Files catches to upgrade the rundown of extra documents to duplicate. Extra documents are replicated to the duplicated venture area after every single other record are copied.To reject produced documents from the duplicate, for example, execution results and reports, select

4.10 Exclude generated files from the copy:

When you select this option, the copied project opens in a state in which processes have not yet been run.

7. To automatically open the copy after creating it, select **Open the copied project**.

Note By default, this option is disabled. If you leave this option disabled, the original project remains open after the copy is made.

Click **OK**.

4.11 Creating a Project Archive:

A project archive is a single, compressed ZIP file with a .zip extension. By default, it contains all project files, source files, and generated files, including the following:

- User-added sources and associated files
- Remote sources
- Verilog `include files
- Files in the macro search path
- Generated files
- Non-project files

4.12 To Archive a Project:

1. Select **Project > Archive**.
2. In the Project Archive dialog box, specify a file name and directory for the ZIP file.
3. Optionally, select **Exclude generated files from the archive** to exclude generated files and non-project files from the archive.
4. Click **OK**.

A ZIP file is created in the specified directory. To open the archived project, you must first unzip the ZIP file, and then, you can open the project.

Note Sources that reside outside of the project directory are copied into a remote_sources subdirectory in the project archive. When the archive is unzipped and opened, you must either specify the location of these files in the remote_sources subdirectory for the unzipped project, or manually copy the sources into their original location.

V. LANGUAGE VERILOG HDL

In the semiconductor and electronic outline industry, Verilog is an equipment portrayal language (HDL) used to

show electronic frameworks. Verilog HDL, not to be mistaken for VHDL (a contending dialect), is most generally utilized as a part of the outline, confirmation, and usage of digital rationale chips at the register-exchange level of reflection. It is likewise utilized as a part of the confirmation of analog and blended sign circuits.

5.1 Overview:

Equipment portrayal dialects, for example, Verilog contrast from programming dialects on the grounds that they incorporate methods for depicting the proliferation of time and flag conditions (affectability). There are two task administrators, a blocking task (=), and a non-blocking (<=) task. The non-blocking task permits planners to portray a state-machine upgrade without expecting to pronounce and utilize transitory capacity variables (in any broad programming dialect we have to characterize some provisional storage rooms for the operands to be worked on along these lines; those are impermanent capacity variables). Since these ideas are a piece of Verilog's dialect semantics, architects could rapidly compose portrayals of expansive circuits in a generally minimal and succinct structure. At the season of Verilog's presentation (1984), Verilog spoke to a huge efficiency change for circuit originators who were at that point utilizing graphical schematic capture software and uniquely composed programming projects to report and mimic electronic circuits.

The originators of Verilog needed a dialect with grammar like the C programming dialect, which was at that point generally utilized as a part of designing programming advancement. Verilog is case-delicate, has a fundamental preprocessor (however less advanced than that of ANSI C/C++), and proportional control stream watchwords (if/else, for, while, case, and so on.), and perfect administrator priority. Syntactic contrasts incorporate variable affirmation (Verilog requires bit-widths on net/reg types[clarification needed]), boundary of procedural squares (start/end rather than wavy props {}), and numerous other minor contrasts.

A Verilog configuration comprises of a chain of importance of modules. Modules epitomize plan order, and speak with different modules through an arrangement of pronounced data, yield, and bidirectional ports. Inside, a module can contain any mix of the accompanying: net/variable affirmations (wire, reg, number, and so forth.), simultaneous and successive proclamation squares, and occurrences of different modules (sub-chains of importance). Successive articulations are put inside a start/end piece and executed in consecutive request inside of the square. Be that as it may, the pieces themselves are executed simultaneously, qualifying Verilog as a dataflow dialect.

Verilog's idea of "wire" comprises of both sign qualities (4-state: "1, 0, coasting, indistinct") and qualities (solid, feeble, and so on.). This framework permits conceptual demonstrating of shared sign lines, where numerous sources drive a typical net. At the point when a wire has various drivers, the wire's (lucid) worth is determined by a component of the source drivers and their qualities.

A subset of articulations in the Verilog dialect is synthesizable. Verilog modules that fit in with a synthesizable coding style, known as RTL (register-exchange level), can be physically acknowledged by combination programming. Combination programming algorithmically changes the (unique) Verilog source into a net rundown, a consistently proportionate depiction comprising just of rudimentary rationale primitives (AND, OR, NOT, flip-flops, and so on.) that are accessible in a particular FPGA or VLSI innovation. Further controls to the net rundown at last prompt a circuit manufacture plan, (for example, a photograph cover set for an ASIC or a bit stream record for a FPGA).

5.2 History:

Beginning:

Verilog was the first cutting edge equipment portrayal dialect to be developed. It was made by Phil Moorby and Prabhu Goel amid the winter of 1983/1984. The wording for this procedure was "Robotized Integrated Design Systems" (later renamed to Gateway Design Automation in 1985) as an equipment demonstrating dialect. Passage Design Automation was bought by Cadence Design Systems in 1990. Rhythm now has full restrictive rights to Gateway's Verilog and the Verilog-XL, the HDL-test system that would turn into the accepted standard (of Verilog rationale test systems) for the following decade. Initially, Verilog was proposed to portray and permit reenactment; just a short time later was backing for blend included.

Verilog-95

With the increasing success of VHDL at the time, Cadence decided to make the language available for open standardization. Cadence transferred Verilog into the public domain under the Open Verilog International (OVI) (now known as Accellera) organization. Verilog was later submitted to IEEE and became IEEE Standard 1364-1995, commonly referred to as Verilog-95.

In the same time frame Cadence initiated the creation of Verilog-A to put standards support behind its analog simulator Spectre. Verilog-A was never intended to be a standalone language and is a subset of Verilog-AMS which encompassed Verilog-95.

Verilog 2001

Extensions to Verilog-95 were submitted back to IEEE to cover the deficiencies that users had found in the original Verilog standard. These extensions became IEEE Standard 1364-2001 known as Verilog-2001.

Verilog-2001 is a significant upgrade from Verilog-95. First, it adds explicit support for (2's complement) signed nets and variables. Previously, code authors had to perform

signed operations using awkward bit-level manipulations (for example, the carry-out bit of a simple 8-bit addition required an explicit description of the Boolean algebra to determine its correct value). The same function under Verilog-2001 can be more succinctly described by one of the built-in operators: +, -, /, *, >>>. A generate/endgenerate construct (similar to VHDL's generate/endgenerate) allows Verilog-2001 to control instance and statement instantiation through normal decision operators (case/if/else). Using generate/endgenerate, Verilog-2001 can instantiate an array of instances, with control over the connectivity of the individual instances. File I/O has been improved by several new system tasks. And finally, a few syntax additions were introduced to improve code readability (e.g. always @*, named parameter override, C-style function/task/module header declaration).

Verilog-2001 is the dominant flavor of Verilog supported by the majority of commercial EDA software packages.

Verilog 2005

Not to be mistaken for SystemVerilog, Verilog 2005 (IEEE Standard 1364-2005) comprises of minor rectifications, spec illuminations, and a couple of new dialect elements, (for example, the uwire watchword).

A different piece of the Verilog standard, Verilog-AMS, endeavors to incorporate simple and blended sign displaying with conventional Verilog.

5.3 SystemVerilog:

SystemVerilog is a superset of Verilog-2005, with numerous new components and capacities to help outline confirmation and configuration demonstrating. Starting 2009, the SystemVerilog and Verilog dialect models were converged into SystemVerilog 2009 (IEEE Standard 1800-2009).

The appearance of equipment confirmation dialects, for example, OpenVera, and Verisity's e dialect empowered the improvement of Superlog by Co-Design Automation Inc. Co-Design Automation Inc was later bought by Synopsys. The establishments of Superlog and Vera were given to Accellera, which later turned into the IEEE standard P1800-2005: SystemVerilog.

In the late 1990s, the Verilog Hardware Description Language (HDL) turned into the most generally utilized dialect for portraying equipment for recreation and combination. On the other hand, the initial two forms institutionalized by the IEEE (1364-1995 and 1364-2001) had just straightforward develops for making tests. As configuration sizes exceeded the check capacities of the dialect, business Hardware Verification Languages (HVL, for example, Open Vera and e were made. Organizations that would not have liked to pay for these devices rather burned through several man-years making their own particular custom devices. This profitability emergency (alongside a comparative one on the configuration side) prompted the making of Accellera, a consortium of EDA organizations and clients who needed to make the up and coming era of Verilog. The gift of the Open-Vera dialect framed the premise for the HVL components of SystemVerilog.Accellera's objective was met in November 2005 with the selection of the IEEE standard P1800-2005 for SystemVerilog, IEEE (2005).

The most profitable advantage of SystemVerilog is that it permits the client to build dependable, repeatable check situations, in a predictable linguistic structure, that can be utilized over various undertakings

A percentage of the run of the mill components of a HVL that recognize it from a Hardware Description Language, for example, Verilog or VHDL are

- Constrained-random stimulus generation
- Functional coverage
- Higher-level structures, especially Object Oriented Programming
- Multi-threading and interprocess communication
- Support for HDL types such as Verilog's 4-state values
- Tight integration with event-simulator for control of the design

There are many other useful features, but these allow you to create test benches at a higher level of abstraction than you are able to achieve with an HDL or a programming language such as C.

System Verilog provides the best framework to achieve coverage-driven verification (CDV). CDV combines automatic test generation, self-checking testbenches, and coverage metrics to significantly reduce the time spent verifying a design. The purpose of CDV is to:

- Eliminate the effort and time spent creating hundreds of tests.
- Ensure thorough verification using up-front goal setting.
- Receive early error notifications and deploy run-time checking and error analysis to simplify debugging.

Examples

Ex1: A hello world program looks like this:

```
module main;
initial
begin
$display("Hello world!");
$finish;
end
endmodule
```

Ex2: A simple example of two flip-flops follows:

```
module toplevel(clock,reset);
input clock;
input reset;
```

```
reg flop1;
reg flop2;

always @ (posedge reset or posedge clock)
if (reset)
begin
flop1 <= 0;
flop2 <= 1;
end
else
begin
flop1 <= flop2;
flop2 <= flop1;
end
endmodule
```

The "<=" administrator in Verilog is another part of its being an equipment depiction dialect rather than a typical procedural dialect. This is known as a "non-blocking" task. Its activity doesn't enlist until the following clock cycle. This implies the request of the assignments are immaterial and will deliver the same result: flop1 and flop2 will swap values each clock.

The other task administrator, "=", is alluded to as a blocking task. Whenever "=" task is utilized, for the reasons of rationale, the objective variable is upgraded promptly. In the above illustration, had the announcements utilized the "=" blocking administrator rather than "<=", flop1 and flop2 would not have been swapped. Rather, as in customary programming, the compiler would comprehend to just set flop1 equivalent to flop2 (and along these lines overlook the repetitive rationale to set flop2 equivalent to flop1.)

Ex3: An example counter circuit follows:

```
module Div20x (rst, clk, cet, cep, count, tc);
// TITLE 'Divide-by-20 Counter with enables'
// enable CEP is a clock enable only
// enable CET is a clock enable and
// enables the TC output
// a counter using the Verilog language

parameter size = 5;
parameter length = 20;

input rst; // These inputs/outputs represent
input clk; // connections to the module.
input cet;
input cep;

output [size-1:0] count;
output tc;

reg [size-1:0] count; // Signals assigned
// within an always
// (or initial)block
// must be of type reg
wire tc; // Other signals are of type wire

// The always statement below is a parallel
// execution statement that
// executes any time the signals
// rst or clk transition from low to high

always @ (posedge clk or posedge rst)
if (rst) // This causes reset of the cntr
count <= {size{1'b0}};
else
if (cet && cep) // Enables both  true
begin
if (count == length-1)
count <= {size{1'b0}};
else
count <= count + 1'b1;
end

// the value of tc is continuously assigned
// the value of the expression
assign tc = (cet && (count == length-1));

endmodule
```

Ex4: An example of delays:

```
...
reg a, b, c, d;
wire e;
...
always @(b or e)
begin
a = b & e;
b = a | b;
#5 c = b;
d = #6 c ^ e;
end
```

The dependably statement above represents the other sort of system for use, i.e. the dependably statement executes at whatever time any of the substances in the rundown change, i.e. the b or e change. At the point when one of these progressions, promptly an is doled out another quality, and because of the blocking task b is alloted another esteem a while later (considering the new estimation of an.) After a deferral of 5 time units, c is relegated the estimation of b and the estimation of c ^ e is concealed in an undetectable store. At that point after 6 additional time units, d is appointed the worth that was concealed.

Signals that are driven from inside of a procedure (a beginning or dependably square) must be of sort reg. Signals that are driven from outside a procedure must be of sort wire. The catchphrase reg does not as a matter of course suggest an equipment register.

Constants

The definition of constants in Verilog supports the addition of a width parameter. The basic syntax is:

<Width in bits>'<base letter><number>

Examples:

- 12'h123 - Hexadecimal 123 (using 12 bits)
- 20'd44 - Decimal 44 (using 20 bits - 0 extension is automatic)
- 4'b1010 - Binary 1010 (using 4 bits)
- 6'o77 - Octal 77 (using 6 bits)

5.4 Synthesizable Constructs:

There are several statements in Verilog that have no analog in real hardware, e.g. $display. Consequently, much of the language can not be used to describe hardware. The examples presented here are the classic subset of the language that has a direct mapping to real gates.

```
// Mux examples - Three ways to do the same thing.
// The first example uses continuous assignment
wire out;
assign out = sel ? a : b;
// the second example uses a procedure
// to accomplish the same thing.
reg out;
always @(a or b or sel)
begin
case(sel)
1'b0: out = b;
1'b1: out = a;
endcase
end
// Finally - you can use if/else in a
// procedural structure.
reg out;
always @(a or b or sel)
if (sel)
out = a;
else
out = b;
```

The next interesting structure is a transparent latch; it will pass the input to the output when the gate signal is set for "pass-through", and captures the input and stores it upon transition of the gate signal to "hold". The output will remain stable regardless of the input signal while the gate is set to "hold". In the example below the "pass-through" level of the gate would be when the value of the if clause is true, i.e. gate = 1. This is read "if gate is true, the din is fed to latch_out continuously." Once the if clause is false, the last value at latch_out will remain and is independent of the value of din.

EX6: // Transparent latch example

```
reg out;
always @(gate or din)
if(gate)
out = din; // Pass through state
// Note that the else isn't required here. The variable
// out will follow the value of din while gate is high.
// When gate goes low, out will remain constant.
```

The flip-flop is the next significant template; in Verilog, the D-flop is the simplest, and it can be modeled as:

```
reg q;
always @(posedge clk)
q <= d;
```

The significant thing to notice in the example is the use of the non-blocking assignment. A basic rule of thumb is to use <= when there is a posedge or negedge statement within the always clause.

A variant of the D-flop is one with an asynchronous reset; there is a convention that the reset state will be the first if clause within the statement.

```
reg q;
always @(posedge clk or posedge reset)
if(reset)
q <= 0;
else
q <= d;
```

The next variant is including both an asynchronous reset and asynchronous set condition; again the convention comes into play, i.e. the reset term is followed by the set term.

```
reg q;
always @(posedge clk or posedge reset or posedge set)
if(reset)
q <= 0;
else
if(set)
q <= 1;
else
q <= d;
```

Note: If this model is utilized to display a Set/Reset flip tumble then recreation blunders can come about. Consider the accompanying test grouping of occasions. 1) reset goes high 2) clk goes high 3) set goes high 4) clk goes high again 5) reset goes low took after by 6) set going low. Expect no setup and hold infringement.

In this sample the dependably @ explanation would first execute when the rising edge of reset happens which would put q to an estimation of 0. Whenever the dependably piece executes would be the rising edge of clk which again would keep q at an estimation of 0. The dependably piece then executes when set goes high which in light of the fact that reset is high powers q to stay at 0. This condition could possibly be right contingent upon the real flip lemon. Be that as it may, this is not the fundamental issue with this model. Notice that when reset goes low, that set is still high. In a genuine flip tumble this will make the yield go to a 1. Nonetheless, in this model it won't happen on the grounds that the dependably piece is activated by rising edges of set and reset - not levels. An alternate methodology may be vital for set/reset flip lemon.

Note that there are no "beginning" pieces said in this portrayal. There is a split in the middle of FPGA and ASIC

union apparatuses on this structure. FPGA devices permit introductory pieces where reg qualities are built up as opposed to utilizing a "reset" signal. ASIC combination devices don't backing such an announcement. The reason is that a FPGA's starting state is something that is downloaded into the memory tables of the FPGA. An ASIC is a genuine equipment usage.

5.5 Initial Vs Always:

There are two separate methods for proclaiming a Verilog process. These are the dependably and the beginning watchwords. The dependably watchword demonstrates a free-running procedure. The beginning watchword demonstrates a procedure executes precisely once. Both develops start execution at test system time 0, and both execute until the end of the piece. Once a dependably piece has come to its end, it is rescheduled (once more). It is a typical misguided judgment to trust that a beginning piece will execute before a dependably square. Truth be told, it is ideal to think about the beginning piece as an exceptional instance of the dependably square, one which ends after it finishes surprisingly.

```
//Examples:
initial
begin
a = 1; // Assign a value to reg a at time 0
#1; // Wait 1 time unit
b = a; // Assign the value of reg a to reg b
end

always @(a or b) // Any time a or b CHANGE, run the process
begin
if (a)
c = b;
else
d = ~b;
end // Done with this block, now return to the top (i.e. the @ event-control)
always @(posedge a)// Run whenever reg a has a low to high change
a <= b;
```

These are the classic uses for these two keywords, but there are two significant additional uses. The most common of these is an alwayskeyword without the @(...) sensitivity list. It is possible to use always as shown below:

```
always
begin // Always begins executing at time 0 and NEVER stops
clk = 0; // Set clk to 0
#1; // Wait for 1 time unit
clk = 1; // Set clk to 1
#1; // Wait 1 time unit
end // Keeps executing - so continue back at the top of the begin
```

The always keyword acts similar to the "C" construct while(1) {..} in the sense that it will execute forever.

The other interesting exception is the use of the initial keyword with the addition of the forever keyword.

7.6 Race Condition

The order of execution isn't always guaranteed within Verilog. This can best be illustrated by a classic example. Consider the code snippet below:

```
initial
a = 0;
initial
b = a;
initial
begin
#1;
$display("Value a=%b Value of b=%b",a,b);
end
```

What will be printed out for the values of a and b? Depending on the order of execution of the initial blocks, it could be zero and zero, or alternately zero and some other arbitrary uninitialized value. The $display statement will always execute after both assignment blocks have completed, due to the #1 delay.

7.7 Operators

Note: These operators are not shown in order of precedence.

Operator type	Operator symbols	Operation performed
Bitwise	~	Bitwise NOT (1's complement)
	&	Bitwise AND
	|	Bitwise OR
	^	Bitwise XOR
	~^ or ^~	Bitwise XNOR
Logical	!	NOT
	&&	AND
	||	OR
Reduction	&	Reduction AND
	~&	Reduction NAND
	|	Reduction OR
	~|	Reduction NOR
	^	Reduction XOR
	~^ or ^~	Reduction XNOR
Arithmetic	+	Addition
	-	Subtraction
	-	2's complement
	*	Multiplication

	/	Division
	**	Exponentiation (*Verilog-2001)
Relational	>	Greater than
	<	Less than
	>=	Greater than or equal to
	<=	Less than or equal to
	==	Logical equality (bit-value 1'bX is removed from
	!=	Logical inequality (bit-value 1'bX is removed from
	===	4-state logical equality (bit-value 1'bX is taken as literal)
	!==	4-state logical inequality (bit-value 1'bX is taken as literal)
Shift	>>	Logical right shift
	<<	Logical left shift
	>>>	Arithmetic right shift (*Verilog-2001)
	<<<	Arithmetic left shift (*Verilog-2001)
Concatenation	{ , }	Concatenation
Replication	{n{m}}	Replicate value m for n times
Conditional	? :	Conditional

5.6 System Tasks:

System tasks are available to handle simple I/O, and various design measurement functions. All system tasks are prefixed with $ to distinguish them from user tasks and functions. This section presents a short list of the most often used tasks. It is by no means a comprehensive list.

- $display - Print to screen a line followed by an automatic newline.
- $write - Write to screen a line without the newline.
- $swrite - Print to variable a line without the newline.
- $sscanf - Read from variable a format-specified string. (*Verilog-2001)
- $fopen - Open a handle to a file (read or write)
- $fdisplay - Write to file a line followed by an automatic newline.
- $fwrite - Write to file a line without the newline.
- $fscanf - Read from file a format-specified string. (*Verilog-2001)
- $fclose - Close and release an open file handle.
- $readmemh - Read hex file content into a memory array.
- $readmemb - Read binary file content into a memory array.
- $monitor - Print out all the listed variables when any change value.
- $time - Value of current simulation time.
- $dumpfile - Declare the VCD (Value Change Dump) format output file name.
- $dumpvars - Turn on and dump the variables.
- $dumpports - Turn on and dump the variables in Extended-VCD format.
- $random - Return a random value.

VI. SIMULATION RESULTS

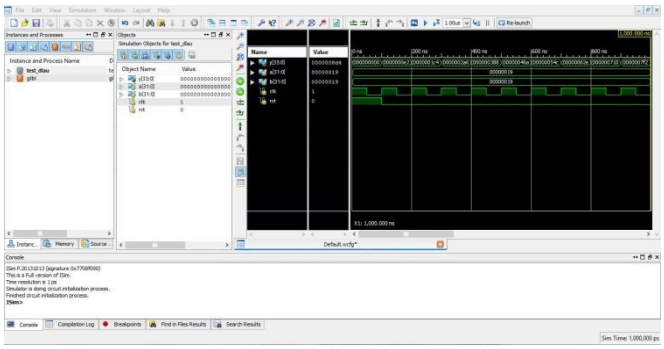

Figure 6.1: Simulation result of the DLAU Accelerator Unit

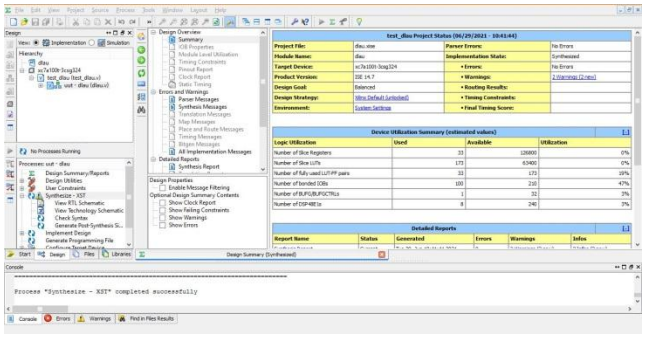

Figure 6.2: Simulation result of the DLAU Accelerator Unit

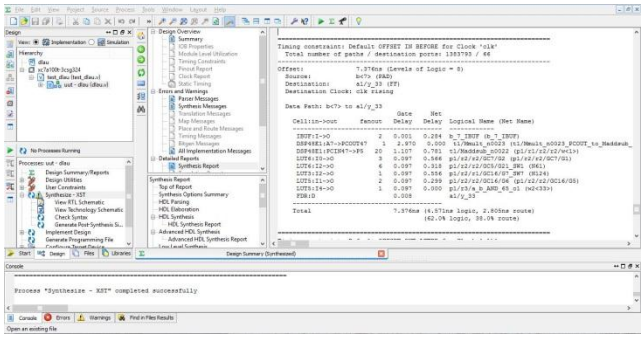

Figure 6.3: Delay report of the DLAU Accelerator Unit

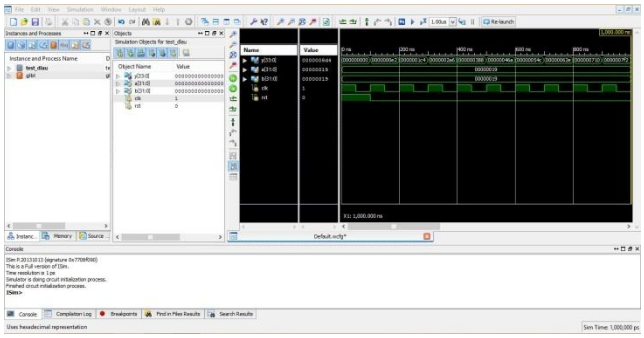

Figure 6.4: Simulation result of the proposed DLAU Accelerator Unit

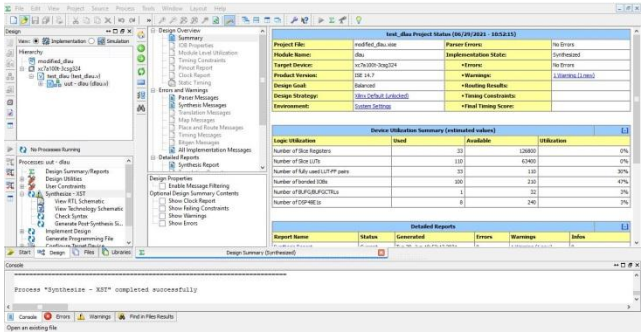

Figure 6.4: Summary report of the proposed DLAU Accelerator Unit

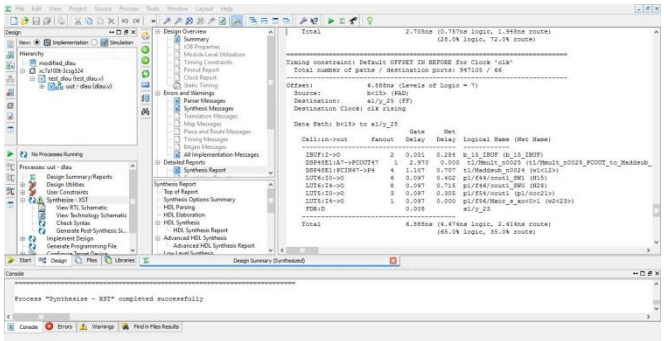

Figure 6.4: Delay report of the proposed DLAU Accelerator Unit

VII. CONCLUSION

In this article we have presented DLAU, which is a scalable and flexible deep learning accelerator based on FPGA. The DLAU includes three pipelined processing units, which can be reused for large scale neural networks. DLAU uses tile techniques to partition the input node data into smaller sets and compute repeatedly by time-sharing the arithmetic logic. Experimental results on Xilinx FPGA prototype. The results are promising but there are still some future directions, including optimization of the weight matrix and memory access. Also the trade-off analysis between FPGA and GPU accelerators is another promising direction for large scale neural networks accelerations..

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IoT Based Advanced Dam Gate Controlling and Water Level Monitoring System Using Arduino

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Abstract---Global climate change and unpredictable rain circle cause uncertainty of water availability. Therefore, the technology which can increase water distribution efficiency is needed. This paper describes prototype water level control system that has an important role in providing convenience in the drainage system. If usually the water gate at the dam is operated manually, this prototype is simulation open and close automatically water gate based on rainfall levels using Arduino. To automatically control open and close the water gate, we use Ultrasonic sensors as input values. The water gate will be driven using a Servo Motor. The output of the water level status is displayed in the form of LCD display and is also followed by sound output for people with visual impairments (blind). The design results of this prototype are expected to be one of the good contributions the drainage system. With this automatic sluice of, the course will minimalize the risk from flood or another risk.

TECHNICAL SPECIFICATIONS:

Domain : Embedded system, IOT.

Software : ARDUINO IDE.

Programming language : Embedded C

Microcontroller : ATMEGA328

Power Supply : +9V, 500mA Regulated Power Supply

Crystal : 11.0592MHz

Sensors : ULTRASONIC SENSORS

Development board: ARDUINO IDE

Motors : DC MOTORS (12-24V DC)

I. INTRODUCTION

Global climate and unpredictable rain circle may cause uncertainty of water availability. Recently, a very important problem from all over the world is the management of water resources. Water is commonly used in households, agriculture, and industry. Therefore, we need technology which can increase water distribution efficiency.

In practice are known that many types of water level control system that can be done. Such system includes providing flood prediction, environmental protection, water discharge, power plant system, providing water control in industry, simple water level control in the home.

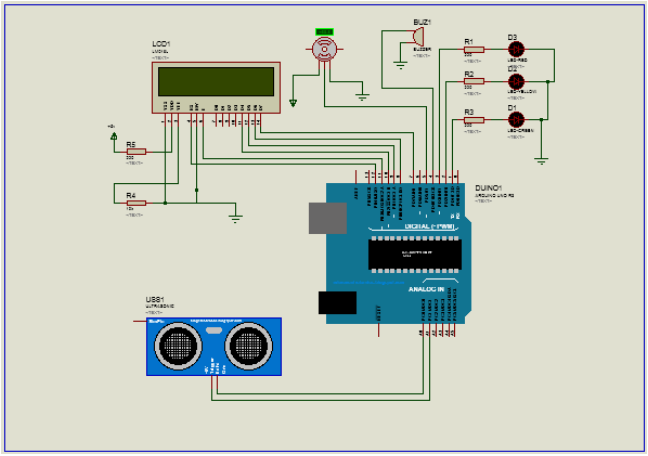
The most efficiency of water distribution system to every aspect can be enhanced through dam automation. For that application can be done by designing open and close automatic water gate at the dam for a drainage system. The drainage system efficiency is not more than 40% if manually operated, through some automation, the drainage system efficiency can be enhanced to 50%.

This paper design prototype water level control system by open and close automatically the water gate use ultrasonic sensor. Open and close automatically the water gate becomes one of the means of service in an effort to control the distribution of more efficient drainage system to every aspect so as to minimalize the risk of the flood.

II. METHODS

Software Design

In this paper, the ultrasonic sensor reads the water level in the aquarium as input to the Arduino. As output, the servo would move the door aquarium, and water level conditions would be visible on LCD and led, as illustrated in the following schematic capture by Proteus (Figure 1).



The open and close automatically water gate operation is illustrated in block diagram system (Figure 2). The diagram contains several parts, that is, water level detected by the ultrasonic sensor, input data from ultrasonic sensor to Arduino, Arduino set servo motion, the servo for moving the water gate (the door aquarium), and the ultrasonic sensor for making feedback to Arduino. If the water level is low so the door would close.

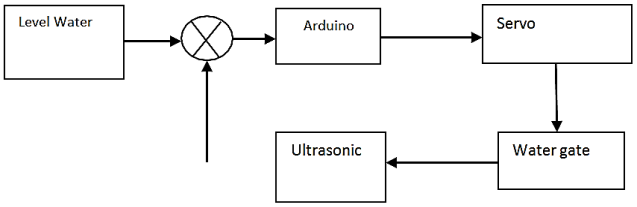


Figure 2. Block diagram system.

The paper programs is set to 3 water level conditions, that is "AMAN" at water level ≤ 5 cm from ultrasonic sensor, "SIAGA" at 5 cm ≥ dist ≤ 10 cm from ultrasonic sensor, and "AWAS" at ≥ 10 cm from ultrasonic sensor. Designing software programs using Arduino software with C programming language.

Hardware design

Plant uses a glass aquarium with a door hole on the front. Aquarium measuring 50 x 30 x 20 cm. The door opening is 5 x 5 cm in size. The door is used using acrylic material with a size of 7 x 7 cm.

The working principle of the ultrasonic sensor is the transmitter sending ultrasonic waves, then measuring the time required until the arrival of the reflection of the object. Ultrasonic sensor used is SRF-05. The time difference when transmitted to capture returns is used as a reference calculation of how far the distance between the sensors with the object that reflects the ultrasonic waves [8]. Ultrasonic Sensor Devantech SRF-05 with the following specifications:

- Works on a 5 volt DC voltage
- Current load of 30 mA - 50 mA
- Generate a wave frequency of 40 KHz
- The range of detectable distance of 3 cm - 400 cm
- Requires a minimum input trigger of 10 uS

It can be used in two choices of input trigger mode and echo output mounted on different pins or input trigger and echo output mounted in one pin the same [9].

The ultrasonic sensor SRF-05 has the following views

ADVANTAGES:

- Low cost,
- automated operation,
- Low Power consumption.

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An Advanced Embedded System for Woman Safety by Using GPS

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Abstract--- This Project presents a women safety detection system using GPS and GSM modems. The system can be interconnected with the alarm system and alert the neighbors. This detection and messaging system is composed of a GPS receiver, Microcontroller and a GSM Modem. GPS Receiver gets the location information from satellites in the form of latitude and longitude.

The Microcontroller processes this information and this processed information is sent to the user using GSM modem A GSM modem is interfaced to the MCU. The GSM modem sends an SMS to the predefined mobile number. When a woman is in danger and in need of self-defense then she can press the switch which is allotted to her. By pressing the switch, the entire system will be activated then immediately a SMS will be sent to concern person with location using GSM and GPS.

TECHNICAL SPECIFICATIONS

Domain	: Embedded system
Software	: ARDUINO IDE
Programming language	: Embedded C
Microcontroller	: ATMEGA328
Power Supply	: +9V, 500mA Regulated Power Supply
Development board	: ARDUINO IDE

I. INTRODUCTION

- Women safety is a very important issue due to rising crimes against women these days.
- To help resolve this issue, a GPS based women safety system is proposed that has dual security feature.
- This device consists of a system that ensures dual alerts in case a woman is harassed or she thinks she is in trouble.
- This system can be turned on by a woman even if she thinks she would be in trouble.
- It is useful because once an incident occurs she may or may not get the chance to press the emergency button.
- In a button press alerting system, if a woman is hit on her head from behind, she might never get a chance to press panic button and no one will know she is in trouble.

II. EMBEDDED SYSTEM

The advanced embedded system aims to introduce students with a range of techniques and methodologies used in embedded system design through the design and implementation of a practical project to accomplish an interactive task involving hardware and software aspects which would be socially helpful for security purposes

An embedded system can be thought of as a computer hardware system having software embedded in it. An embedded system can be an independent system or it can be a part of a large system. An embedded system is a microcontroller or microprocessor based system which is designed to perform a specific task. For example, a fire alarm is an embedded system; it will sense only smoke.

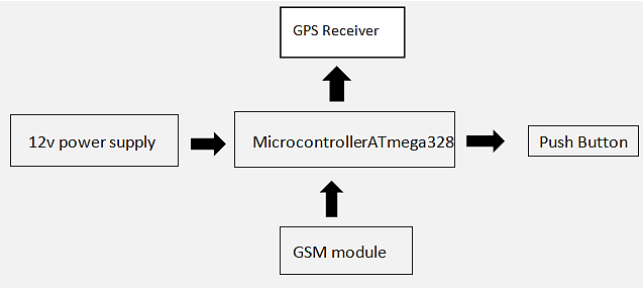
- An embedded system has three components −

- It has hardware.
- It has application software.
- It has Real Time Operating system (RTOS) that supervises the application software and provide mechanism to let the processor run a process as per scheduling by following a plan to control the latencies. RTOS defines the way the system works. It sets the rules during the execution of application program. A small scale embedded system may not have RTOS.

III. COMPONENTS

- Arduino Uno
- GSM Module
- GPS Module
- Power supply
- LEDs
- Push Buttons
- Capacitors
- Resistor

IV. BLOCKDIAGRAM



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Android Controlled Robot for detecting Metal Mines using GSM

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I. INTRODUCTION

This paper studies design and implementation of the Android GSM controlled robotic system aims at achieving successful surveillance at places human intervention is at high risk such as hot or sub zero temperature environment, war fields, disaster affected zone, etc. It also aims to fulfill the task assigned to the user through various text messages.

GSM controlled robotic system is very beneficial in areas where there is high risk for humans to enter. GSM controlled robotic system is controlled through text message commands received via android device. The integration of control unit with messages is achieved using a Arduino and GSM module to transmit and receive the message commands.

II. EXISTING METHOD

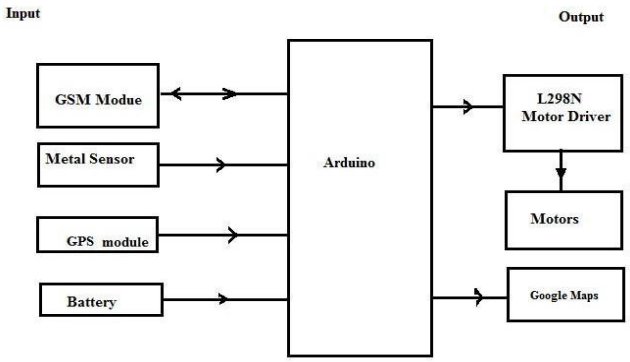
The existing robotic vehicle operates as per the command received via android device using Bluetooth module which is capable about 10meters, for this Arduino is integrated in the system. The controlling device may be any smart phone having an android OS. The transmitter uses an android application required for transmitting the data, The receiver end reads these commands and interprets them into controlling the robotic vehicle.

When a key is pressed, the corresponding data is transmitted to the Bluetooth Module from the phone over Bluetooth communication. In the Arduino code, the Arduino receives any of this data from the Bluetooth Module and perform a simple switch case operation, where each case associated with appropriate instructions to the motor driver input pins. The android device sends commands to move the vehicle in forward, backward, right and left directions. After receiving the commands, Arduino operates the motors in order to move the vehicle in four directions. The communication between android device and receiver is sent as serial communication data.

III. PROPOSED METHOD

The GSM module is interfaced with Arduino in replacement to the Bluetooth module, where a robot vehicle can operate from any place of world with a single text message. Arduino program is designed to move the motor through a motor driver circuit as per the text commands sent by android device.GPS module is used to find the present location of robot which is send in text message to the mobile in latitude and longitude. A Metal detector sensor is added to send the information in text format to phone if any explosive materials are detected to robot.

IV. CIRCUIT DIAGRAM



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Comparative Analysis and Design of Solid and Multilayered Composite Pressure Vessel

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Abstract— A pressure vessel is designed to work under a high internal pressure condition, so selecting material and the vessel's design are the most crucial parts. This paper compares the solid pressure vessel made of a steel s515-gr70 and composite material pressure vessel made of epoxy s-glass, epoxy e-glass and epoxy carbon. The static deformation, von-mises stress and strain energy for a pressure vessel calculated with multi-layered composite material. The main objective of the work is to compare the solid pressure vessel with composite material pressure vessel and multi-layered composite pressure and find out the best suitable material and design for the pressure vessel to reduces the stress on the object; here, we are designing one more model, i.e., multilayer vessel and calculating the deformation and stress and strain energy values from all these values and all other material combinations we conclude which composite is the most suitable and efficient pressure vessel.

Index Terms— Design, Analysis, Solid & Multilayer Composite pressure Vessel.

I. INTRODUCTION

In Process Industries, like chemical and petroleum, boiler industries, there are design restrictions for large volumes of high internal pressures in metallic single-wall cylindrical vessels. As the pressure of the operating fluid rises, an increment in the thickness of the vessel intended to hold that fluid is an automatic choice. The increment in the thickness beyond a specific value will pose fabrication difficulties and demand more robust material for the vessel construction. Due to increasing demands from the process industry for higher operating pressures and temperature, new technologies developed and underdeveloped to handle the present-day specialised requirements. Multilayer Pressure Vessels have broadened the art of pressure vessel fabrication or construction and introduce the process designer with a genuine piece of valuable equipment. In a wide range of operating conditions for the problems generated by the storage of hydrogen and hydrogenation processes, the term pressure vessel referred to those reservoirs or containers which subjected to internal or external pressures.

Pressure vessels find wide applications in thermal and nuclear power plants, process, and chemical industries, space and ocean depths, and water, steam, gas, and air supply systems in industries. The pressure vessel material may be brittle such as cast iron, or ductile such as mild steel.

Multilayer composite vessels are built up by wrapping and combining a series of sheets over a core tube to give a unique combination of properties. The construction involves using several layers of material, like metals, alloys, plastic co-polymers, minerals, and wood, usually for quality control and optimum properties. Multilayer construction used for higher pressures. It provides inbuilt safety, high stiffness, strength-to-weight ratio, long fatigue life, utilises material economically, no stress relief required. The finite element method is exceptionally versatile and efficient for analysing the complex structural behaviour of multilayered composite laminated structures. Using the finite element method, a significant amount of research devoted to the analysis of deformation, stress, and strain energy.

II. LITERATURE SURVEY

Zhang et al. [1] derived an analytical solution for determining the stress distribution of a multi-layered composite pressure vessel subjected to internal fluid pressure and a thermal load. The stress distribution of the pressure vessel computed using the FE method. Ali, Ghosh, and Alam

[2] investigated the effect of the auto frottage process in strain hardened thick-walled pressure vessels theoretically by FE modelling. Wang and Ding [3] obtained the thermoelastic dynamic solution of a multi-layered orthotropic hollow cylinder in the state of axisymmetric plane strain. Atefi and Mahmoudi [4] offered an analytical solution for obtaining thermal stresses in a pipe caused by periodic time-varying of the temperature of the medium fluid. Jabbari, Sohrabpour, and Eslami [5] developed a general analysis of one-dimensional steady-state thermal stresses in a thick hollow cylinder made of functionally graded material. Shao, Wang, and Ang [6] carried out a thermomechanical analysis for the functionally graded hollow cylinder subjected to axisymmetric mechanical and transient thermal loads.

In engineering applications, the thick-walled cylinder subjected to internal heat flow. Typical examples are nuclear engineering structures, nozzle sections of rockets, gun tubes, and dies of hot forming tools. The study of thick-

walled cylinders subjected to internal heat flow and internal pressure is a problem of great practical interest. Industrial demands for such applications have focused the researcher on research on these topics. However, most investigators have only dealt with the analysis of thermal stresses of thick-walled cylinders under steady-state conditions [7]. Conductivity as a function of temperature concluded that the effect of thermal conductivity on the temperature and stresses is slight for small values of internal heat flow. However, the difference in temperature and stresses between temperature-dependent-independent thermal conductivity can be as much as 20% for large heat flow. Vollbrecht [8] has analyzed the stresses in cylindrical and spherical walls subjected to internal pressure and stationary heat flow.

III. PROBLEMS DEFINITION

This paper will compare the solid pressure vessel and multi-layered pressure vessel and find the best suitable material and design for the pressure vessel. It modeled using CREO, and analysis is carried out into Ansys software using the structural analysis method. The von-mises stress, deformation and strain energy found for various pressure vessel materials.

The pressure vessel material for analysis is M.S. steel and composite material such as glass epoxy fiber and epoxy carbon.

IV. METHODOLOGY

Modelling of the pressure vessel:

A virtual model of the solid pressure vessel and the composite pressure vessel created using CREO software; then, the model imported to ANSYS for analysis. The results of deformation, stress and strain analysis of different materials compared with each other.

The line diagram of the pressure vessel shown in Fig. 1. The 3D model of the pressure vessel created in CREO and demonstrated in Fig. 2.

V. GEOMETRY AND BOUNDARY CONDITION

1. Geometry of reference model for creating an object:

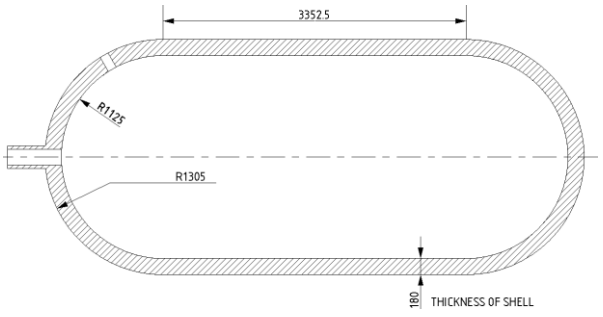

Fig. 1. Line Diagram of the Pressure Vessel

2. 3D Model

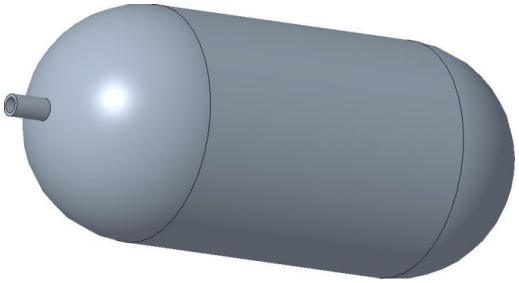

Fig. 2. 3-D CAD model of the Pressure Vessel

3. Meshing (FE Modeling)

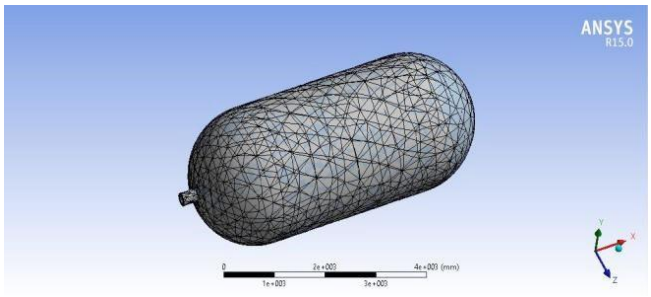

Fig. 3. FE Tetra-Mesh of Pressure Vessel in Ansys Workbench

4. Boundary Conditions

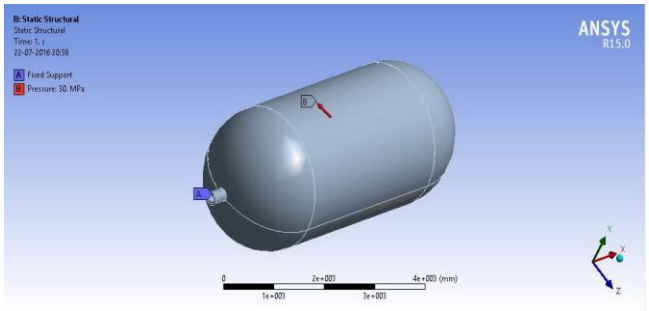

Fig. 4. Boundary Conditions of the Pressure Vessel

VI. STATIC STRUCTURAL ANALYSIS RESULT

This paper aims to determine the static analysis of the pressure vessels like deformation, stress, and strain energy. Effects of the different materials of steel and different composite materials and multilayered composite material on static deformation, stress and strain energy are investigated, including comparison with results using Creo and Ansys.

The material properties of various materials with which the pressure vessel made are:

Mild Steel:

Young's modulus: 205 x 10^9 Pa, Poisson's ratio: 0.29,

Density: 7850 Kg/m^3.

Epoxy e-glass:

Density: 2000 kg/m^3, Young's modulus in x-direction: 45x 10^9 Pa, Young's modulus in y-direction: 10x10^9 Pa, Young's modulus in z-direction: 10x10^9 Pa, Poisson's ratio in xy: 0.3, Poisson's ratio in yz: 0.4, Poisson's ratio in zx: 0.3.

Epoxy s-glass:

Density: 2000 kg/m^3, Young's modulus in x-direction: 50 x 10^9 Pa, Young's modulus in y-direction: 8 x10^9 Pa, Young's modulus in z-direction: 8 x10^9 Pa, Poisson's ratio in xy: 0.3, Poisson's ratio in yz: 0.4, Poisson's ratio in zx: 0.3.

Epoxy carbon:

Density: 1480 kg/m^3, Young's modulus in x-direction:

91.82 x 10^9 Pa, Young's modulus in y-direction: 91.82 x 10^9 Pa, Young's modulus in z-direction: 9 x10^9 Pa, Poisson's ratio in xy: 0.05, Poisson's ratio in yz: 0.3, Poisson's ratio in zx: 0.3.

A. ***Analysis of Solid Pressure Vessel***

(Existing material (steel s515-gr70))

1. Deformation

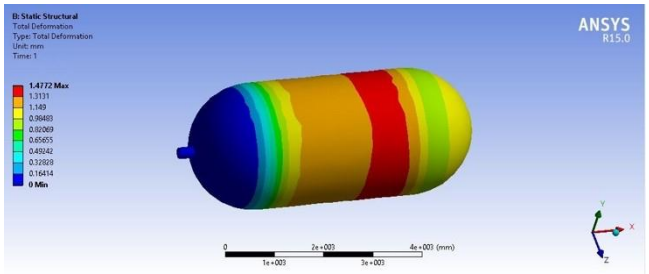

Fig. 5. Static Structural Deformation of Steels515-gr70

2. Stress

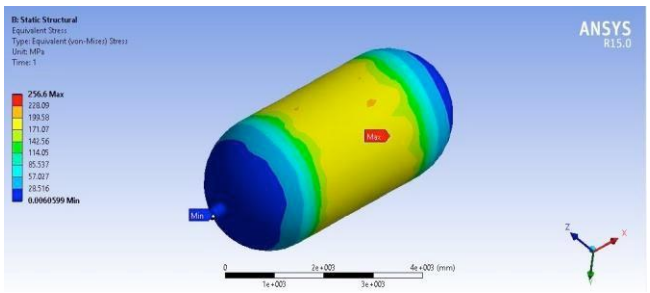

Fig. 6. Static Structural Von-Mises stress of Steels515-gr70

3. Strain Energy

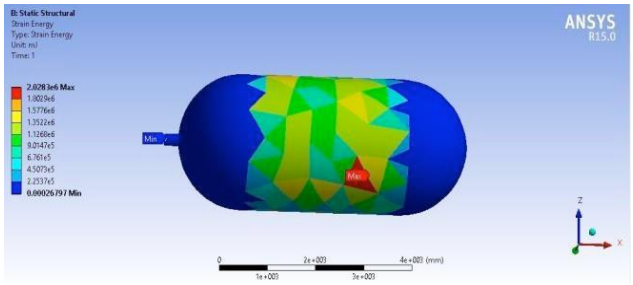

Fig. 7. Static Structural Strain Energy of Steels515-gr70

When we applied 30Mpa pressure on the vessel, it produces stress of nearly 256Mpa to reduces the stress on the body; here, we are changing material. We have chosen three composite materials now, and we will analyze these three materials with the same boundary conditions.

B. ***Analysis of Composite Material***

I. Epoxy s-glass

1. Deformation

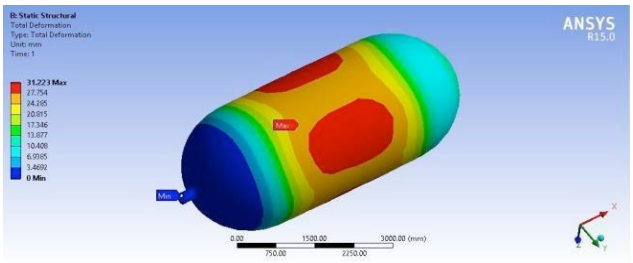

Fig. 8. Static Structural Deformation of Epoxy s-Glass

2. Stress

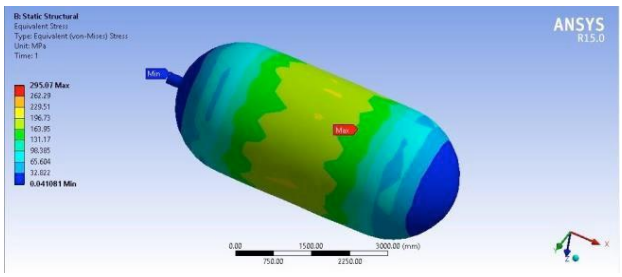

Fig. 9. Static Structural Von-Mises stress of Epoxy s-Glass

3. Strain Energy

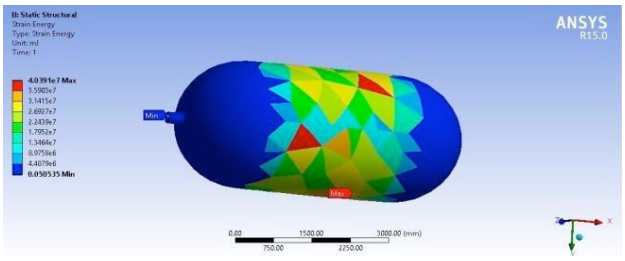

Fig. 10. Static Structural Strain Energy of Epoxy s-Glass

II. Epoxy e-glass

1. Deformation

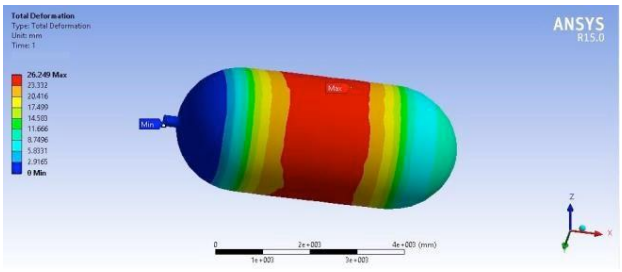

Fig. 11. Static Structural Deformation of Epoxy e-Glass

2. Stress

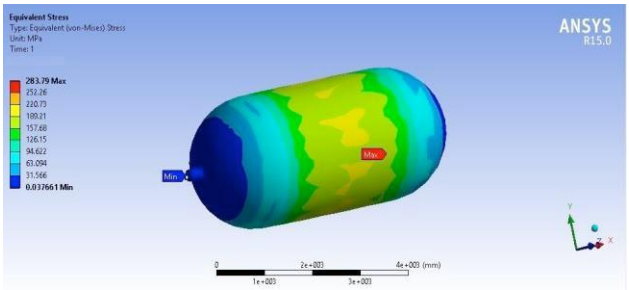

Fig. 12. Static Structural Von-Mises stress of Epoxy e-Glass

3. Strain Energy

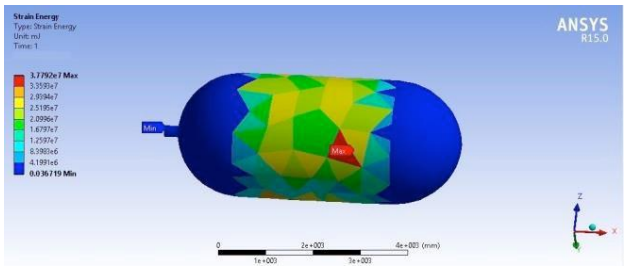

Fig. 13. Static Structural Strain Energy of Epoxy e-Glass

III. Epoxy Carbon

1. Deformation

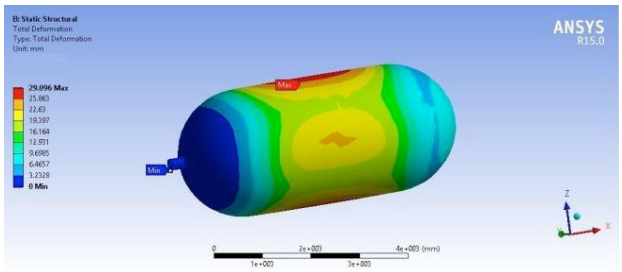

Fig. 14. Static Structural Deformation of Epoxy Carbon

2. Stress

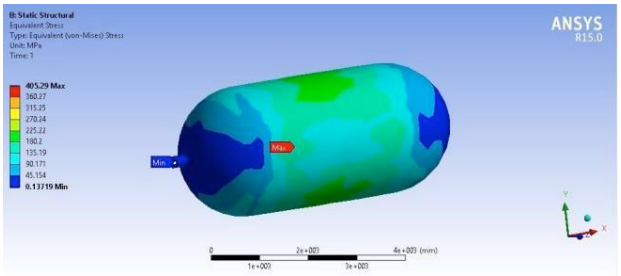

Fig. 15. Static Structural Von-Mises stress of Epoxy Carbon

3. Strain Energy

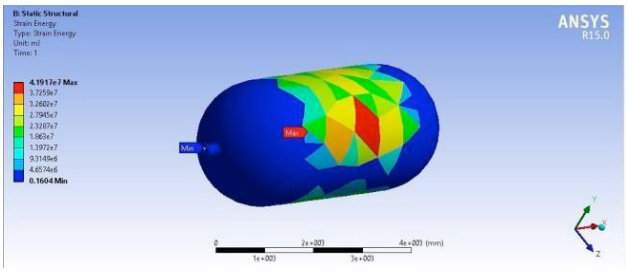

Fig. 16. Static Structural Strain Energy of Epoxy Carbon

TABLE I. RESULT OF SOLID AND COMPOSITE MATERIAL VESSEL

Material	*Deformation (mm)*	*Stress (Mpa)*	*Strain energy (mJ)*
Steel-s515-gr70	1.6143	264.48	9.3644e5
Epoxy s-glass	31.223	295.07	4.0391e7
Epoxy e-glass	26.249	283.79	3.7792e7
Epoxy-carbon	29.096	405.29	4.1917e7

We can say that the deformation values are low for steel-s515-gr70 and high for epoxy e-glass. The stress has been increasing for all materials and in this steel-s515-gr-70 have fewer stress values, and epoxy carbon has high-stress values.

The above solid vessel (180 mm thickness) results when we change material from ss515-gr70 to composite materials; no other material gave fewer stress values. By these changes,

the stress increased, so we cannot use complete composite material for a vessel. So we follow another concept, i.e., multilayer vessel; in this process, we have created the original model with the exact dimensions, but here we made two layers for a vessel which are those 162mm and 18mm, respectively, and here we are applying the outer layer as same steel-s515-gr70 but inner material we are adding composite materials.

VII. STEEL-S515-GR70 AND EPOXY-CARBON COMPOSITE MATERIAL

1. Geometry Modification of model for creating the object:

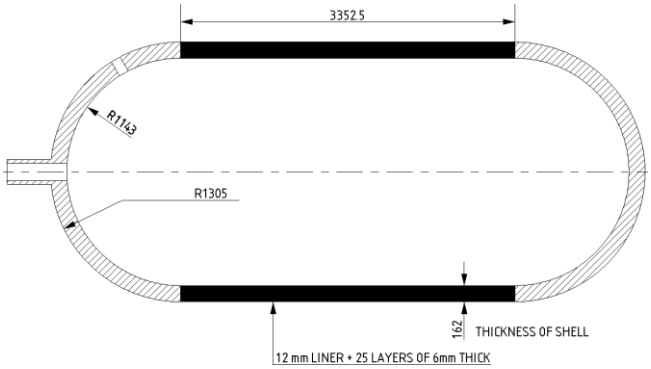

Fig. 17. Line Diagram of the Multi-layered Composite Pressure Vessel

We are going to create one newer model of multilayer composite pressure vessel. The line diagram of the multilayer composite pressure vessel shown in Fig. 17.

The construction of the multilayer composite pressure vessel is:

Total No. of layers: 26, (25 shell layers + 1Liner)

Total Thickness: 162 mm; Liner thickness: 12 mm & Each Shell layers Thickness, t: 6 mm.

1. Deformation

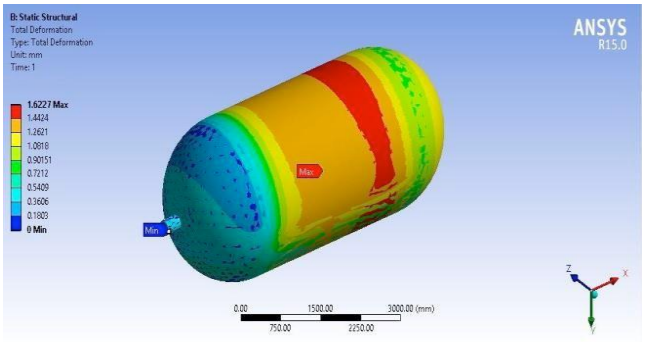

Fig. 17. Static Structural Deformation of Steel-s515-gr70 and Epoxy Carbon

2. Stress

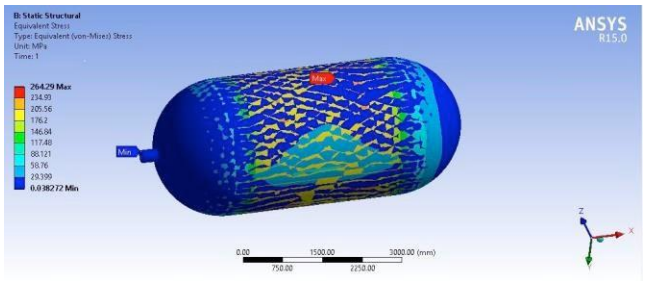

Fig. 18. Static Structural Von-Mises stress of Steel-s515-gr70 and Epoxy Carbon

3. Strain Energy

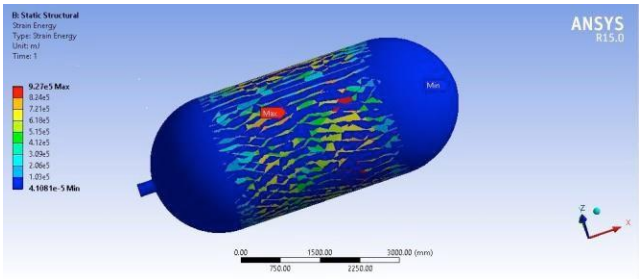

Fig. 19. Static Structural Strain Energy of Steel-s515-gr70 and Epoxy Carbon

TABLE II. RESULT OF STEEL-S515-GR70 AND EPOXY MATERIAL

Material	*Deformation (mm)*	*Stress (Mpa)*	*Strain energy (mJ)*
Steel-s515-gr70 & epoxy-s-glass	1.6152	264.49	9.3705e5
Steel-s515-gr70 & epoxy-e-glass	1.4772	256.6	2.0283e6
Steel-s515-gr70 & epoxy-carbon	2.1842	230.25	9.27e5

Deformation: Values for all multilayer models and in this steel-s5155 and epoxy e-glass has produced minor deformation among all and steel-s515-gr70 and epoxy carbon-producing high deformation.

Stress: For steel-s515-gr70 producing high deformation, it has exceptionally low stresses among all other materials. **Strain Energy:** From all results here, steel-s515-gr70 and epoxy e-glass having high energy compares to others. But it also has high-stress values, which is not safe for a model.

VII. CONCLUSION

In this paper, we analyze one solid vessel (180mm thickness) of existing material steel-s515-gr70 and applied 30Mpa pressure on it. We got nearly 256Mpa stress on the whole body; to reduce these stress values, we use entirely composite materials: epoxy carbon and epoxy e-glass and epoxy s-glass, respectively. But these changes will not satisfy our condition. These composite materials have excellent strength compare with existing material, but it also produces remarkably high stress on the body.

To avoid these stresses on the model, we have done one more model called multilayer vessel (162mm thick & 18mm thick) with steel-s515-gr70 and composite material, respectively and analyses with the same boundary conditions and calculated results for all combinations. From all combination results, steel-s515-gr70 with epoxy carbon produces fewer stress values 230Mpa only compared to a solid vessel; by this change, we have been reduced 35Mpa stresses on the body, and composite materials are lightweight, so we reduce component weight in this case.

Finally, we conclude that a multilayer vessel with (steel-s515-gr70&epoxy carbon) gave fewer stress values than a solid vessel with steel-s515-gr70 materials.

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Assessment on the Effects of Using Formwork Materials in Construction Sector

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Abstract— Formwork materials are useful in the project of the construction. It has several effects on the quality of the project. This research study has described the effects of the formwork materials in a well manner. Benefits of the materials are discussed in this regard. Flowchart is given in this study for understanding the work process of the formwork materials in the project of construction. Diagram as well as statistical data from other research paper are also included in this study. At the end a profound conclusion has been drawn.

Index Terms— Formwork materials, construction project, casting process, quality management, cost management

I. INTRODUCTION

Formwork material in the construction industry is one of the crucial aspects that can be considered in a well manner. In this aspect, the process of casting is critically analysed with the help of this type of materials in the sector of construction. It can be said that with the help of formwork material, it is required to augment the process of casting in a well approach. It has been found that there are certain advantages of formwork material that should be taken into account effectively. This research study is going to evaluate the usage of the formwork materials in the construction sector of the marketplace. Moreover, advantages of the formwork materials are considered in this aspect. Furthermore, the effects of the materials of formwork are also going to be described in this research study. The novelty of this paper is going to be analysed in a well manner in this study.

II. USAGE OF FORMWORK MATERIALS

It can be possible for the formwork analysis that is used in the construction sector in a well manner. It is required to state that formwork materials are useful in the construction industry to complete the work of the project effectively. It has been found that there are certain essential aspects in the marketplace. Metal formwork systems are enhanced protected against fire as well as rot than traditional timber formwork. It is basically a re-usable plastic formwork (Mansuri *et al*. 2017). These modular along with the interlocking systems are used for the purpose of building widely variable However, it is comparatively simple as well as concrete in structure. The panels are frivolous and very healthy. It can be possible to elucidate that the formwork material are used for the project of construction industry. It is required to focus on different types of formwork material in a well manner. It can be possible to elucidate that this is basically used in the process of casting by considering the fresh concrete in order to provide the anticipated shape as well as surface.

It can be possible to elucidate that there are certain aspects of setting form in the construction on a collective note. It can be stated that by considering the improper formwork materials as well as workmanship during the time of casting can result in many concrete ruining problems such as stains as well as discoloration, and brushing are attributed to formwork of concrete (Søndergaard *et al.* 2018). Additionally, some misshapen concrete shells are due to distorted formwork systems that is caused by repetitive reprocess of formwork and insufficient provision of formwork. In addition to this, formwork materials are used for managing the work of the construction project on a systematic note. It can be feasible to manage the functions of the formwork materials. It is required to manage the importance of the formwork materials effectively. It has been identified that functions of the formwork material should be evaluated in a well manner for augmenting the efficiency of the process of casting effectively. The utilisation of the material of formwork ought to be considered effectively. It can be possible to explicate that with the help of the formwork materials, it is needed to complete the work of the project within the stated time period.

III. ADVANTAGES OF FORMWORK MATERIALS

It can be stated that there are certain benefits of formwork materials in this context. It is required to manage the profit margin of the construction work by considering the formwork material in an effectual manner. It can be evaluated that the advantages of the materials of formwork help to understand the importance of this aspect in a well manner. The benefits are outlined below in a detailed note:

Easy to fix

It can be possible to elucidate that with the help of the formwork materials, it is required to develop the fixed structure of the building in an effective way. It is required to focus on the process of building different things by using a concrete structure effectively. It is quite useful for the organisation to manage the construction related activities (Rajeshkumar *et al*. 2021). It can be feasible to improve the potentiality of the work on a significant note. It is effective

for the construction workers to manage the process of casting effectively.

Easy handling

It can be feasible to state that easy handling is one of the key aspects of the formwork material during the management of construction project. It helps to meet the objectives of the construction project on a collective note. It is needed for the organisation to manage the cost of the company effectively to improve business profitability effectively. In addition to this, it is required to manage the business profit by managing the cost as well as cash flow of the construction project. Formwork material are helpful to handle the cost of the construction project effectively.

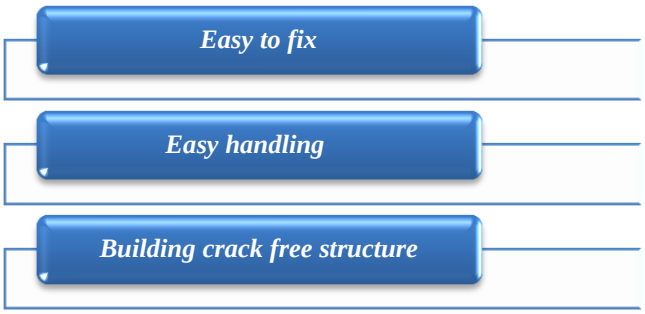

Figure 1: Advantages of formwork material
(Source: Rajeshkumar *et al*. 2021)

Building crack free structure

It can be stated that with the help of the formwork material, it is needed to build a crack free structure of the building or other construction related things in the marketplace of the country. It can be effective for the project manager to develop a strong structure of the building or other constructed material. It is helpful for the organisation in the sector of construction to manage the business operation in the potential marketplace by meeting the needs of the consumers. Quality management is an essential aspect in this regard (Lee *et al*. 2018). As for this reason, the material of formwork is used in this context. It helps to meet the requirements of the client by managing cost, time along with the quality of the construction work effectively.

The above advantages need to be considered in this aspect for completing the project of construction within the stated period of time. It is helpful for the project manager to develop the crack free building effectively. It is also possible to focus on the materials used in the project of the construction. It can be evaluated that easy fixing is required to manage the work of the construction. It is also possible to handle the cost of the project effectively. It is also feasible for the project worker to maintain the work quality by using the formwork materials in an effectual note.

IV. EFFECTS OF FORMWORK MATERIALS ON CONSTRUCTION SECTOR

It can be possible to explicate that effects of the formwork material on the sector of the construction business need to be evaluated on a detailed note. It can be evaluated that with the help of the formwork materials quality of the work is possible to be maintained on a collective note. It is helpful for the organisation to manage the business work quality effectively.

Forms ought to be accurately clean, set as well as tight. Along with this, it should be sufficiently steadied, as well as constructed of or likened with resources that can instruct the anticipation of the form in order to finish to the toughened concrete (Nemati *et al.* 2017). Wood forms along with unless lubricated or then treated with a form-release agent in the project of construction, would be diminished before placing the concrete. It is because, these can absorb water from the existing and swell. Forms need to be made for elimination with least impairment to the concrete. With the help of the wood forms, it is possible to avoid the use of too large and/or too many pins for facilitating the removal as well as decrease of the damage. As for this reason, it is possible to explain that in the project of construction, it is needed to use the formwork materials effectively. It is also possible for the organisation to manage the work of this materials in a well manner in order to maintain the quality of the building as well as other construction related work (Suasira *et al*. 2020). In addition to this, time management is also done in the construction work for meeting the requirements of the client. It can be feasible to focus on the process of casting in this regard. It helps to manage the entire work process properly.

In the sector of construction, it is possible to analyse different types of form that have the effects on the project.

Timber Formwork

It can be explicated that this formwork has the positive effects on the construction project. It helps to handle the work easily within the given period of time. As for this reason, it poses positive impacts on the construction. It is also easy to disassemble in this aspect. It is also effective for the construction project to deal with any obstructions that occur during the project management. It has been identified that with the help of the timber formwork in the project of the construction, it is required to make the process of development flexible (Huszár and Lublóy, 2021). It is also helpful for the project manager to replace the damaged part with new thing during the construction work. As for this reason, the timber formwork materials are quite useful for the organization.

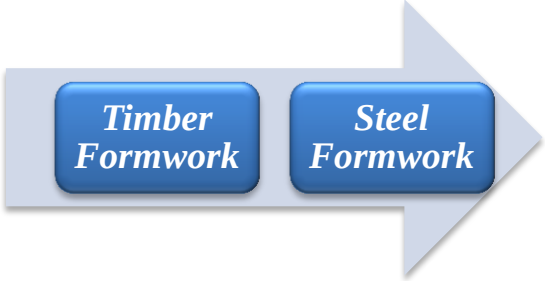

Figure 2: Formwork material
(Source: Huszár and Lublóy, 20210

Steel Formwork

It can be stated that steel formwork is useful for the organisation in the construction sector. It is because, steel forms are quite strong in nature as well as it is solid to build the shape properly. It has been identified that with the help of this formwork materials, it is required to make the shape limited in size (Tahmoorian *et al.* 2020). It is because, steel formwork are limited in the size. However, it is possible to use many steel formwork s as per the requirements.

V. COMPARISON FROM OTHER PAPERS

It can be compared with the article named ***Assessment on the Effect of Using Different Types of Formwork Materials on Building Construction: A Case Study in Benshangul Gumuz Region*** y considering the information contained within it (GIZACHEW, 2020). It has been found from the mentioned article that different formworks are used in the sector of construction by considering the mean value of the collected data (GIZACHEW, 2020). However, in this research paper, qualitative data can be used for understand the positive along with negative effects of usage of formworks in the construction sector of the country. The analysis is quite in-depth as well as qualitative in this research paper.

In the mentioned paper the work responsibilities are given in the graphical manner below:

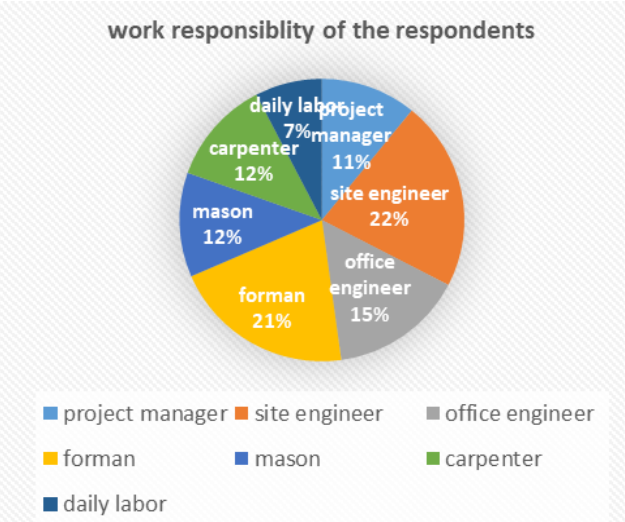

Figure 3: Work responsibilities

(Source: GIZACHEW, 2020)

Quality of concrete is also given in this research paper by focusing on mean value of data.

No.	Concrete quality related problems	Mean	Rank
P1	Quality of the surface of concrete finish is affected by form working and formwork martials	4.61	4
P2	Using timber formwork more repeatedly results poor quality concrete finish.	3.78	9
P3	Incorrect aligning or positioning of formwork results poor quality concrete finish.	4.62	3
P4	Bad form joints, offsets and poor facing materials /oiling material/results poor quality concrete finish.	3.82	8
P5	Corrective works /e.g. chiseling/ are results of poor form working.	3.68	10
P6	Discoloring of concrete surface resulted due to oiling of the form work material.	4.51	5
P7	Steel form work results a smooth concrete surface than timber forms.	4.56	4
P8	Using steel formwork connected by nails and wires results small openings at the joints.	3.98	7
P9	Misplaced surface on concrete surface is resulted from incorrectly aligning or positioning formwork materials.	4.70	1
P10	Using eucalyptus during column form working than wooden battens gives bad concrete surface.	4.67	2

Table 1: Formwork material

(Source: GIZACHEW, 2020)

In this aspect, it can be said that, in the current paper, the researcher has found that timber formwork is mostly effective in order to manage cost, quality along with time of the construction work.

VI. NOVELTY OF PAPERS AND RESULT

In this aspect, a result analysis needs to be described on the basis of the proposed flow chart of the research work. The diagram is given below:

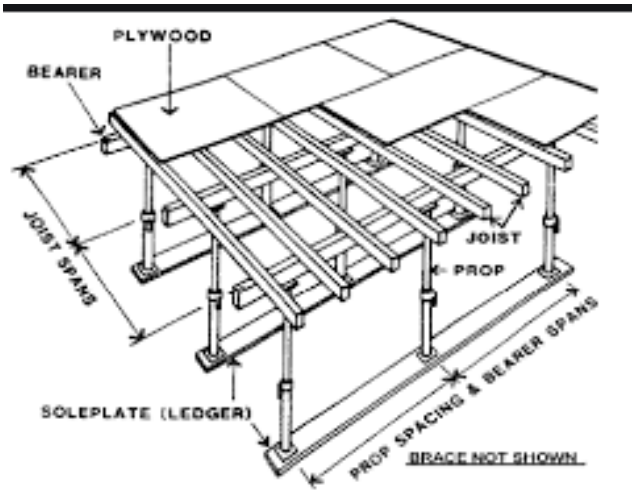

Figure 4: Diagram of the formwork
(Source: Collected by the researcher)

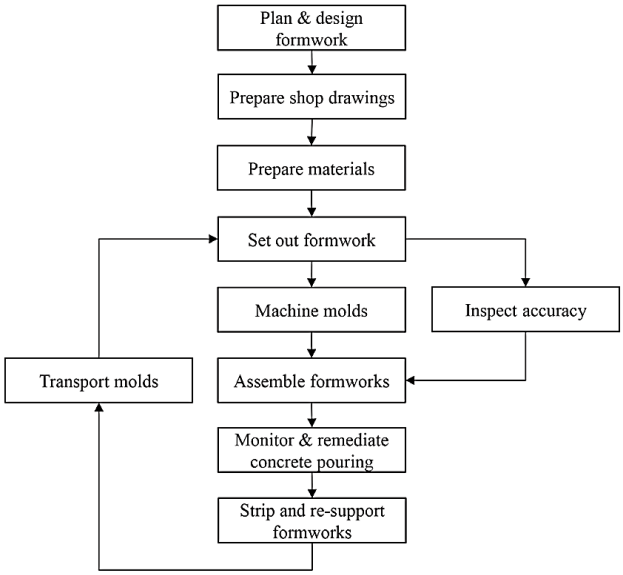

Figure 5: Proposed flowchart of the formwork
(Source: developed by the researcher)

The above flow chart as well as diagram help to analyse the result of this research. It has been found that accuracy can be managed by using formwork material in the construction project.

VII. CONCLUSION

It can be concluded that formwork materials are used in the sector of construction in an effectual manner. In addition to this, formwork materials are useful in the process of constructing building or other things in the market. Effects of the formwork materials need to be understood on a collective note. Additionally, the formwork materials are effective for the construction project to augment the efficiency of the work in a well manner. As for this reason, it is needed to assess the advantages of the formwork materials in the project of the construction work in the potential marketplace. It can be feasible to explicate that by measuring the efficiency of the formwork materials it is required to evaluate the efficacy of the consultation project. It can be elucidated that formwork materials are effective for the project of the construction to managing the process of casting on a collective note. This study is quite useful in order to understand the effectiveness of form in the project of construction.

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Area and Delay Optimization for Amba Bus Protocal in SOC Applications

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Abstract— System-on-a-Chip (SoC) design has become more and more complexly. Because difference functions components or IPs (Intellectual Property) will be integrated within a chip. The challenge of integration is "how to verify on-chip communication properties". Although traditional simulation-based on-chip bus protocol checking bus signals to obey bus transaction behavior or not, however, they are still lack of a chip-level dynamic verification to assist hardware debugging. We proposed a rule based synthesizable AMBA AXI protocol checker. The AXI protocol checker contains 44 rules to check on-chip communication properties accuracy. In the verification strategy, we use the Synopsys VIP (Verification IP) to verify AXI protocol checker. In the experimental results, the chip cost of AXI protocol checker is 70.7K gate counts and critical path is 4.13 ns (about 242 MHz) under TSMC 0.18um CMOS 1P6M Technology.

I. INTRODUCTION

In recent years, the improvement of the semiconductor process technology and the market requirement increasing. More difference functions IPs are integrated within a chip. Maybe each IPs had completed design and verification. But the integration of all IPs could not work together. The more common problem is violation bus protocol or transaction error. The bus-based architecture has become the major integrated methodology for implementing a SoC. The on-chip communication specification provides a standard interface that facilitates IPs integration and easily communicates with each IPs in a SoC. The semiconductor process technology is changing at a faster pace during 1971 semiconductor process technology was 10μm, during 2010 the technology is reduced to 32nm and future is promising for a process technology with 10nm. Intel, Toshiba and Samsung have reported that the process technology would be further reduced to 10nm in the future. So with decreasing process technology and increasing consumer design constraints SoC has evolved, where all the functional units of a system are modelled on a single chip.

To speed up SoC integration and promote IP reuse, several bus-based communication architecture standards have emerged over the past several years. Since the early 1990s, several onchip bus-based communication architecture standards have been proposed to handle the communication needs of emerging SoC design. Some of the popular standards include ARM Microcontroller Bus Architecture (AMBA) versions 2.0 and 3.0, IBM Core Connect, STMicroelectronics STBus, Sonics SMARRT Interconnect, Open Cores Wishbone, and Altera Avalon[1]. On the other hand, the designers just integrate their owned IPs with third party IPs into the SoC to significantly reduce design cycles. However, the main issue is that how to efficiently make sure the IP functionality, that works correctly after integrating to the corresponding bus architecture.

There are many verification works based on formal verification techniques [2]-[6]. Device under test (DUT) is modeled as finite-state transition and its properties are written by using computation tree logic (CTL) [7], and then using the verification tools is to verify DUT's behaviors [8]-[10]. Although formal verification can verify DUT's behaviors thoroughly, but here are still unpredictable bug in the chiplevel, which we want to verify them.

The benefits of using rule-based design include improving observability, reducing debug time, improving integration through correct usage checking, and improving communication through documentation. In the final purpose, increasing design quality while reducing the time-to-market and verification costs [19]. We anticipate that the AMBA AXI protocol checking technique will be more and more important in the future. Hence, we propose a synthesizable AMBA AXI protocol checker with an efficient verification mechanism based on rule checking methodology. There are 44 rules to check the AMBA AXI protocol that provide AXI master, slave, and default slave protocol issues.

A.AMBA AXI4 architecture:

AMBA AXI4 [3] supports data transfers up to 256 beats and unaligned data transfers using byte strobes. In AMBA AXI4 system 16 masters and 16 slaves are interfaced. Each master and slave has their own 4 bit ID tags. AMBA AXI4 system consists of master, slave and bus (arbiters and decoders). The system consists of five channels namely write address channel, write data channel, read data channel, read address channel, and write response channel. The AXI4 protocol supports the following mechanisms:

- Unaligned data transfers and up-dated write response requirements.
- Variable-length bursts, from 1 to 16 data transfers per burst.
- A burst with a transfer size of 8, 16, 32, 64, 128, 256, 512 or 1024 bits wide is supported.
- Updated AWCACHE and ARCACHE signaling details

Each transaction is burst-based which has address and control information on the address channel that describes the nature of the data to be transferred. The data is transferred between master and slave using a write data channel to the slave or a read data channel to the master. Table 1[3] gives the information of signals used in the complete design of the protocol.

The write operation process starts when the master sends an address and control information on the write address channel as shown in fig. 1. The master then sends each item of write data over the write data channel. The master keeps the VALID signal low until the write data is available. The master sends the last data item, the WLAST signal goes HIGH.

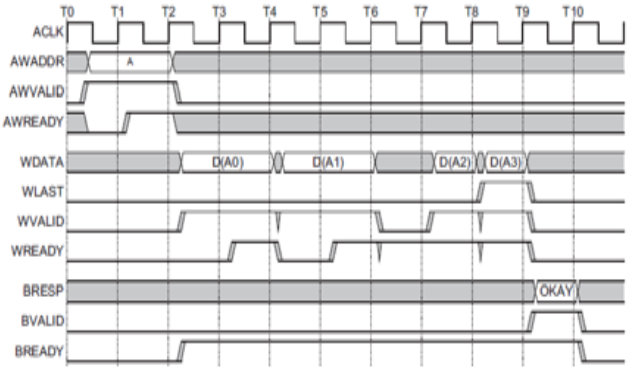

Figure 1: Write address and data burst.

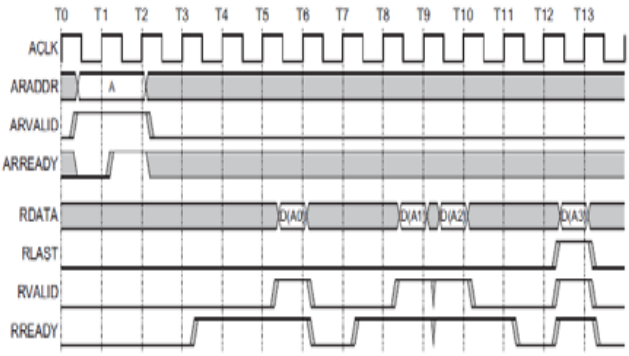

Figure 2: Read address and data burst.

TABLE 1: Signal descriptions of AMBA AXI4 protocol.

Signal	Source: master/ slave	Input/ Output	Description
Aclk	Global	Input	Global clock signal.
AResetn	Global	Input	Global reset signal
AWID[3:0]	Master	Input	Write address ID.
AWADDR[31:0]	Master	Input	Write address.
AWLEN[3:0]	Master	Input	Write burst length.
AWSIZE[2:0]	Master	Input	Write burst size.
AWBURST[1:0]	Master	Input	Write burst type.
AWLOCK[1:0]	Master	Input	Write lock type.
AWCACHE[3:0]	Master	Input	Write cache type.
AWPROT[2:0]	Master	Input	Write protection type.
WDATA[31:0]	Master	Input	Write data.
ARID[3:0]	Master	Input	Read address ID.
ARADDR[31:0]	Master	Input	Read address.
ARLEN[3:0]	Master	Input	Read Burst length.
ARSIZE[2:0]	Master	Input	Read Burst size.
ARLOCK[1:0]	Master	Input	Read Lock type.
ARCACHE[3:0]	Master	Input	Read Cache type.
ARPROT[2:0]	Master	Input	Read Protection type.
RDATA[31:0]	Master	Input	Read data.
WLAST	Master	Input	Write last.
RLAST	Slave	Output	Read last.
AWVALID	Master	Output	Write address valid.
AWREADY	Slave	Output	Write address ready.
WVALID	Master	Output	Write valid.
RAVLID	Slave	Output	Read valid.
WREADY	Slave	Output	Write ready.
BID[3:0]	Slave	Output	Write Response ID.
RID[3:0]	Slave	Output	Read response ID.
BRESP[1:0]	Slave	Output	Write response.
RRESP[1:0]	Slave	Output	Read response.
BVALID	Slave	Output	Write response valid.
BREADY	Master	Output	Response ready.
RVALID	Slave	Output	Read valid.

When the slave has accepted all the data items, it drives a write response signal BRESP[1:0] back to the master to indicate that the write transaction is complete. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR. After the read address appears on the address bus, the data transfer occurs on the read data channel as shown in fig. 2. The slave keeps the VALID signal LOW until the read data is available. For the final data transfer of the burst, the slave asserts the RLAST signal to show that the last data item is being transferred. The RRESP[1:0] signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.

The protocol supports 16 outstanding transactions, so each read and write transactions have ARID[3:0] and AWID [3:0] tags respectively. Once the read and write operation gets completed the module produces a RID[3:0] and BID[3:0] tags. If both the ID tags match, it indicates that the module has responded to right operation of ID tags. ID tags are needed for any operation because for each transaction concatenated input values are passed to module

B. Comparison of AMBA AXI3 and AXI4

AMBA AXI3 protocol has separate address/control and data phases, but AXI4 has updated write response requirements and updated AWCACHE and ARCACHE signaling details. AMBA AXI4 protocol supports for burst lengths up to 256 beats and Quality of Service (QoS) signaling. AXI has additional information on Ordering requirements and details of optional user signaling. AXI has the ability to issue multiple outstanding addresses and out-

oforder transaction completion, but AXI has the ability of removal of locked transactions and write interleaving. One major up-dation seen in AXI is that, it includes information on the use of default signaling and discusses the interoperability of components which can't be seen in AXI3.

In this paper features of AMBA AXI listed above are designed and verified. The rest of the paper is organized as follows: Section 2 discusses related work. Section 3 of this paper, discusses proposed work. In Section 4, simulation parameters are discussed. Section 5 discusses results. Future scope and concluding remarks are given in Section 6.

AMBA 3.0 AXI	AMBA 2.0 AHB
Channel-based specification, with five separate channels for read address, read data, writes address, write data, and write response enabling flexibility in implementation	Explicit bus-based specification, with single shared address bus and separate read and write data buses.
Burst mode requires transmitting address of only first data item on the bus.	Requires transmitting address of every data item transmitted on the bus.
Out-of-Order ransaction completion provides native support for multiple, outstanding ransactions.	Simpler SPLIT transaction scheme provides limited and rudimentary outstanding transaction completion
Fixed burst mode for memory mapped I/O peripherals.	No fixed burst mode.
Advanced security and cache hint support.	Simple protection and cache hint support.
Native low-power clock control interface.	No low-power interface.
Default bus matrix topology support.	Default hierarchical bus topology support

II. RELATED WORK

In a SoC, it houses many components and electronic modules, to interconnect these a bus is necessary. There are many buses introduced in the due course some of them being AMBA [2] developed by ARM, CORE CONNECT [4] developed by IBM, WISHBONE [5] developed by Silicore Corporation, etc. Different buses have their own properties the designer selects the bus best suited for his application. The AMBA bus was introduced by ARM Ltd in 1996 which is a registered trademark of ARM Ltd. Later advanced system bus (ASB) and advanced peripheral bus (APB) were released in 1995, AHB in 1999, and AXI in 2003[6]. AMBA bus finds application in wide area. AMBA AXI bus is used to reduce the precharge time using dynamic SDRAM access scheduler (DSAS) [7]. Here the memory controller is capable of predicting future operations thus throughput is improved. Efficient Bus Interface (EBI) [8] is designed for mobile systems to reduce the required memory to be transferred to the IP, through AMBA3 AXI. The advantages of introducing Network-on-chip (NoC) within SoC such as quality of signal, dynamic routing, and communication links was discussed in [9]. To verify on-chip communication properties rule based synthesizable AMBA AXI protocol checker [10] is used.

1) Master

2) AMBA AXI4 Interconnect

2.1) Arbiters

2.2) Decoders

3) Slave

The master is connected to the interconnect using a slave interface and the slave is connected to the interconnect using a master interface as shown in fig. 3. The AXI4 master gets connected to the AXI4 slave interface port of the interconnect and the AXI slave gets connected to the AXI4 Master interface port of the interconnect. The parallel capability of this interconnects enables master M1 to access one slave at the same as master M0 is accessing the other.

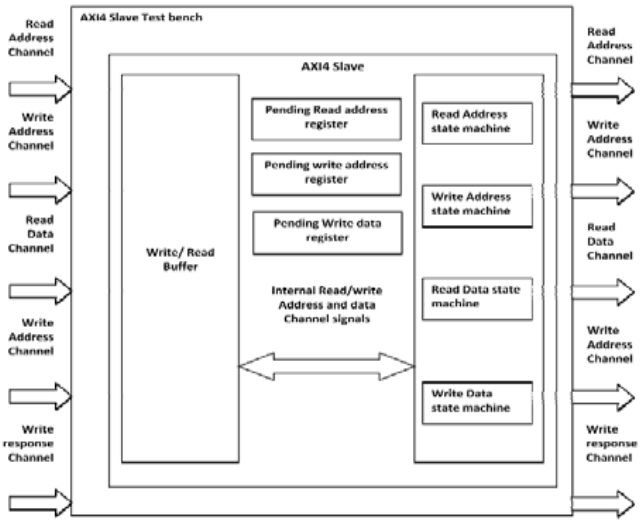

Figure 4: AMBA AXI slave Read/Write block Diagram

III. SIMULATION

Simulation is being carried out on Model Sim Quretus II[11] which is trademark of Menter Graphics, using Verilog [12] as programming language. The test case is run for multiple operations and the waveforms are visible in discovery visualization environment

A. Simulation inputs

To perform multiple write and read operations, the concatenated input format and their values passed to invoke a function is shown in the fig. 6 and 7 respectively. Here the normal type of the burst is passed to module. Internal_lock value is 0, internal_burst value is 1 and internal_prot value is 1,for both read and write operations, which indicate that the burst is of normal type. For write

operation address locations passed to module are 40, 12, 35, 42 and 102; for read operations 45, 12, 67 and 98.

B. Simulation outputs

The simulation output signals generated are as follows:

- From input side the validating signals AWVALID/ARVALID signals are generated by interconnect which gives the information about valid address and ID tags.
- For write operations BRESP[1:0] response signal generated from slave indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLERR, and DECERR.
- For read operations RLAST signal is raised by slave for every transaction which indicates the completion of operation

IV. RESULTS

Simulation is carried out in Modelsim tool and Verilog is used as programming language.

A. Simulation result for write operation

The AResetn signal is active low. Master drives the address, and the slave accepts it one cycle later. The write address values passed to module are 40, 12, 35, 42 and 102 as shown in fig. 8 and the simulated result for single write data operation is shown in fig. 9. Input AWID[3:0] value is 11 for 40 address location, which is same as the BID[3:0] signal for 40 address location which is identification tag of the write response. The BID[3:0] value is matching with the AWID[3:0] value of the write transaction which indicates the slave is responding correctly. BRESP[1:0] signal that is write response signal from slave is 0 which indicates OKAY. Simulation result of slave for multiple write data operation is shown in fig. 10.

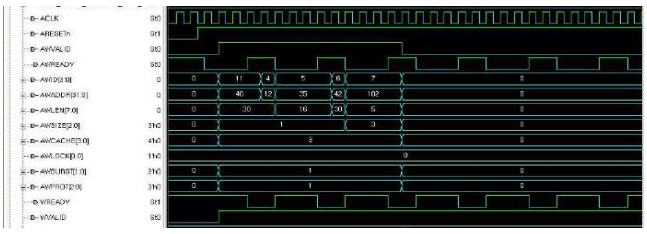

Fig 8: Simulation result of slave for write address operation

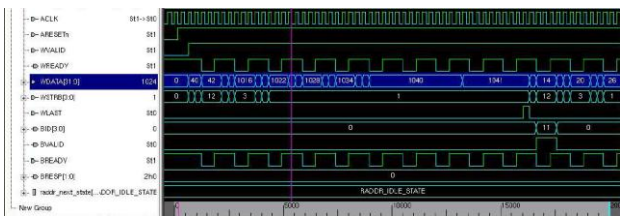

Fig9: Simulation result of slave for single write data operation

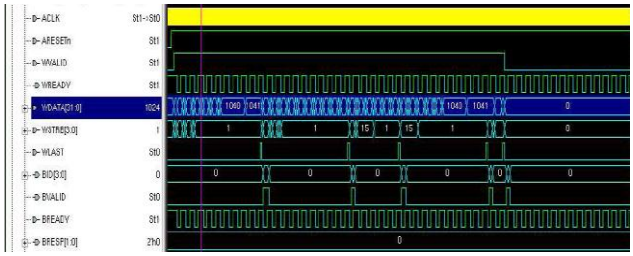

Figure 10: Simulation result of slave for multiple write data operation

B. Simulation result for read operation

The read address values passed to module are 45, 12, 67, 98 as shown in fig. 11 and the simulated result for single read data operation is shown in fig. 12.

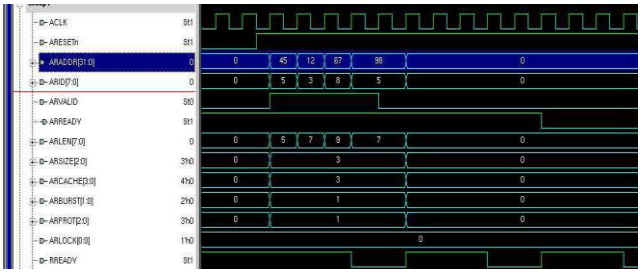

Figure 11: Simulation result of slave for read address operation

Input ARID[3:0] value is 3 for 12 address location, which is same as the RID[3:0] signal for 12 address location which is identification tag of the write response. The RID[3:0] and ARID[3:0] values are matching, which indicates slave has responded properly. RLAST signal from slave indicates the last transfer in a read burst. Simulation result of slave for multiple read data operation is shown in fig. 13.

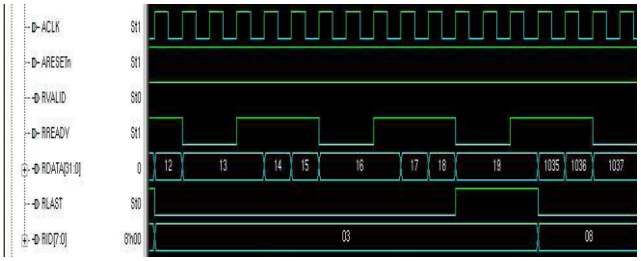

Figure 12: Simulation result of slave for single read data operation

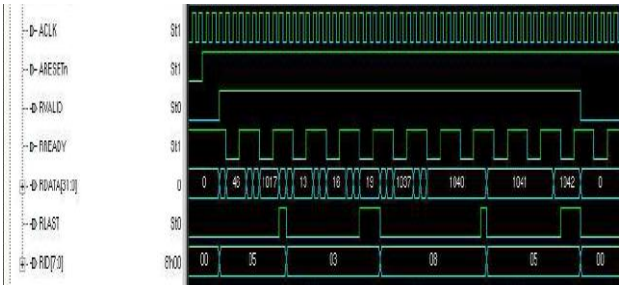

Figure 13: Simulation result of slave for multiple read data operation.

V. CONCLUSION AND FUTURE SCOPE

A. Future scope

The AMBA AXI4 has limitations with respect to the burst data and beats of information to be transferred. The burst must not cross the 4k boundary. Bursts longer than 16 beats are only supported for the INCR burst type. Both WRAP and FIXED burst types remain constrained to a maximum burst length of 16 beats. These are the drawbacks of AMBA AXI system which need to be overcome.

B. Conclusion

AMBA AXI4 is a plug and play IP protocol released by ARM, defines both bus specification and a technology independent methodology for designing, implementing and testing customized high-integration embedded interfaces. The data to be read or written to the slave is assumed to be given by the master and is read or written to a particular address location of slave through decoder. In this work, slave was modeled in Verilog with operating frequency of 100MHz and simulation results were shown in Modelsim tool. To perform single read operation it consumed 160ns and for single write operation 565ns.

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Analysis of Precast Segmental Post-Tensioned Concrete Bridge

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Abstract— Segmental bridge construction is a method of incremental construction of segments, stitching them to the segments already placed, by pre-stressing. The use of precast segmental concrete bridges is been increased in past decades due to the demand for speedy construction. A simple method is adapted to approach towards objective where two models were created using MIDAS-Civil considering parameters from Indian Standard Code and Euro Code. Midas Civil is software developed by MIDAS IT, used for bridge structural analysis and design. With the help of this software, models of post-tensioned segmental bridge are analyzed for different loading condition (e.g.; Vehicular loading), and comparison of bridge model is done using IS Codes and EURO Codes.

Index Terms— Euro Code, IS Code, Precast Segmental Bridge, Vehicular Load

I. INTRODUCTION

The construction of post tensioned segmental bridges has been recognized as one of the most efficient type of bridges without the need for extensive false work. This method has great advantages over other kinds of construction, particularly in urban areas where temporary shoring would disrupt traffic and the services below, in roadways and over waterways where false work would not only be expensive but also a hazard

II. METHODOLOGY

A simple method is adapted to approach towards objective where two models were created using MIDAS-Civil considering parameters from Indian Standard Code and Euro Code. Several software packages are available for numerical simulation and analysis of structures. MIDAS-Civil is one such software used widely by professional to analyze bridges. MIDAS- Civil software is used for the work presented in this thesis. The models which were created using Midas Civil were confirmed by IS Code (IRC 112-2011) and Euro Code (EN 1992-2 (2005)).

Clauses Referred from Codes are as mentioned below in table form

Table 1. Materials

MATERIAL PROPERTIES	
IRC 112: 2011	EN 1992-2 (2005)
M50 - PIER M40 – GIRDER	C50/60 – PIER & GIRDER
FE500 - STEEL	Y1770S7 - STEEL
Clauses Referred	
CL 5.5.1 & CL6.4.1 PAGE 142 – TABLE 14.2	EN 1992.1.1 SECTION 3 – MATERIALS CL 3.1.1

Table 2. Vehicular Load

MOVING LOAD	
IRC 6-2017	EN 1991-2 (2003)
CLASS A CLASS 70R	LOAD MODEL 1 LOAD MODEL 3 SV100
Clauses Referred	
CL 201	CL 4.3

Modeling of Bridge in MIDAS, bridge model can be created in two ways, the first and basic way of creating the model is by node creation method, and the second method is by structure wizard which is more time efficient. The models which are created in this project are by structure wizard.

Two models of same dimensional properties are created by structure wizard, main difference between the two models are their material properties and vehicular loading which is applied according to the IS codes and another one with EURO codes.

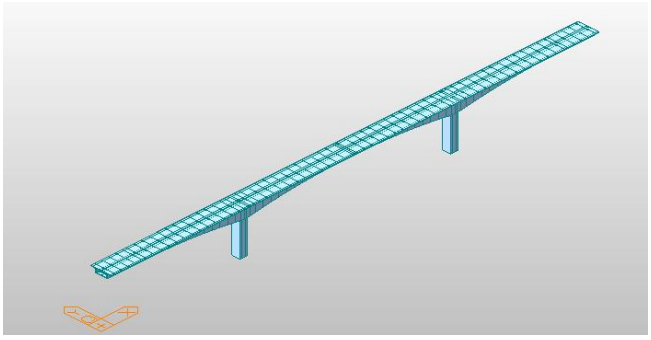

Figure 1. Rendered Model

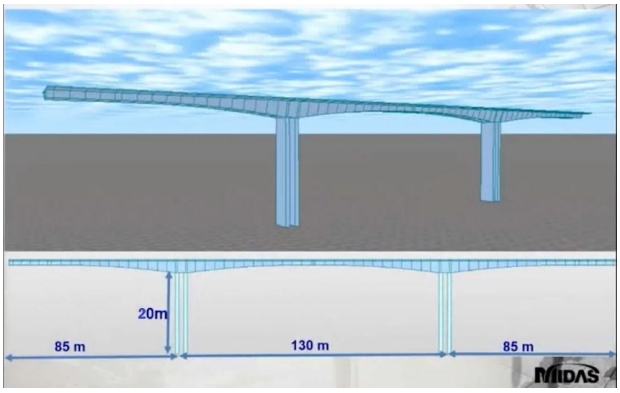

Figure 2. Dimensional Properties of Bridge

Vehicular load was applied in both the models, and two-lane bridge was considered, as per IS code, if the width of the bridge is between 9 m to 13 m bridge should be of two lanned.

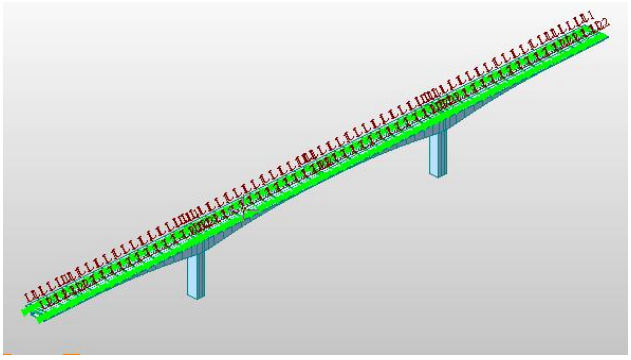

Figure 3. Lane Profile

Construction Stages: Segmental bridges are constructed in different stages, e.g., after casting pier, diaphragm is placed and then box girder is attached with the help of cranes. Thus, at different construction stages various load acts on bridge like traveler load, self-weight etc., and we have to consider the construction stage loads in analysis of segmental bridge for the correct analysis. In this bridge model the construction stage is divided into 12 parts, so as to understand what the various loading pattern are and what they differ at various stages of the construction.

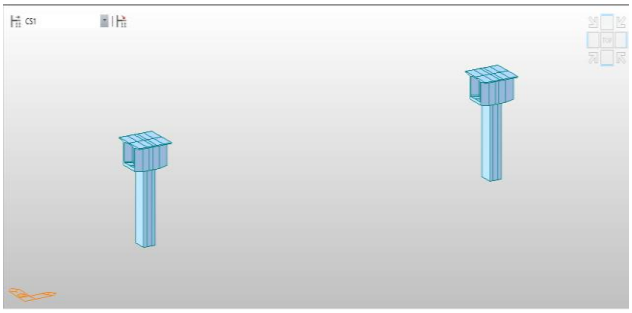

Figure 4. Construction Stage 1

Traveler Load: Traveler load is one of the important aspect to be considered in the segmental bridge construction, as you can see in the below figure the traveler load for construction stage 9 in x direction and y direction.

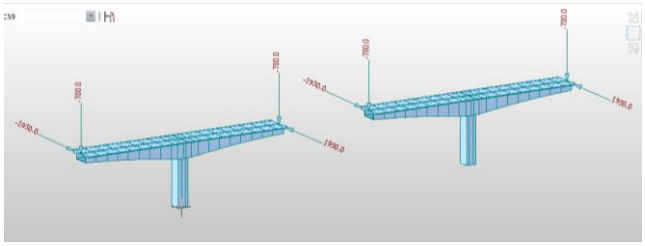

Figure 5. Traveler load

Tendon Profiles: Tendons are placed simultaneously after placing the box girder, after each construction stage tendons are placed and stretched. Tendons are placed in top as well as in bottom of box girder.

Duct diameter and tendon property was selected according to the respective codes of the country, in both the models duct diameter of 110mm was used.

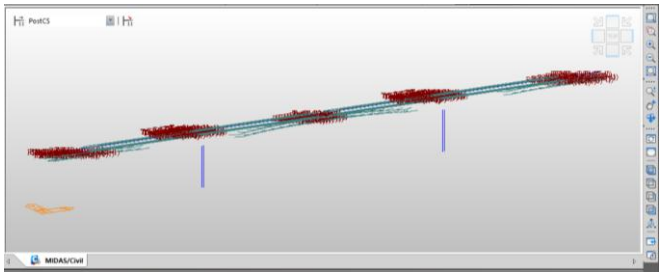

Figure 6. Tendon Profile

III. RESULT

Behavior of bridge due to Moments

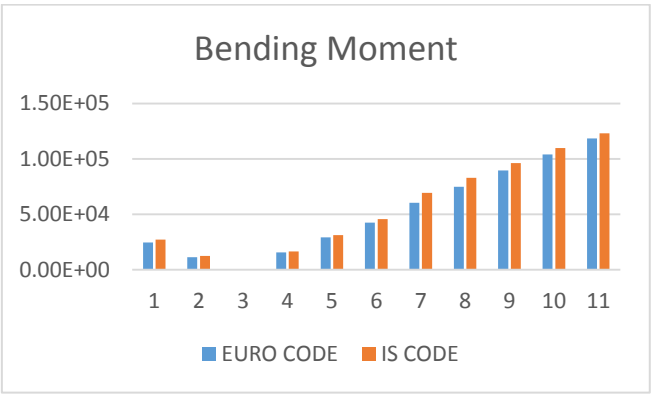

Figure 7. Bending Moment values in KN/m indicating values positive to negative moments

Behavior of bridge due to Shear Force

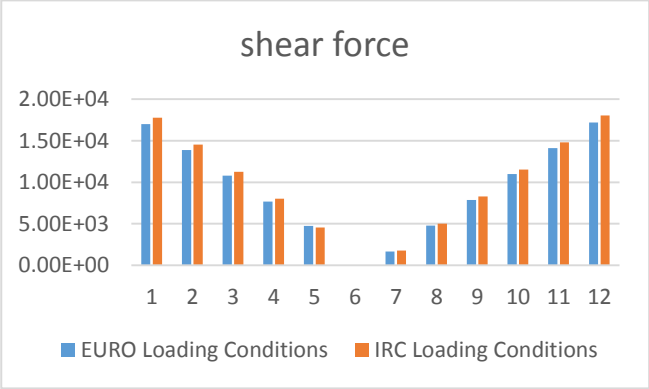

Figure 8. Shear Force values in KN/m indicating values positive to negative forces

Behavior of Pier due to Loads & Moments

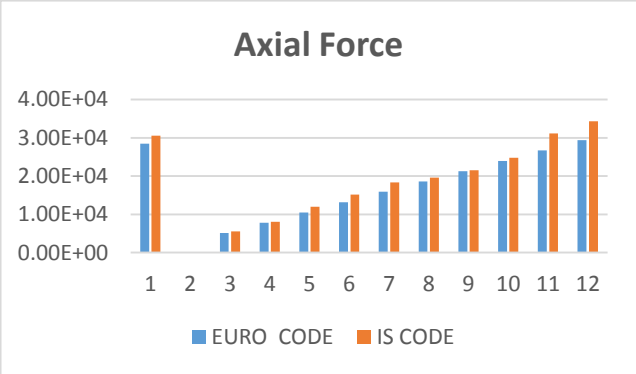

Figure 8. Axial Force values in KN/m indicating values positive to negative forces

Section Capacity Check:

The maximum load which is bearable by the box girder is to be used and checked whether the deck is capable to bear the loads safely without abrupt deflection.

The green line indicates the maximum moment carrying capacity of the section, and the colored contour indicates the actual moments on the section

The contour should not cross the maximum moment capacity; In this case, the section can safely bear the loads and moments.

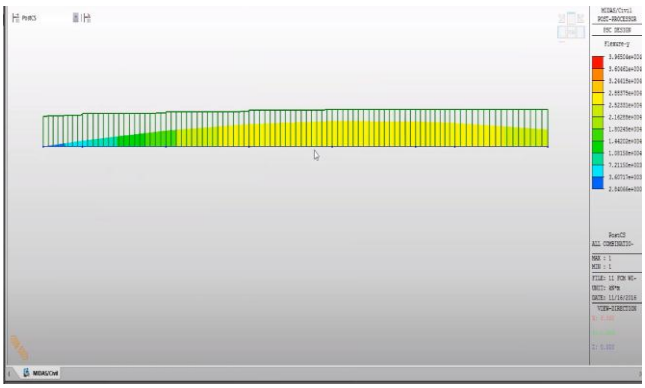

Figure 9. Section Capacity Check

IV. CONCLUSION

The work presented here was with the aim to evaluate the factor mentioned in the IS CODE and EUROPEAN CODE for the behavior of bridge under vehicular loading. The methodology to achieve aim was successfully developed, validated and executed over various bridge models. The conclusion that can be drawn out is as follows

- The very obvious observation is that there is increase in the value of the reaction, bending moments and deflection in bridge model which was generated using IS code parameters (Model 2) as compared to the model which was created using EURO code parameters (Model 1).
- Another equally obvious observation is that there is more dynamic load acting on pier in Model 2 rather than Model 1.
- At each construction stage the section was capable to resist the loads safely in both the models.
- Due to variance in the vehicular load application on the lanes in both the models, it was seen that there is less load acting on Model 1 as compared to Model 2.
- The basic understanding to reduce moments in case of long span structure is to use higher grade of concrete in box girders and use Tendons of higher strength.

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Synthesis and Structural Studies of Eu Doped Ni-Zn Nano Ferrites

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Abstract---The ferrites are the magnetic materials exhibiting properties which are commercially used for magnetic storage, microwave absorption and permanent magnets. The different types of ferrites include spinel type, garnet type and hexagonal ferrites. Ferrites have electrical and magnetic unique characteristics which are useful for wide range of applications. Nickel Zinc ferrites are provided with Low loss, High magnetic field, Thermal shock resistance, Stress resistance, High permeability, Rotary transformers, additionally, Ni-Zn ferrite materials have the advantage of high resistively, high curie temperature, low temperature factor, low relative loss features. In this paper, the influence of small substitution of iron with Europium in nickel zinc nano ferrites has been investigated. The samples were prepared through Citrate Sol-Gel method. The powders were calcinated at 500oC for 2hrs. To confirm the crystal structure of the samples, X-Ray diffraction has been used. It has been found from the XRD data that all the samples are exhibiting diffraction peaks indicating the nano crystalline nature of the samples. There is a small secondary Fe2O3 peak in x=0.002 and 0.008 samples. XRD data has been analyzed with Fullprof Rietveld refinement analysis. The sample crystallized in Cubic structure with F d-3 m space group. The lattice parameters were calculated and the values varying with the Eu doping. The crystallite size, lattice strain were calculated and the details are discussed in the manuscript.

Keywords---Nano ferrites, Citrate Gel Method, Micro-Strain, Rare-earth cations, Spinel ferrites

IOT Network in Indoor Environment Monitoring

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Abstract--- Air pollution is an important environmental issue that has a direct effect on human health. In this paper the development of an Internet of Things-based system for real time indoor personal exposure monitoring is described. The system was tested for real time personal exposure assessment to formaldehyde and CO_2 air pollutants. It provides accurate and real time personal exposure assessment. New IoT advances promise more fine-grained data, better accuracy, and flexibility. Effective forecasting requires high detail and flexibility in range, instrument type, and deployment. This allows early detection and early responses to prevent loss of life and property the real time and continuous monitoring capability makes it possible to better predict worker health risks and protect them from occupational overexposure to air pollution. IoT improves on this technology by reducing the need for human labor, allowing frequent sampling, increasing the range of sampling and monitoring, allowing sophisticated testing on-site and binding response efforts to detection systems. This allows us to prevent substantial contamination and related disasters.

Gas Detection and Auto Valve Shutdown

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Abstract---Safety is becoming a big issue at present. What's more, home flames have incurred significant damage in lives and property in ongoing year. LPG is profoundly inflammable and can devour even at some great ways from the well spring of leakage.

As the use of LPG gas is increasing day by day, the risk of its leakage and damages caused by this leakage is also increasing in same ratio. Smart Gas management system monitors leakage and fire. The main aim of this system is to design the model and circuit board that control exhaust fan automatically when detects leakage of LPG. In addition to that, alert message and call will be sent to the house owner so that he/she can turn off gas valve on time before much damages are caused by leakage. The essential rule behind the caution discovery is the adjustment in the centralization of air.

LPG is utilized in numerous necessities, for example, home grown fuel, mechanical fuel, auto movable fuel. So the principle point of the proposed frame work is to give welfare from the gas spills. The frame work recognizes the spillage of LPG utilizing a gas sensor and cautions the customer about the gas spill by sending the SMS. The frame work additionally turns on the buzzer and exhaust fan with goal that leakage can be conveyed. It is useful for us to maintain a strategic distance from the blast. Typically, individuals don't utilize any gas indicator gadget to check any LPG (liquefied petroleum gas) spillage in the kitchen since blast seldom occurs. Yet, it can't be measure, at some point it unexpectedly happened.

The result of every module can be viewed in LCD display. Buzzer starts beeping if leakage or wastage of gas has been detected. Thus, the damages caused due to gas leakage can be minimized.

Examination Room Guide Using RFID

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Abstract---The main functionality of this project is to access the examination hall details of an individual through RFID technology. For this purpose, the authorized person is given an RFID card. This card contains an integrated circuit that is used for storing, processing information through modulating and demodulating of the radio frequency signal that is being transmitted. Thus, the data stored in this card is referred as the details of the person.

Seating Arrangement of students during examinations is distributed. Students face difficulties as they have to scrounge for their examination hall numbers and seating arrangement while they are wits end. An innovation which could aid the students in finding their exam halls and seats would be welcoming and very rewarding. This project, presents a modernized method of examination hall management. It is possible for a student to identify the particular exam hall from any other hall, when they scan RFID card at the RFID reader present in the premises. This helps them to identify the floor or get directions to their respective halls without delays. The card reader is provided at the entrance of the building and if the unauthorized card is scanned, a buzzer alarm will be activated, otherwise the room number is displayed on the LCD, interfaced to controller.

GSM Based Home Automation Application

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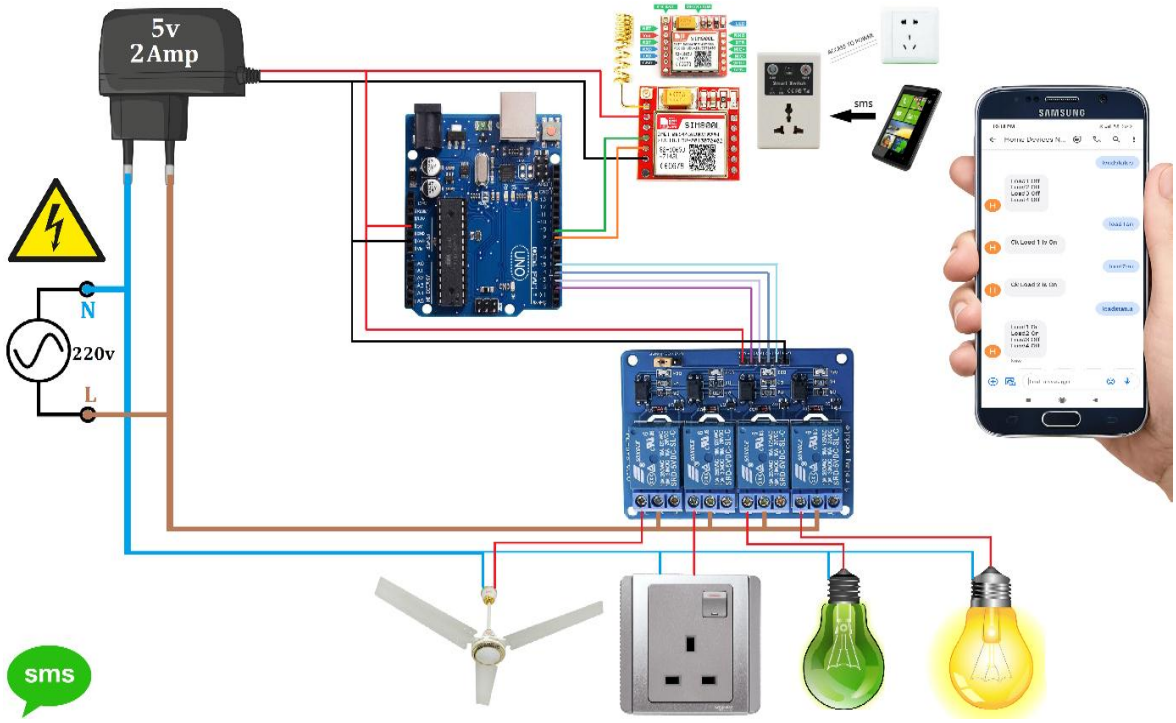
Abstract--- This research work investigates the potential of 'Full Home Control', which is the aim of the Home Automation Systems in near future. The analysis and implementation of the home automation technology using Global System for Mobile Communication (GSM) modem to control home appliances such as light, conditional system, and security system via Short Message Service (SMS) text messages is presented in this paper. The proposed research work is focused on functionality of the GSM protocol, which allows the user to control the target system away from residential using the frequency bandwidths. The concept of serial communication and AT-commands has been applied towards development of the smart GSM-based home automation system. Home owners will be able to receive feedback status of any home appliances under control whether switched on or off remotely from their mobile phones. Arduino UNO with the integration of GSM provides the smart automated house system with the desired band rate of 9600 bps. The proposed prototype of GSM based home automation system was implemented and tested with maximum of two loads and shows the accuracy of ≥98%.

CIRCUIT DIAGRAM:



Sign Language Translator

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Abstract---Sign language is the only way to communicate for listening and talking with disabled people. Approximately 10% of deaf people use sign language as their first language. We designed a hand glove that will make the sign language understandable to all. The result is shown on the LCD display of the glove. When the finger is moved, word will be detected according to valid movement. As a consequence, the output will be displayed on LCD .A flex sensor uses carbon on a strip of plastic to act like a variable resistor. The resistance changes by flexing the component. The sensor bends in one direction, the more it bends, the higher the resistance gets.

Design and Implementation of Automated Serving Robo

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Abstract--- In today's world the use of robot is going on increasing. Robots are able to carry out every work more effectively and efficiently than a man can do. Hence one of such application of robot could be SERVING ROBO. There are many areas of research that could be done for a serving robot. In this paper we have try to demonstrate a prototype of Autonomous Serving Robot which will take order and serve the food to the customer. The implementation is done with available resources to reduce the cost of project. The robotics technology is replacing manual work at a fast place throughout the world. In classical cafe, restaurants and hotels, the customers face a lot of problems due to congestion at peak hours, unavailability of waiters and due to manual order processing. These shortcomings can be handled by using a restaurant automation system where "Waiter Robots" are used for ordering food and beverages.

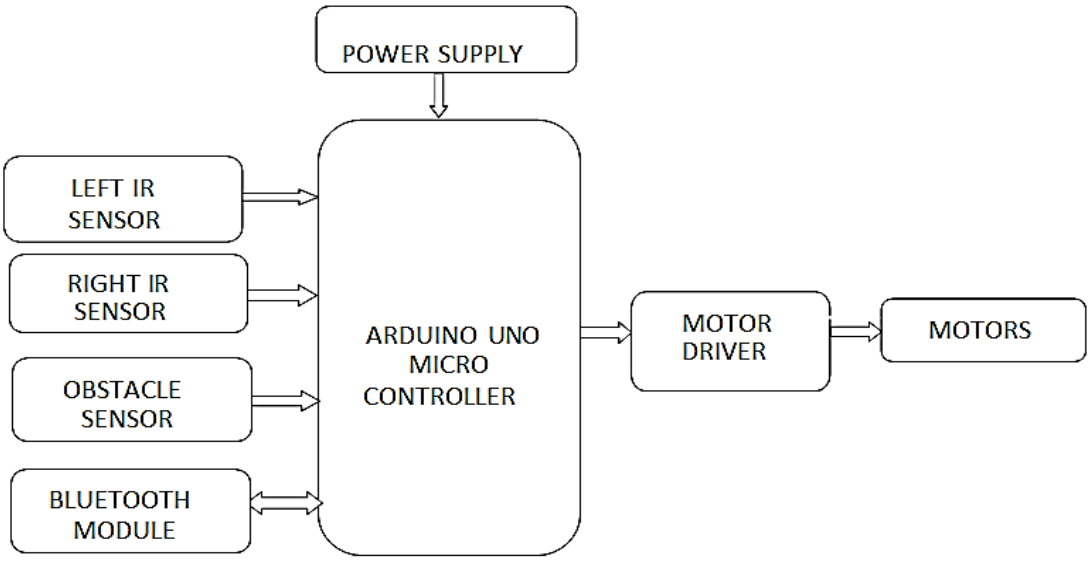
In this project we are taking the idea of were there may be several tables which are arranged in round. This is done to provide a simple path to the robot. Besides this there is a circular track which is of black colour for the movement of the robot. It consists of the counter, robot and the arrangement of the tables. The robot will start following black line, when it will get a white light in the way it will stop and it will take the order from the customer and send it to counter. After the preparation of food, it will come back and serve the food. After serving it will again follow the returning black line path and come to the starting position. The model consists of the following segments:

Line Follower The Robot will move in the particular directions as for the commands. we give Line follower actually senses the line and follows it. We use here the behaviour of light at the black and white surfaces. When light falls on a white surface it is almost fully reflected and in the case of a black surface light is completely absorbed. This behaviour of light is used in building a line follower robot.

Obstacle Detector An obstacle detector is an intelligent feature of the device, which can automatically sense obstacles on its path. It is designed by using IR sensor. The principle behind it is that whenever an obstacle comes in front of the IR sensor there will be a change in output of sensor and this change will be detected by micro- controller and hence the obstacle is detected.

Wireless Technology The wireless technology (BLUETOOTH Technology) is used to give the direction control to move the robot in respective table.

BLOCK DIAGRAM:



Voice Controlled Robotic Vehicle

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Abstract--- Voice controlled robotic system is very beneficial in areas where there is high risk for humans to enter. Voice controlled robotic system is controlled through voice commands via android device. The integration of control unit with Bluetooth device is achieved using a Bluetooth module to capture and read the voice commands. The robotic vehicle operates as per the command received via android device, for this Arduino is integrated in the system. The controlling device may be any smart phone having an Android Operating System. The transmitter uses an android application required for transmitting the data. The receiver end reads these commands and interprets them into controlling the robotic vehicle. The android device sends commands to move the vehicle in forward, backward, right and left directions.

After receiving the commands, Arduino operates the motors in order to move the vehicle in four directions. The communication between android device and receiver is sent as serial communication data. Arduino program is designed to move the motor through a motor driver circuit as per the commands sent by android device. A robotic arm is mounted at the front of the system to make changes in the environment. An obstacle detector is added to protect the system from object on the way by using an ultrasonic sensor.

Removal of Chromium from Waste Water Using Coal Fly Ash

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Abstract---Coal Fly Ash is produced by coal-fired electric and steam generating plants is the finely divided residue that results from the combustion of pulverized coal. It mainly comprised of oxides having high adsorption capacity. Coal fly ash is used as a low-cost adsorbent to remove heavy metals such as Lead, Chromium, Arsenic, Cadmium etc. from industrial wastewater. Wastewater containing Chromium has adverse effects on environment like changing leaching of soil, soil fertility disorders, contamination of natural water etc. The constant exposure of Chromium causes various health disorders like Respiratory tract irritants, pulmonary sensitization, Risk of lung, nasal and sinus cancer, severe dermatitis and skin ulcers etc.

The main aim of the present work is to remove Chromium from wastewater by using coal fly ash by using adsorption. The effect of contact time, pH, concentration and dosage of fly ash was studied. The kinetic studies and isotherms were also developed.

Keywords--- Waste water, Chromium, Fly ash, Adsorption

Mobile Charging on Insertion of Coin

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Abstract--- Now a days mobile phones plays important role in the present communication world as well as day to day life. This paper describes the mobile battery charging on insertion of coin. So to operate these mobile phones public charging is needed, and it should be useful to public. The coin based mobile charging system charges the mobile phones when the coin is inserted.

This system is used by shop owners, rural people and can be implemented in the public place like railway stations, bus stand to provide mobile charging facility. So the coin acceptor recognizes valid coins and then signals the arduino for further action. If a valid coin is found, it signals the arduino and then arduino starts the mobile charging mechanism by providing 5V supply through power section to the mobile phone. The arduino starts a reverse countdown timer to display the charging time for that mobile phone. Further the user adds another coin, the arduino adds to the currently remaining time and once again decrements the countdown.

This system can be used for smart mobile charging at public places. This coin based mobile charging system will supply the enough amount of charge to the mobile phone.So that the mobile phone users can reactivate a low or dead battery by simply plugging in and charging for one rupee.

Smart Helmet for Two Wheeler

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Abstract--- There are thousands of highway deaths and serious injuries due to "Run-Off-Road" accidents. Everything from simple driver inattentiveness, to fatigue, to driving-while-impaired, to drunken driving is responsible. This is a much more common cause of single vehicle fatalities than is generally thought. In India most of the people prefer two wheelers compared to other vehicle due to simplicity and its low cost. A smart helmet is a type of protective headgear used by the rider which makes bike driving safer than before. A smart helmet is a special idea which makes motorcycle driving safer. The main aim of the smart helmet is to prevent the biker from starting his bike until and unless he actually wears the helmet.

The main aim of this smart helmet is to provide safety for the rider. In addition other advance features like alcohol detection is also built in the helmet. This makes not only smart helmet but future of smart bike. Its compulsory to wear helmet, without helmet ignition switch cannot ON. If the rider is drunk, automatically ignition is switched OFF automatically. The wireless communication implemented between the smart helmet and the vehicle is through RF technology. In addition the vehicle speed is also monitored and when exceeds more than the specific speed automatic acknowledge will be given by activating the alarm or the buzzer. This is demonstrated through a DC motor operation controlled via two relays with two different voltages applied to the DC motor by the controller. A limit switch is used to identify whether the helmet is put ON the head or not and a alcohol (gas) sensor MQ2 for drunken driving. The DC motor is used to indicate the vehicle running condition. The helmet will communicate with the bike unit through RF communication.

Knowledge Discovery from e Government Data: A Text Mining Approach

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Abstract--- Nowadays, citizens are increasingly using the possibilities offered by the new generation of the World Wide Web (Web 2) to interact and exchange views on eGovernment issues on social networking sites (blogs or microblogs and wikis), thus participating in social dialogue. This process results in the creation of 'collective opinions' on both service delivery and legislative issues commented on in these virtual communities. This general opinion of citizens and the specific opinion of each individual are of particular importance because they can provide useful feedback information that can lead to improvements, both in the provision of eGovernment services and in filling legislative gaps (e. g. laws under public consultation, participatory budgeting, etc.). Since the volume of this collective information is growing exponentially, and on the other side, the textual form of these data, it is obvious, to be able to estimate the feedback information it is necessary to use text mining techniques.

Solar Powered Floating Trash Collector with Water Purifier

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Abstract--- Water is essential for our life, and there is no life without water on earth. It is important to maintain its cleanliness as it is the basic need for all living organisms on Earth. Water gets polluted due to many reasons such as waste from industry, garbage waste, sewage waste etc. This makes water unfit for drinking and other human activities. All urban water bodies in India are enduring a direct result of contamination and this results in scarcity of clean water. We have to incorporate technology such that cleaning work is done efficiently and effectively.

This project helps in reducing pollution of water bodies thereby serves as a helping hand in removing scarcity of clean water. The main aim of our project is to collect trashes from water bodies together with purification of water. The system is made as a floating apparatus, when powered, it starts to float through water body and collect trashes. Along with trash collection a considerable amount of water is purified using filters. To make the boat self-sustainable, two solar panel are used which would charge the battery. When the Microcontroller is powered, it will drive the DC motors; motor for conveyer belt mechanism and motor for purification. Ardupilot, an open source unmanned vehicle Autopilot software suite is used for autonomous vehicle control. Finally, a Wi-Fi module is used for visualising the status of microcontroller working. Thus by incorporating this technology water scarcity and water purification can be overcome.

Implementation of Human Speed Detection Using 8051 Microcontroller

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Abstract--- The main aim of our project is to detect the speed of humans. Thus this system proves very beneficial in areas of sports. In order to record the speed of humans, this system uses a handheld radar gun pointing towards the person of whose speed is to be detected. In case of running race, it may be required to detect speed of the participants to take the decision or for some other reason. The proposed system calculates the speed by considering the time taken parameter to travel from start to end point. For this IR transmitter and receiver are installed on either of the road side on the set points. Calculation of the time taken by the human is done by the control unit of 8051 Microcontroller. The speed of the human is displayed on a LCD display.

We have used 8051 Microcontroller as the base unit on which our Project has been built upon. The objective of our Project is to determine the Speed travelled by humans and to display it automatically based on Microcontroller Programming. In earlier days, we used to have stopwatches, clocks or any random person to determine the speed. But now due to the advancement of Technology, we have developed this project to determine speed of humans without any external help. This Project can detect the human's movement using Infrared LED's on both sides and determines the speed with which they have moved from one place to another. The Speed can be calculated using the basic formula of ratio of distance travelled and time taken. The Infrared LED's will sense the movements of humans and send the details to Microcontroller, which is the heart of our Project. The Microcontroller then calculates the Speed based on the registered commands which are given using C Programming language. The end result as computed by 8051 will be displayed on LCD Screen helps us to determine the human speed automatically without any external help.

This Project is particularly used in Sports where it comes handy to measure the speed of athlete's in various games such as Running races where Speed plays Crucial factor in determining the winners without much of human effort. It can save lot of our time and efforts which otherwise used in holding the stopwatch just to check for Speed. This Project also helps with accurate results with no compromise to external factors like atmosphere & other environmental conditions. Thus our project is robust and plays a vital role in today's generation where Speed holds utmost importance in almost everything that we do. We made our project by keeping in mind the cost reductions and thus it's very economical.

GSM Based Vehicle Fuel Theft Detection System with SMS Indication

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Abstract--- GSM based Vehicle Fuel Theft Detection System with SMS indication has application in Bikes, cars and all other vehicles. This project has a GSM modem which send SMS to owner of vehicle when there is fuel theft going on.Vehicle Petrol theft is one of the main concerns of many bike owners and car owners. Many times we have heard or some of us have already faced that petrol from their bike or cars has been stolen. Main intention of this project is to avoid such situation. In SMS based petrol theft detection system, we have used a Level sensor to detect the petrol level in petrol tank. If the level goes below certain threshold level then this sensor gives a particular signal to the microcontroller. Then microcontroller turns on the buzzer and sends SMS to the car/bike owner.

Microcontroller is a main heart or Central Processing Unit of the system.

One question arises here is that what if we are driving our car or bike? In this case petrol or the diesel level will decrease which can trigger the microcontroller through the level sensor. To avoid this situation we have taken a signal from ignition key. Whenever the bike owner or car owner or driver inserts key into the ignition lock and switch it on then at that time a signal will be given to the microcontroller. This way microcontroller understands that the bike/car has been started and so it will not monitor fuel level.

We have provided bike ignition key with this project. Level sensor is turned on only when the key is removed from the ignition lock. So once the person gets out of the car then he/she will remove the key and system is activated.

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